Comparison of Electrical Failure Mechanisms in COTS Parts and Their Scaling with Supply Voltage – An Overview

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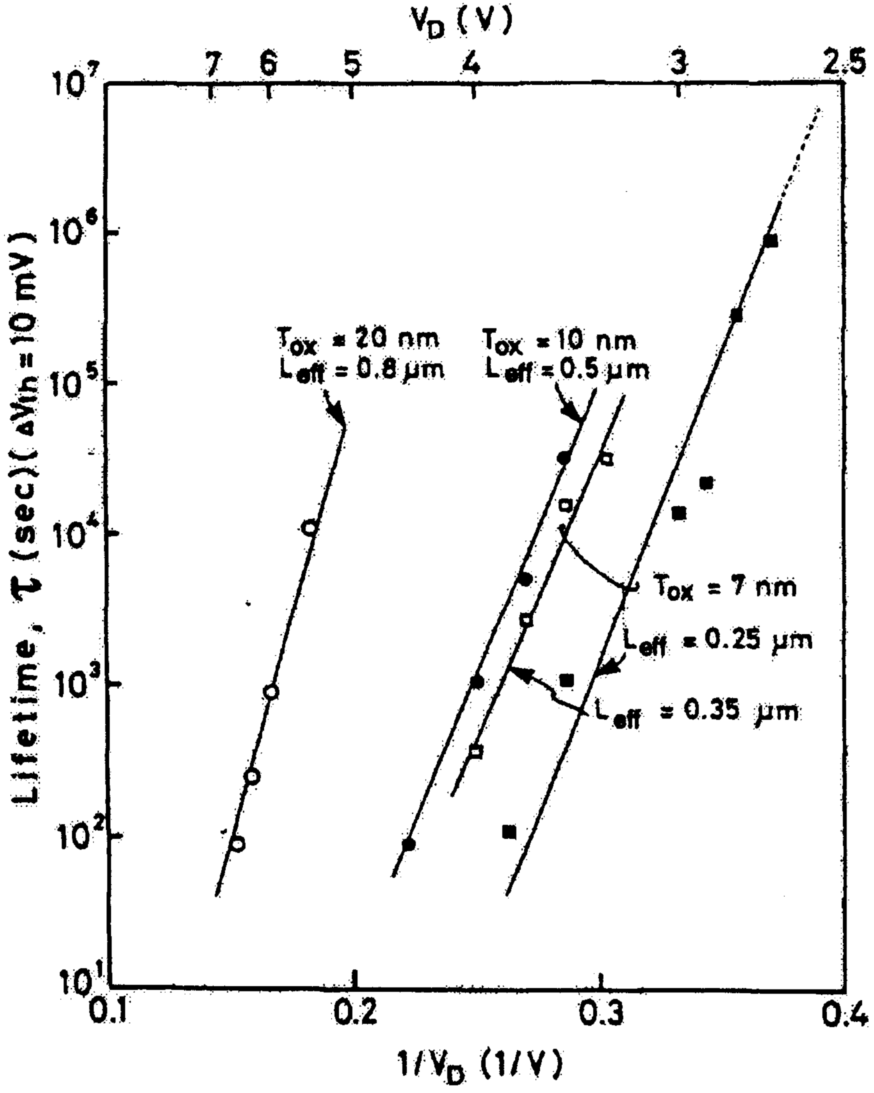
Abstract

Electrical failure mechanisms in commercial CMOS parts, including hot-carrier effects, gate-oxide breakdown, and electromigration were reviewed with particular emphasis on scaling with supply voltage. The effects of these mechanisms on lifetime are estimated and compared in a typical ASIC chip designed for 5.5-V operation. The improvement in lifetime by reduction of the supply voltage to 3.3 V is followed and a reliability design strategy based on minimizing early failures and maximizing the onset of late failures is derived. An outlook to reliability features of advanced low-power technologies, such as ultra-thin gate-oxides, silicon-on-insulator, and high-conductivity/low-permittivity interconnects concludes the presentation.

Hot-Carrier Lifetime vs. Drain Voltage for Different Technologies



Model:

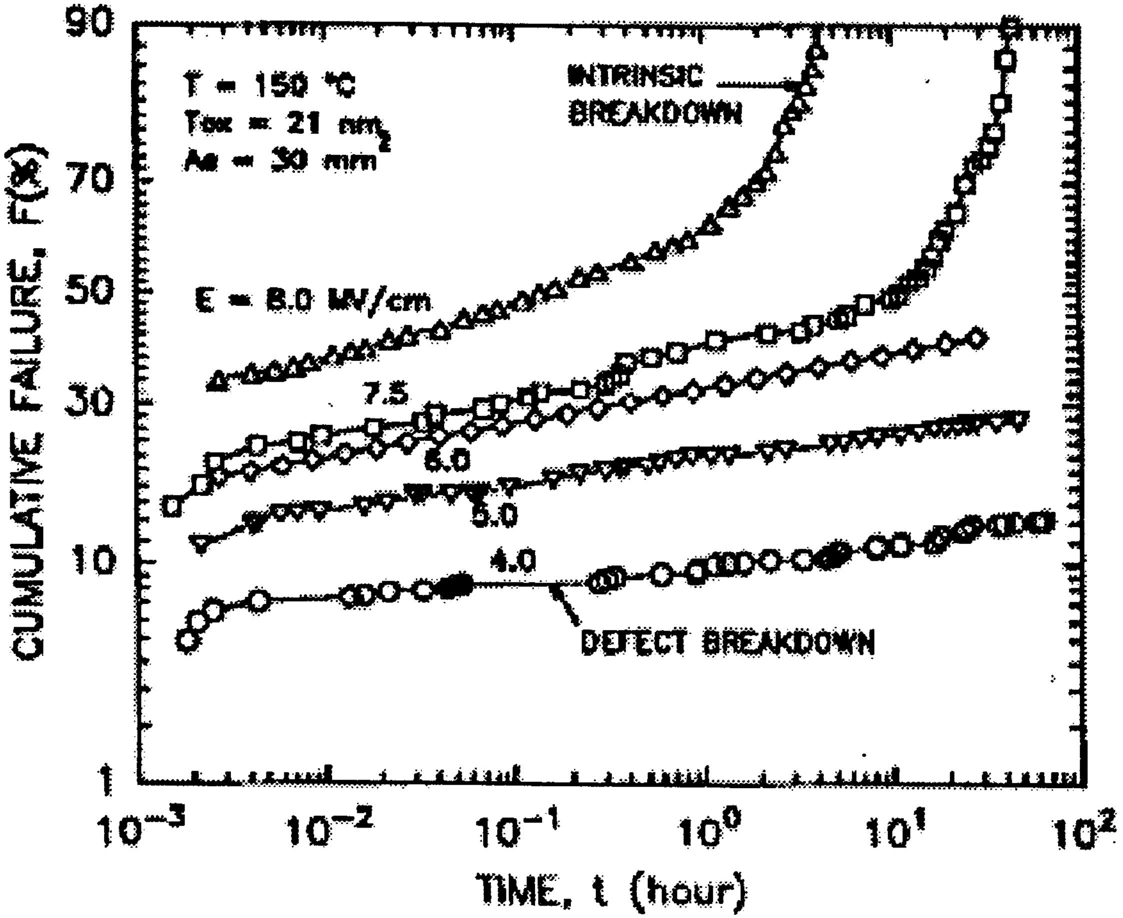
$$\tau = \tau_0 \exp\{ b / V_D \}$$

$b \approx$ 70 V ...100 V

Very strong dependence at least down to 2.5 V

[E. Takeda, C.Y. Yang, A. Miura-Hamada, "Hot-carrier effects in MOS devices", Academic Press, San Diego, 1995]

Gate-Oxide Failures F as Function of Stress at Different Electric Fields E



Model for time to early failures, caused by defects:

$t_F \propto \exp\{-B\,E\}$

with

$B = 91.6$ nm/V

or

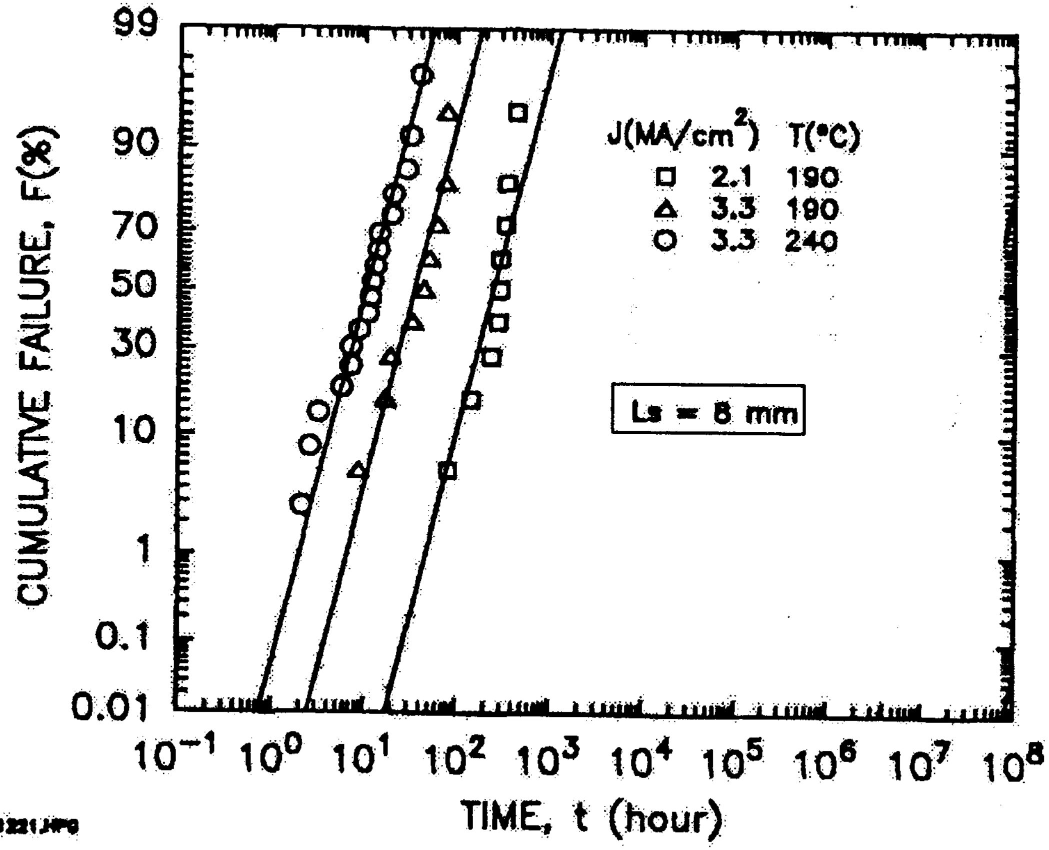
$t_F \propto \exp\{-V_{ox}/V_B\}$

with

$V_B = d/B = 0.229$ V

[K.C. Boyko and D. L. Gerlach, "Time dependent dielectric breakdown of 210 Angstrom oxides", IEEE IRPS, 1 (1989)]

Electromigration Failures F as Function of Stress at Different Current Densities J and Temperatures T



[M.G. Buehler, B.R. Blaes, G.A. Soli, N. Zamani, and K.A. Hicks, “Design and qualification of the SEU/TD radiation monitor chip”, JPL Publ. 92-18, p.15 (1992)]

Model [Mixed Black-McPherson] :

$$t_F \propto [1/j \sinh(\gamma j)] \times \exp\{(Q_0 - \gamma_1 j)/k_B T\}$$

with

$\gamma_1 \approx 0.038$ eV cm^2/MA

$Q_0 \approx 0.63$ eV

$\gamma \approx \gamma_1 / k_B T$

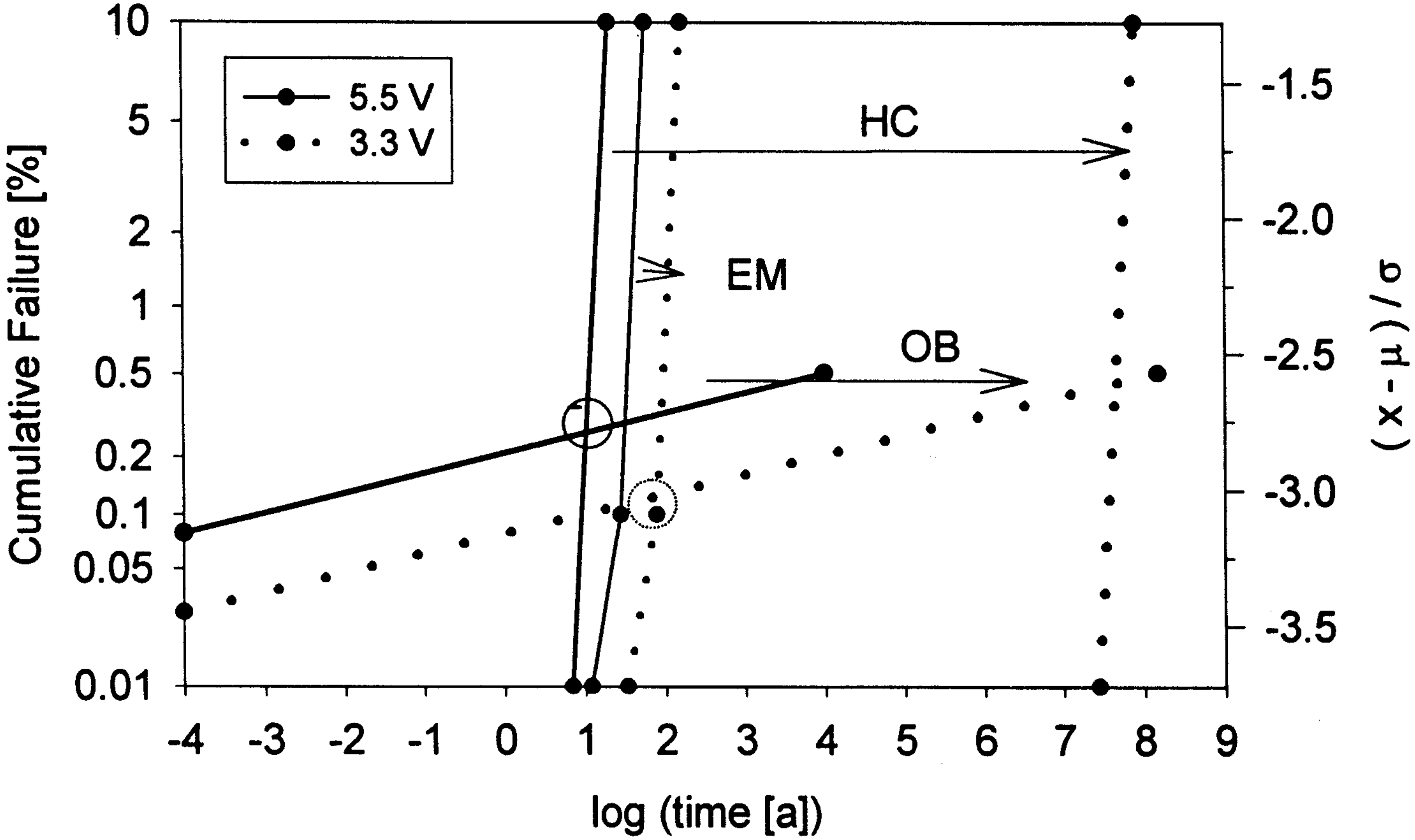
For $\gamma j \ll 1$:

$$t_F \propto [1/j^2]$$

Assumptions for a "Typical" CMOS ASIC Circuit

- Chip area 50 mm^2.
- Total oxide area $A_C = 3\ mm^2$.
- LDD-NMOSFETs with 1 μm gatelength and 17 nm oxide thickness.
- Metal lines Al-Si, width 2.4 μm, total length $L_C = 80$ mm.
- Added early EM failure mode, defect density 0.1/cm^2.

Yearly CMOS circuit failures by gate oxide breakdown (OB), hot carrier degradation (HC), and electromigration (EM) for V_{DD} = 5.5 V and 3.3 V



Conclusions

- Steep failure distributions, i.e., Hot Carrier Effects (HC) and Electromigration (EM), limit lifetime.
- Flat failure distribution, extrinsic Oxide Breakdown (OB), limits circuit failure probability.
- Limit values given by (circled) cross-over points, i.e.,
  - $V_{DD} = 5.5\,\mathrm{V}: \; F = 0.25\,\%, \; t_F = 10\,\mathrm{a}$
  - $V_{DD} = 3.3\,\mathrm{V}: \; F = 0.1\,\%, \; t_F = 80\,\mathrm{a}$
- Reduction of supply voltage from 5.5 V to 3.3 V :
  - reduces HC lifetime by orders of magnitude
  - reduces EM lifetime only quadratically with voltage ratio
  - reduces OB failure probability from 0.25 % to 0.1 % .
- Assumed extrinsic EM failures of no consequence.

Outlook: New Low-Power Technologies

- Thinner oxides (5-7 nm)
  - Degrade in the form of threshold voltage shift and leakage current before breakdown.
- Ultrathin oxides (< 3 nm)
  - "Soft" breakdown in many steps with a lasting increase of flicker noise.
- Cu-Interconnect Metal
  - Quality of interface with passivation critical for electromigration behavior.
- Low-Permittivity Dielectrics
  - Properties to watch:
    - electrical leakage and/or breakdown, thermal and chemical stability, thermal conductance.
  - Results for silsesquioxane:
    - 10 x leakage of SiO_2, breakdown > 100 V, thermally stable, thermal conductance decreased by 25 %, interlevel capacitance decreased by 30 %.
- Hot-Carrier effects may decrease faster than $1/V_{DD}$ below $V_{DD} = 2.5$ V.