Comparison of Electrical Failure Mechanisms in COTS Parts and Their Scaling with Supply Voltage – An Overview

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Abstract

Electrical failure mechanisms in commercial CMOS parts, including hot-carrier effects, gate-oxide breakdown, and electromigration were reviewed with particular emphasis on scaling with supply voltage. The effects of these mechanisms on lifetime are estimated and compared in a typical ASIC chip designed for 5.5-V operation. The improvement in lifetime by reduction of the supply voltage to 3.3 V is followed and a reliability design strategy based on minimizing early failures and maximizing the onset of late failures is derived. An outlook to reliability features of advanced low-power technologies, such as ultra-thin gate-oxides, silicon-on-insulator, and high-conductivity/low-permittivity interconnects concludes the presentation.
Hot-Carrier Lifetime vs. Drain Voltage for Different Technologies

Model:

\[ \tau = \tau_0 \exp\left\{ \frac{b}{V_D} \right\} \]

\[ b \approx 70 \text{ V} \ldots 100 \text{ V} \]

Very strong dependence at least down to 2.5 V

Gate-Oxide Failures $F$ as Function of Stress at Different Electric Fields $E$

Model for time to early failures, caused by defects:

$$t_F \propto \exp\{-B \cdot E\}$$

with

$$B = 91.6 \text{ nm/V}$$

or

$$t_F \propto \exp\{-V_{ox}/V_B\}$$

with

$$V_B = d/B = 0.229 \text{ V}$$

Electromigration Failures $F$ as Function of Stress at Different Current Densities $J$ and Temperatures $T$

Model [Mixed Black-McPherson]:

$$t_F \propto \left[1/j \sinh(\gamma j)\right] \times \exp\left\{\left(\frac{Q_0 - \gamma_1 j}{k_B T}\right)\right\}$$

with

- $\gamma_1 \approx 0.038$ eV cm$^2$/MA
- $Q_0 \approx 0.63$ eV
- $\gamma \approx \gamma_1/k_B T$

For $\gamma j \ll 1$:

$$t_F \propto \left[1/j^2\right]$$

Assumptions for a "Typical" CMOS ASIC Circuit

- Chip area 50 mm².
- Total oxide area \( A_C = 3 \text{ mm}^2 \).
- LDD-NMOSFETs with 1 \( \mu \text{m} \) gate length and 17 nm oxide thickness.
- Metal lines Al-Si, width 2.4 \( \mu \text{m} \), total length \( L_C = 80 \text{ mm} \).
- Added early EM failure mode, defect density 0.1/cm².
Yearly CMOS circuit failures by gate oxide breakdown (OB), hot carrier degradation (HC), and electromigration (EM) for $V_{DD} = 5.5\, \text{V}$ and $3.3\, \text{V}$
Conclusions

- Steep failure distributions, i.e., Hot Carrier Effects (HC) and Electromigration (EM), limit lifetime.
- Flat failure distribution, extrinsic Oxide Breakdown (OB), limits circuit failure probability.
- Limit values given by (circled) cross-over points, i.e.,
  - $V_{DD} = 5.5 \text{ V}$ : $F = 0.25 \%$, $t_F = 10 \text{ a}$
  - $V_{DD} = 3.3 \text{ V}$ : $F = 0.1 \%$, $t_F = 80 \text{ a}$
- Reduction of supply voltage from 5.5 V to 3.3 V :
  - reduces HC lifetime by orders of magnitude
  - reduces EM lifetime only quadratically with voltage ratio
  - reduces OB failure probability from 0.25 % to 0.1 %.
- Assumed extrinsic EM failures of no consequence.
Outlook: New Low-Power Technologies

- Thinner oxides (5-7 nm)
  - Degrade in the form of threshold voltage shift and leakage current before breakdown.

- Ultrathin oxides (< 3 nm)
  - "Soft" breakdown in many steps with a lasting increase of flicker noise.

- Cu-Interconnect Metal
  - Quality of interface with passivation critical for electromigration behavior.

- Low-Permittivity Dielectrics
  - Properties to watch:
    - electrical leakage and/or breakdown, thermal and chemical stability, thermal conductance.
  - Results for silsesquioxane:
    - $10 \times$ leakage of SiO$_2$, breakdown > 100 V, thermally stable, thermal conductance decreased by 25\%, interlevel capacitance decreased by 30\%.

- Hot-Carrier effects may decrease faster than $1/V_{DD}$ below $V_{DD} = 2.5$ V.