Simulator Development for Nanoelectronic Devices

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The NASA/JPL goal to reduce payload in future space missions while increasing mission capability demands miniaturization of active and passive sensors, analytical instruments and communication systems among others. Currently, typical system requirements include the detection of particular spectral lines, associated data processing, and communication of the acquired data to other systems. Similar goals are presently imposed on military and industry technology developments. While silicon device technology dominates the microprocessor and memory market, III-V heterostructure devices maintain their niche for light detection, light emission, and high-speed data transmission. The design and optimization of devices such as heterostructure field effect transistors (HFETs), resonant tunneling diodes (RTDs), quantum well infrared photodetectors (QWIPs), and quantum well lasers requires a detailed understanding of material properties, their influence on electron transport, and the device coupling to the surrounding electromagnetic field. Heterostructure device designs involve layering different materials and doping profiles on an atomic scale. The variety of available material systems, material compositions and layer configurations is staggering. The goal of simulation of such devices and systems is to focus and limit the number of experiments needed. This reduces cost and time to product and enables incremental optimization as well as revolutionary creation of devices. We will provide an overview of the capabilities of the High Performance Computing Group in the areas of electromagnetic and nanoelectronic modeling, optimization with genetic algorithms, and simulator development. In particular we will focus on the continued development of the Nanoelectronic Modeling Tool (NEMO) and its application to RTDs. Finally we will present our vision on heterostructure device modeling in 2D and 3D models including the interactions with light and time dependent fields.