EB: Numerical Analysis in EMC problems (I)

Modeling ESD Events in Low Earth Orbit Satellites

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Introduction

Over the last two years several satellites in Low Earth Orbit (LEO) and geosynchronous orbit (GEO) have experienced serious or catastrophic failures. In preliminary analyses it has been shown that severe electrostatic discharges from spacecraft dielectric surfaces (e.g solar arrays and thermal blankets) can sustain high discharge currents capable of disabling key avionics components posing a threat to satellite survivability.

Short Summary

Surface charging of spacecraft surfaces in LEO and GEO orbit environments is caused primarily by electrons with energies oscillating between 1 and 50 KeV, specially during magnetospheric substorms. In this type of charging strong electric fields develop. When the electric fields exceed critical values electrostatic discharges (ESD) can cause not only EMI but can pose potential threats to spacecraft hardware.

When an ESD event occurs, charge is blown off from the dielectric surface which induces a replacement current to flow in the satellite structure. A rapid surface potential change induces noise in circuits through capacitive coupling. The objective is to estimate the current distribution and generated fields along complex conductive paths as shown for example in Figure 1 for the discharge event between a solar array and shielded wires connecting the solar array cells and a charge control unit inside the spacecraft. The method of moments is used to analyze the current distribution paths.

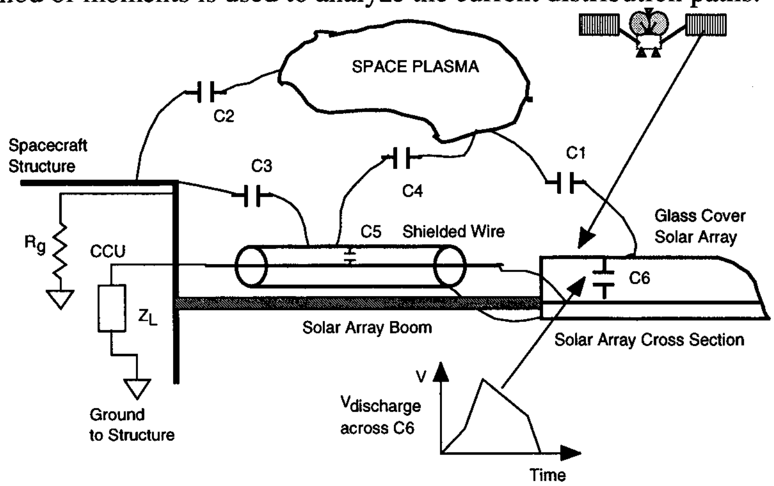

Figure 1. Modeling ESD Events Between a Solar Array and Cable.

References:
[1] Wilson, P.F. "Fields radiated by electroststatic discharges," IEEE Trans. on Electromagnetic Compatibility, Vol. 33, Feb. 1991.

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OUTLINE

1) Illustration of the ESD Problem in Satellites

2) Explaining the Problem of ESD Events

3) Methods for Modeling ESD Events

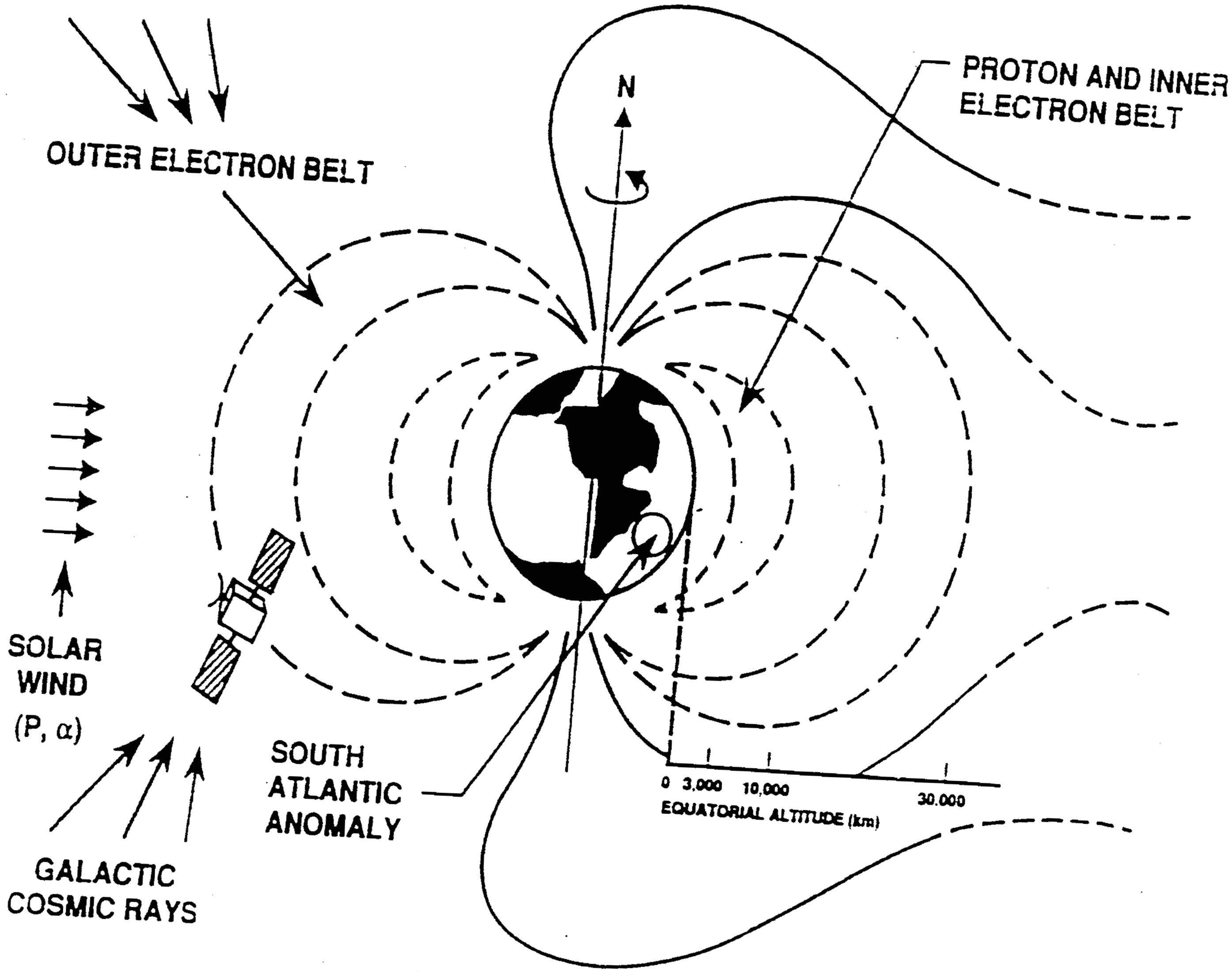
4) The usage of computational tools for modeling the ESD events.

5) Conclusions

Illustration of the ESD Problem in Satellites

JPL

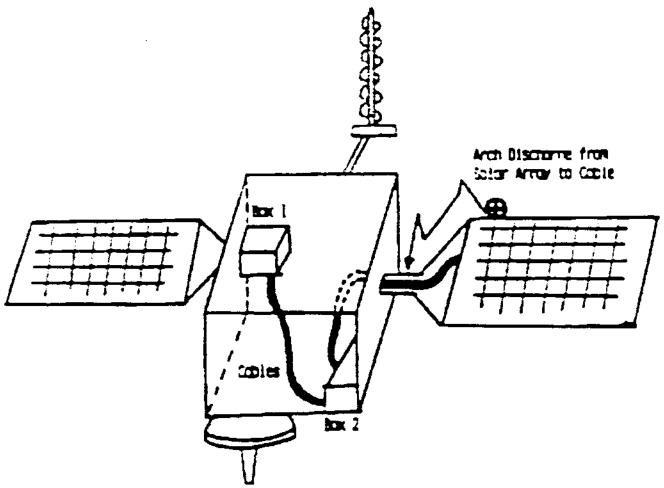
Earth's Van Allen Radiation Belts

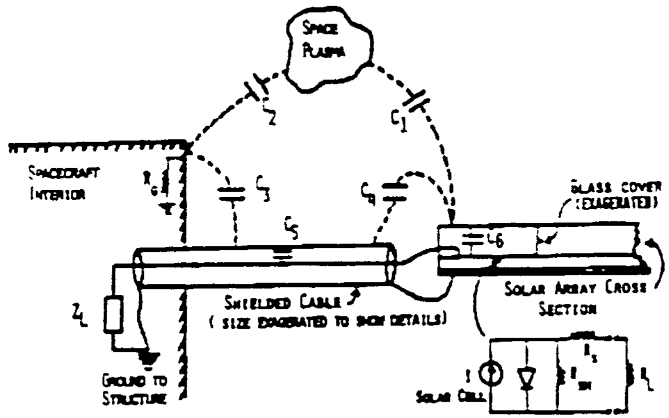


Explaining the Problem of ESD Events

ESD Effects on Satellites

Simply stated: Electroststic discharge events in satellites can disable a satellite.





Methods for Modeling ESD Events

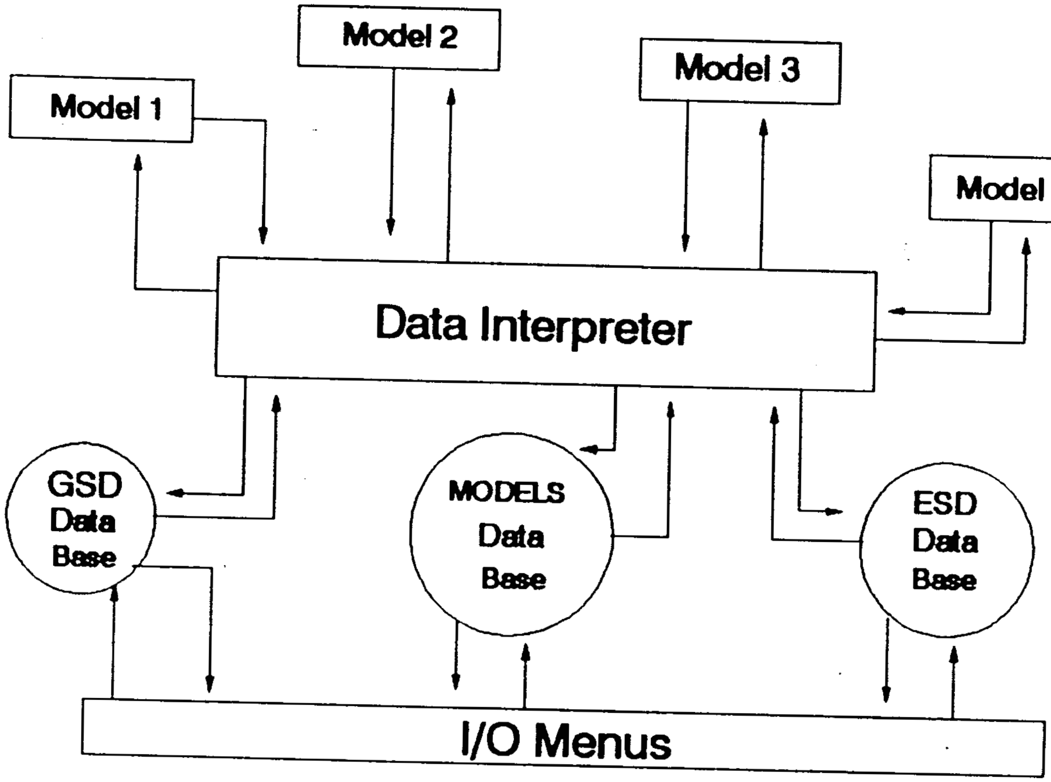
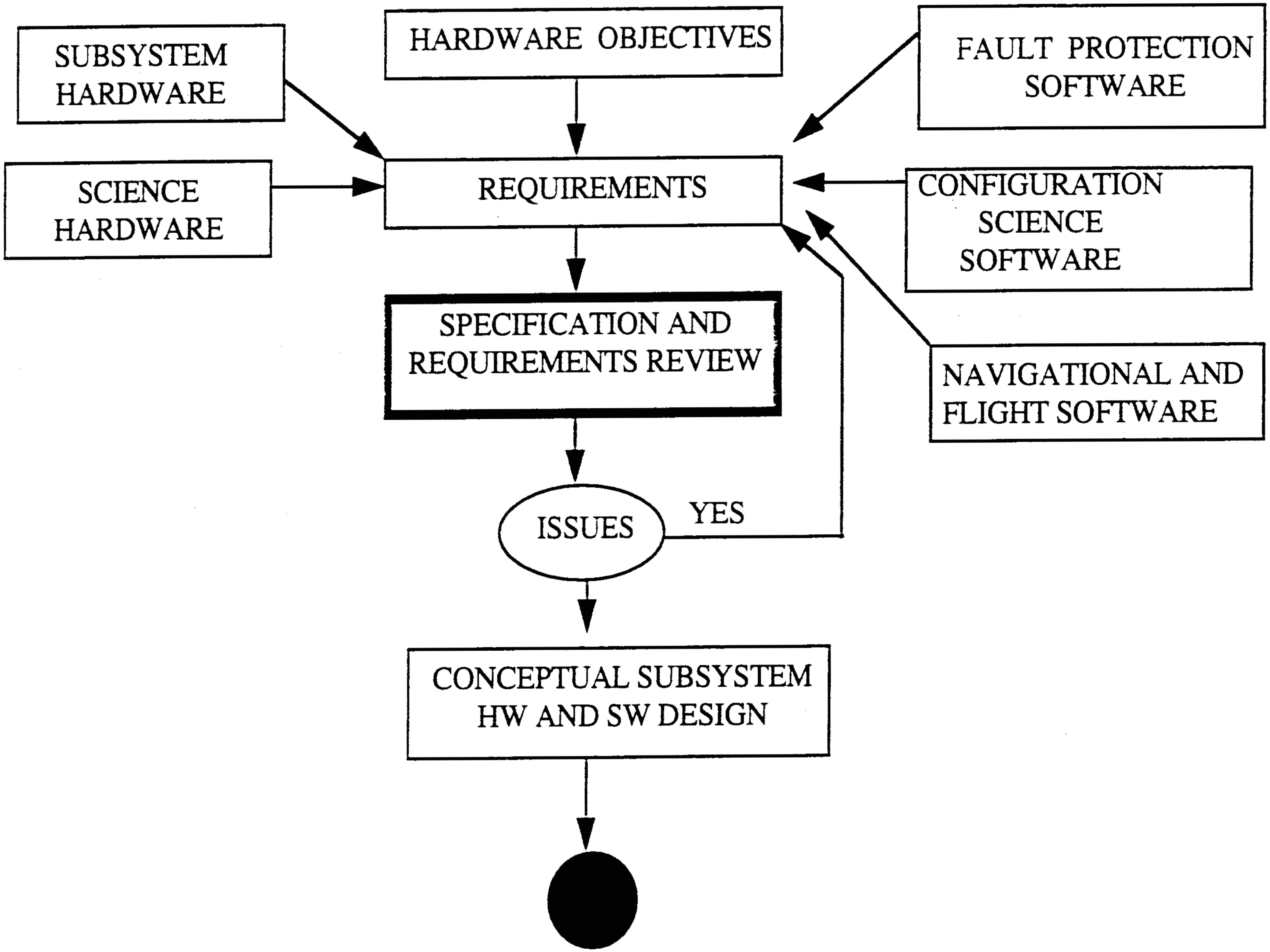
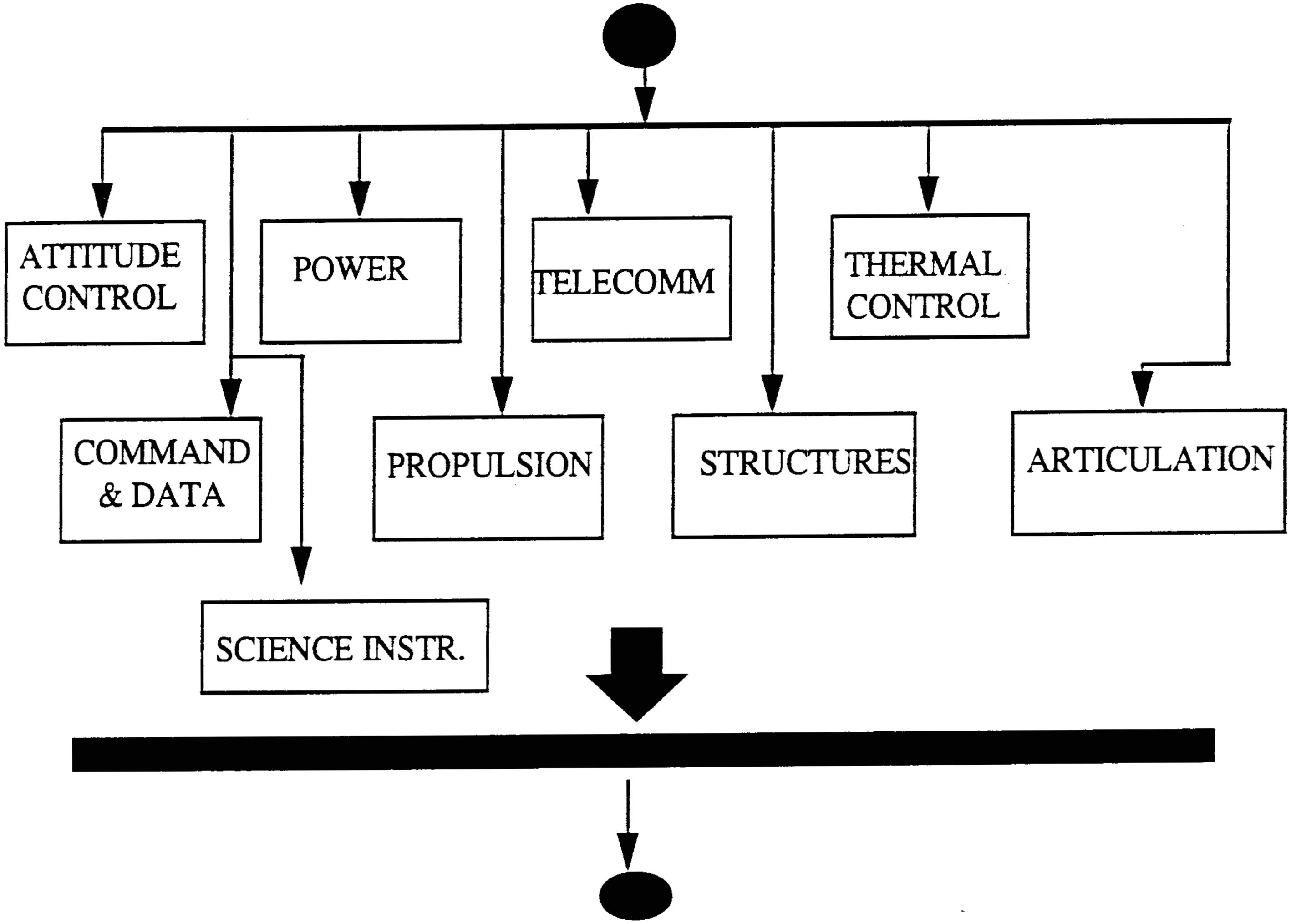
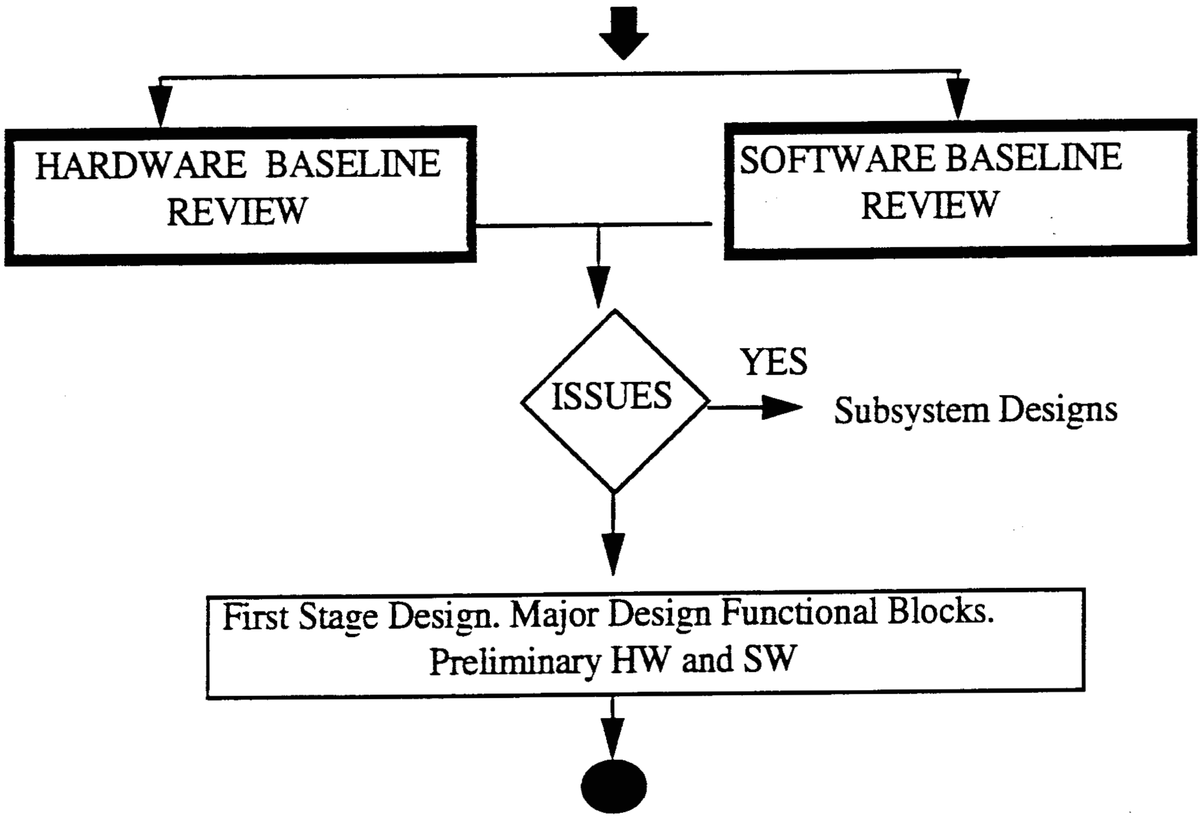


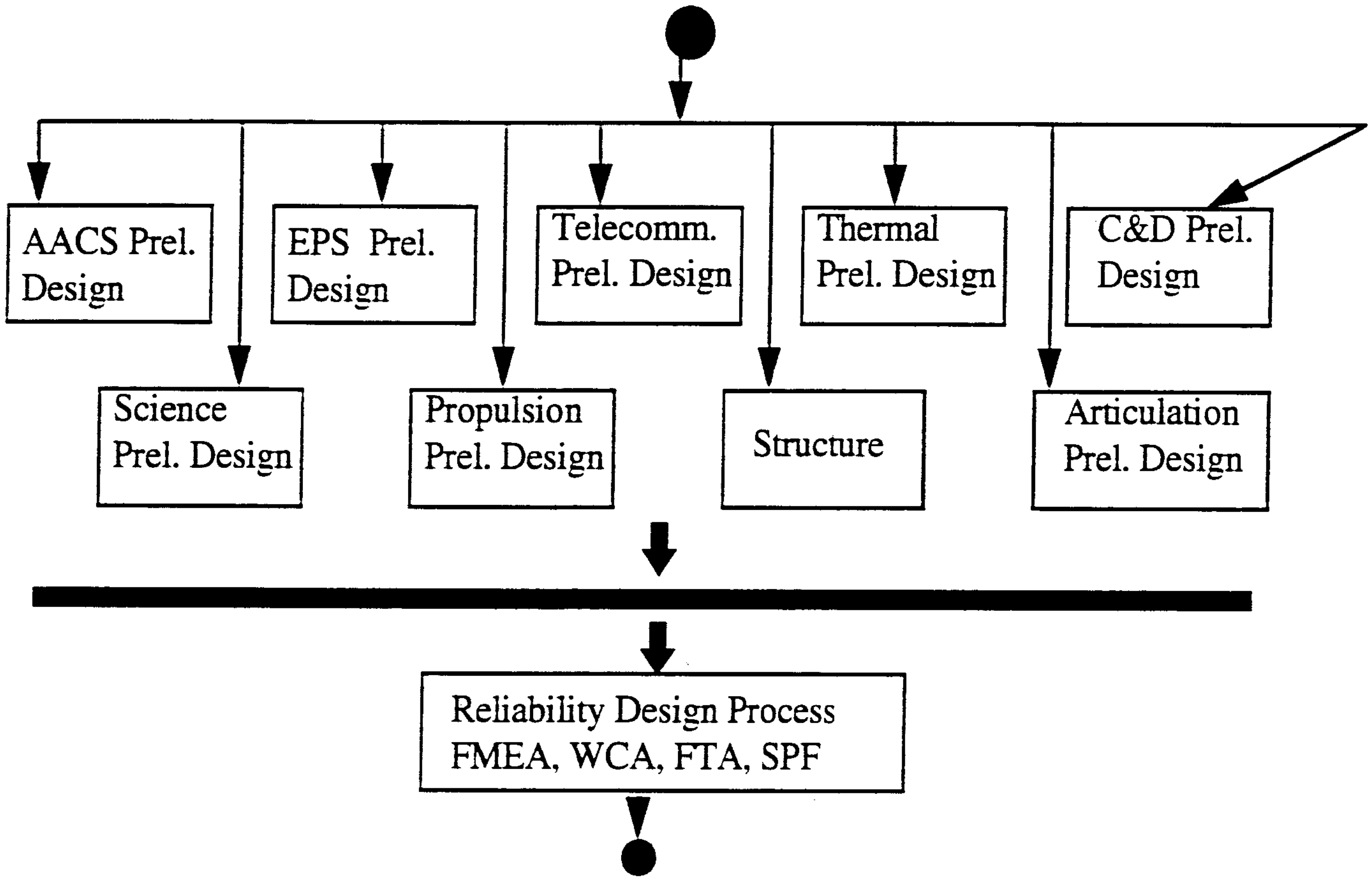
FIGURE 1. EMCWB BLOCK DIAGRAM

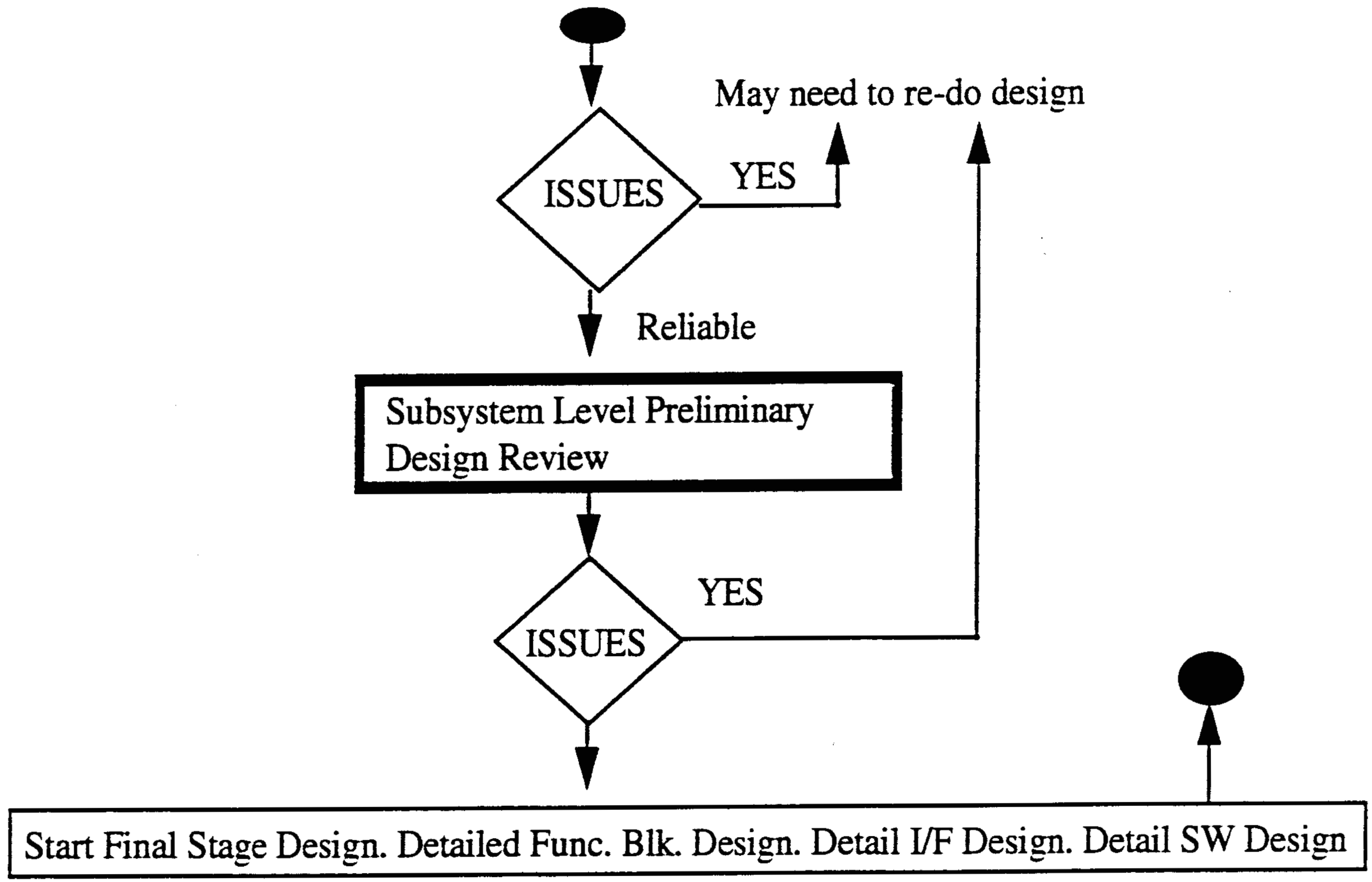
ELECTRONIC HARDWARE DESIGN CYCLE

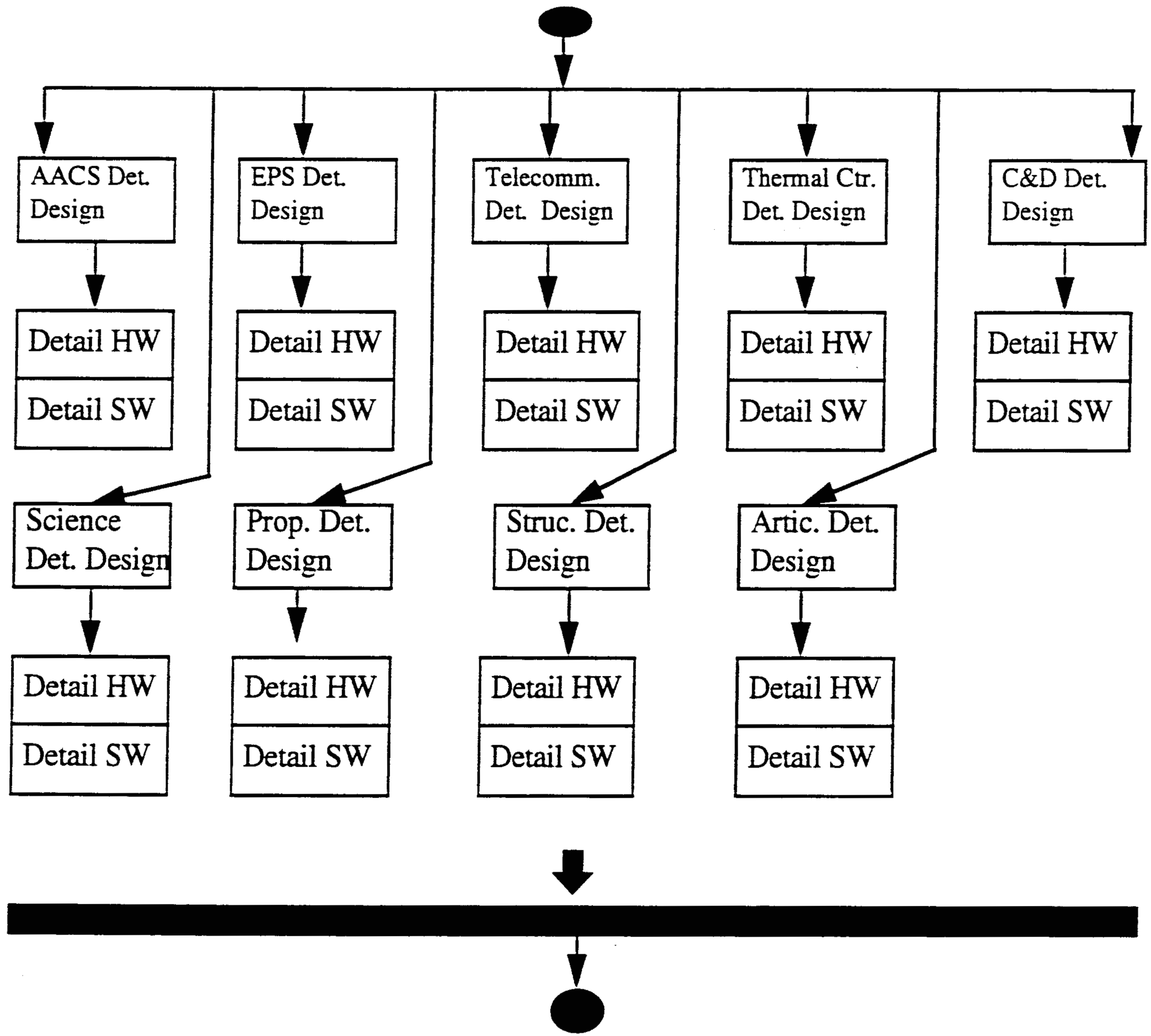


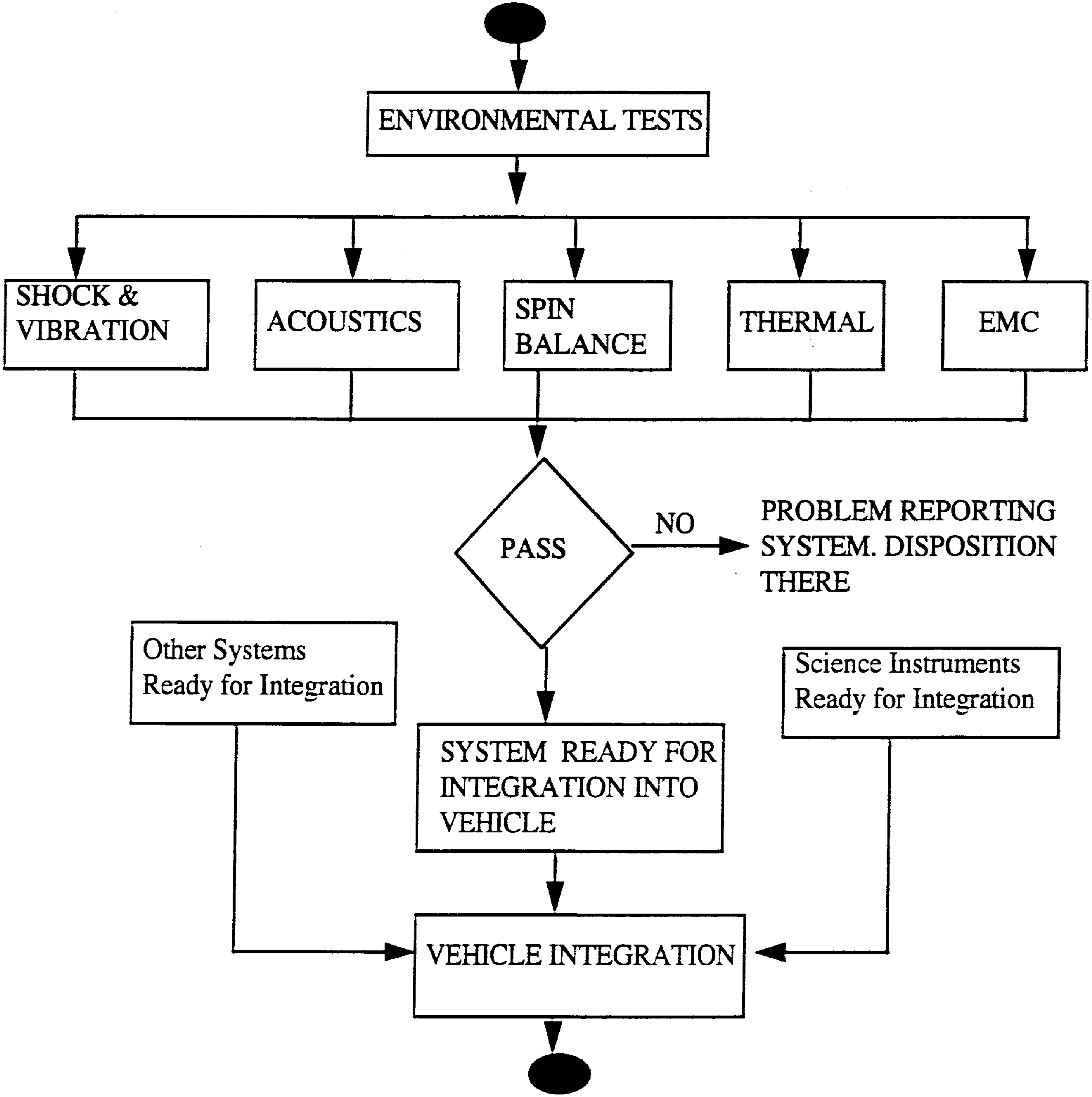

ATTITUDE CONTROL
POWER
TELECOMM
THERMAL CONTROL
COMMAND & DATA
PROPULSION
STRUCTURES
ARTICULATION
SCIENCE INSTR.

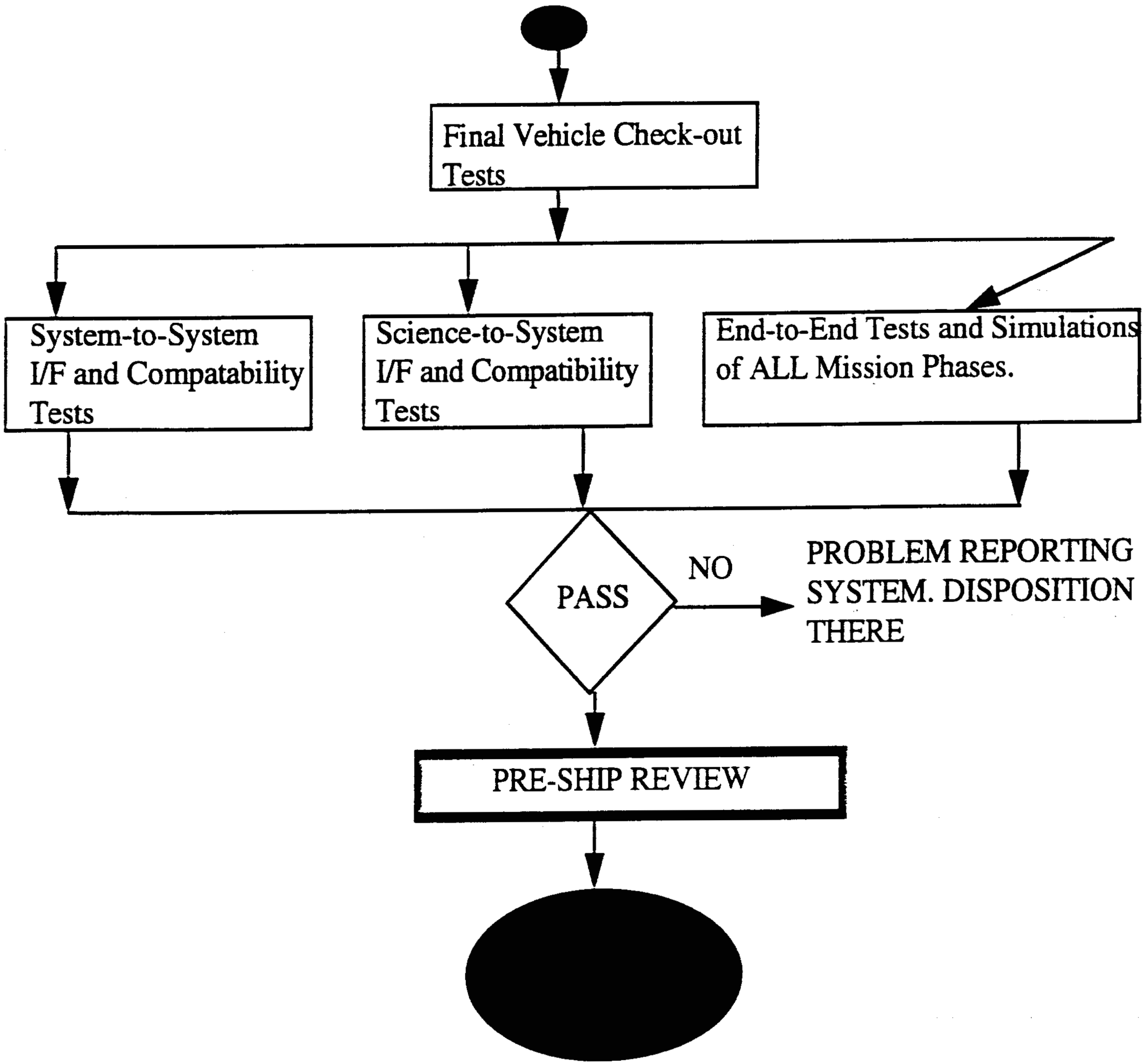

HARDWARE BASELINE REVIEW
SOFTWARE BASELINE REVIEW
ISSUES
YES
Subsystem Designs
First Stage Design. Major Design Functional Blocks.
Preliminary HW and SW

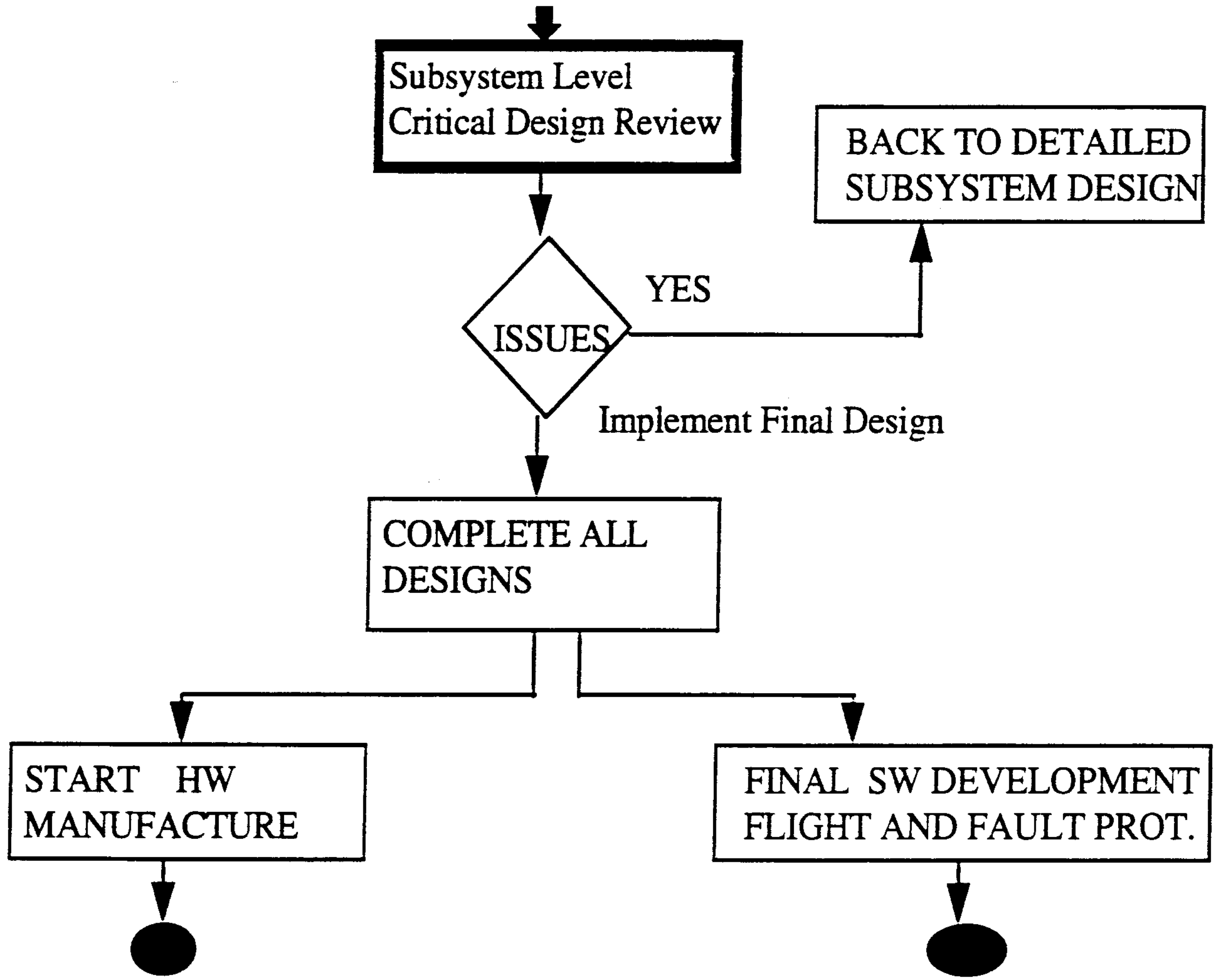

AACS Prel. Design
Science Prel. Design
EPS Prel. Design
Propulsion Prel. Design
Telecomm. Prel. Design
Structure
Thermal Prel. Design
Articulation Prel. Design
C&D Prel. Design
Reliability Design Process
FMEA, WCA, FTA, SPF


May need to re-do design
YES
ISSUES
Reliable
Subsystem Level Preliminary Design Review
YES
ISSUES
Start Final Stage Design. Detailed Func. Blk. Design. Detail I/F Design. Detail SW Design

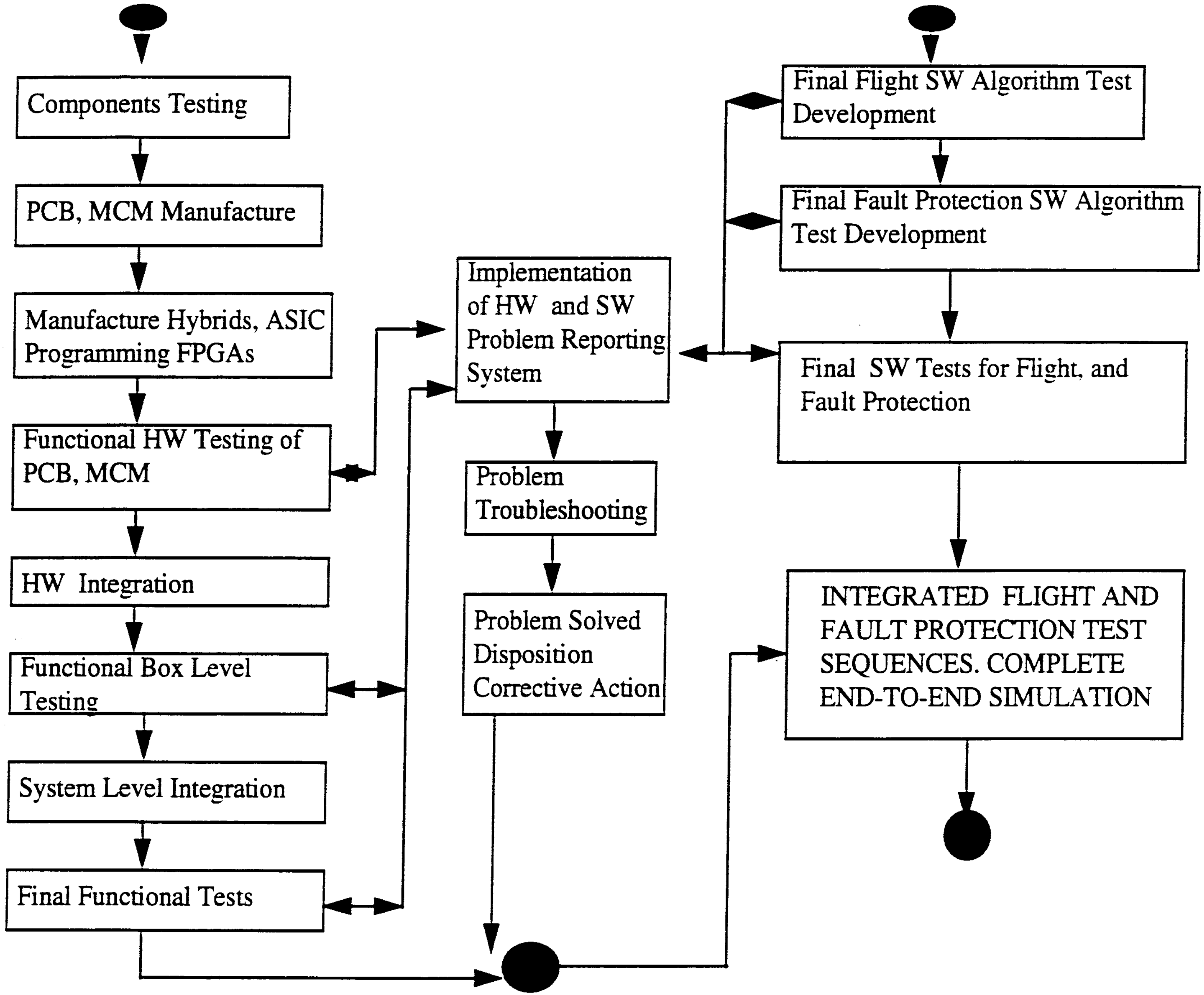

AACS Det. Design
Detail HW
Detail SW
EPS Det. Design
Detail HW
Detail SW
Telecomm. Det. Design
Detail HW
Detail SW
Thermal Ctr. Det. Design
Detail HW
Detail SW
C&D Det. Design
Detail HW
Detail SW
Science Det. Design
Detail HW
Detail SW
Prop. Det. Design
Detail HW
Detail SW
Struc. Det. Design
Detail HW
Detail SW
Artic. Det. Design
Detail HW
Detail SW


ENVIRONMENTAL TESTS
SHOCK & VIBRATION
ACOUSTICS
SPIN BALANCE
THERMAL
EMC
PASS
NO
PROBLEM REPORTING SYSTEM. DISPOSITION THERE
Other Systems Ready for Integration
Science Instruments Ready for Integration
SYSTEM READY FOR INTEGRATION INTO VEHICLE
VEHICLE INTEGRATION

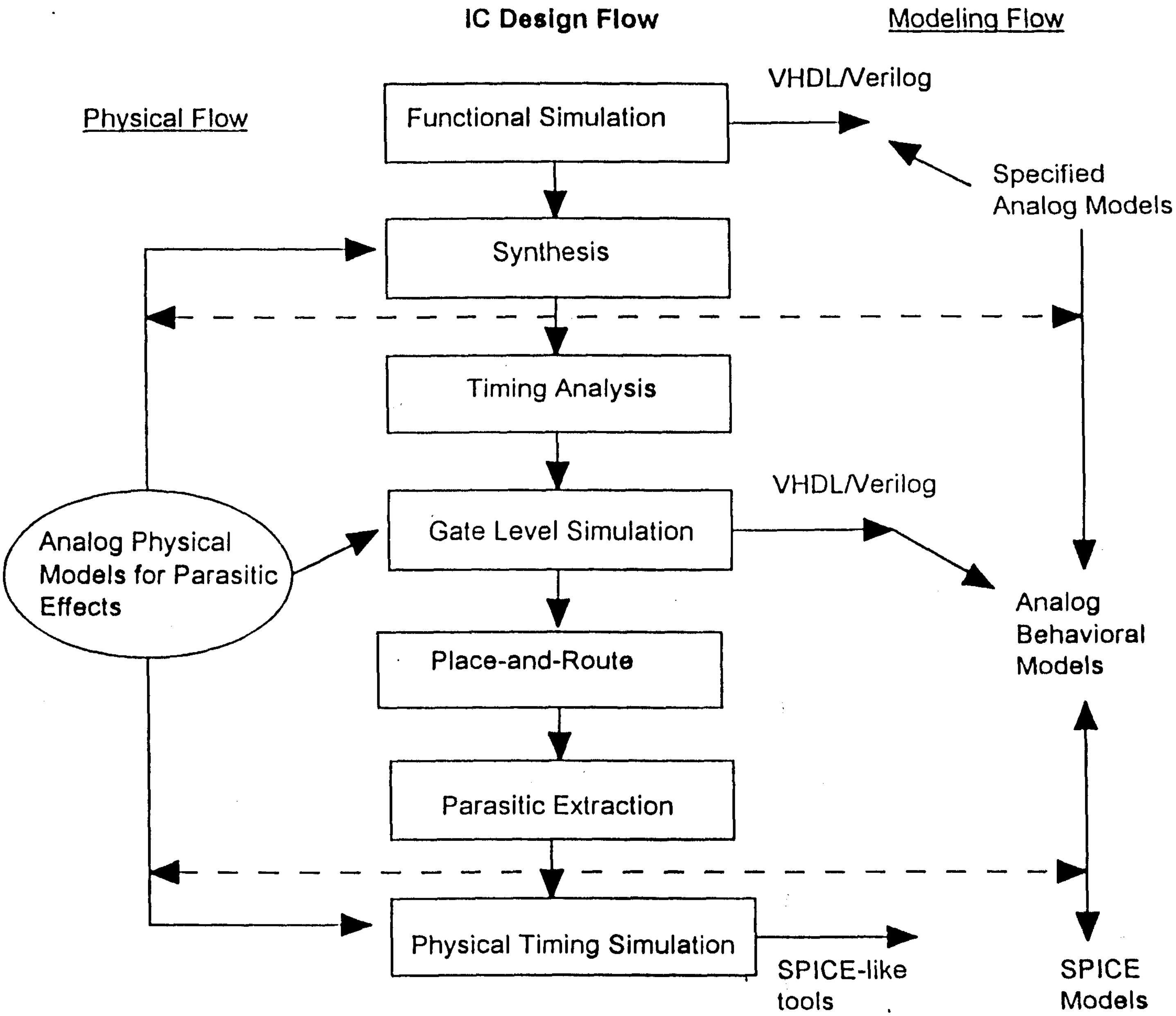

Final Vehicle Check-out Tests
System-to-System I/F and Compatability Tests
Science-to-System I/F and Compatibility Tests
End-to-End Tests and Simulations of ALL Mission Phases.
PASS
NO
PROBLEM REPORTING SYSTEM. DISPOSITION THERE
PRE-SHIP REVIEW



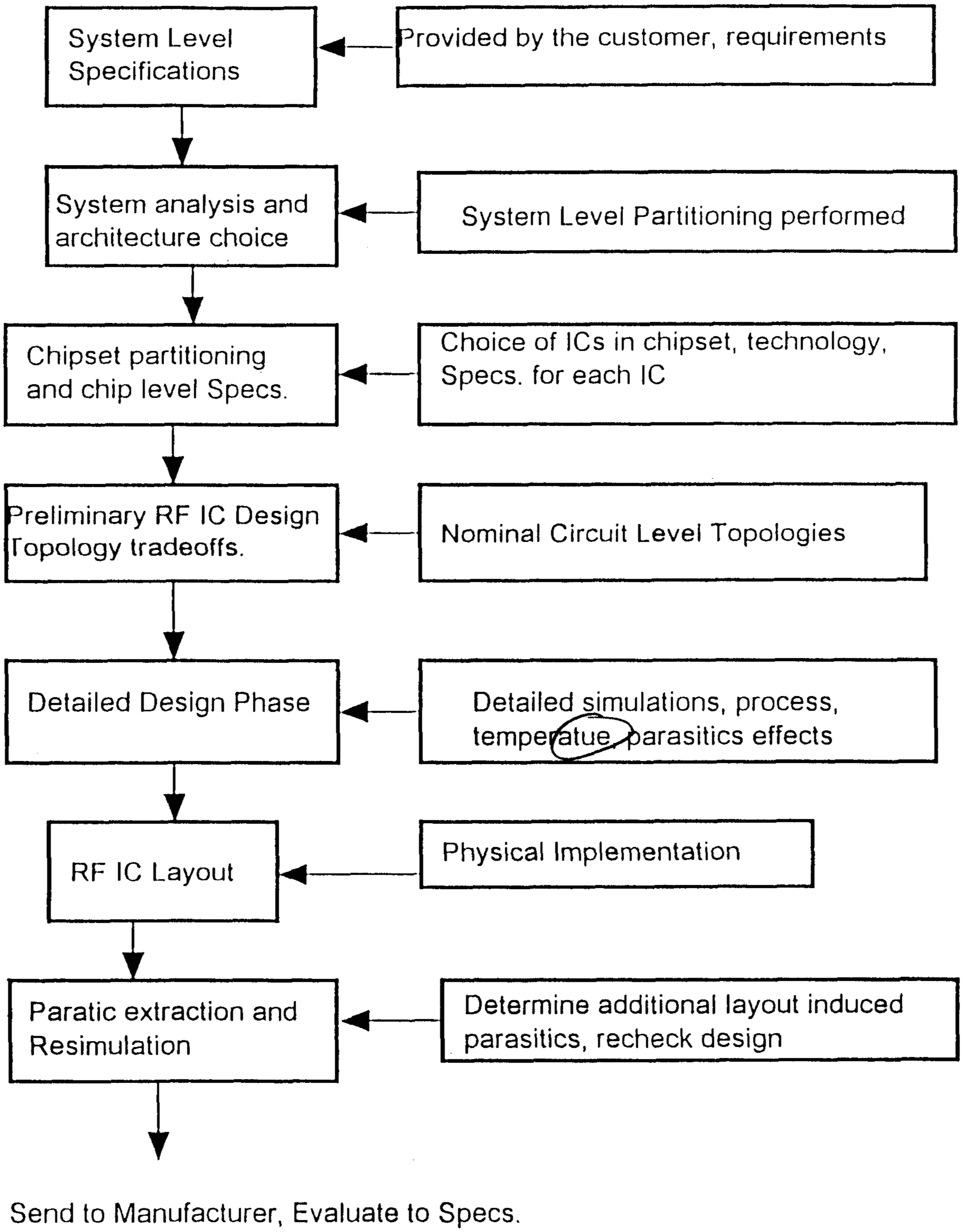
Subsystem Level
Critical Design Review
ISSUES
YES
BACK TO DETAILED
SUBSYSTEM DESIGN
Implement Final Design
COMPLETE ALL
DESIGNS
START HW
MANUFACTURE
FINAL SW DEVELOPMENT
FLIGHT AND FAULT PROT.


Components Testing
PCB, MCM Manufacture
Manufacture Hybrids, ASIC Programming FPGAs
Functional HW Testing of PCB, MCM
HW Integration
Functional Box Level Testing
System Level Integration
Final Functional Tests
Implementation of HW and SW Problem Reporting System
Problem Troubleshooting
Problem Solved Disposition Corrective Action
Final Flight SW Algorithm Test Development
Final Fault Protection SW Algorithm Test Development
Final SW Tests for Flight, and Fault Protection
INTEGRATED FLIGHT AND FAULT PROTECTION TEST SEQUENCES. COMPLETE END-TO-END SIMULATION

The usage of computational tools for modeling the ESD events



DIGITAL ASIC OR HYBRID DESIGN



TYPICAL RF ASIC DESIGN FLOW

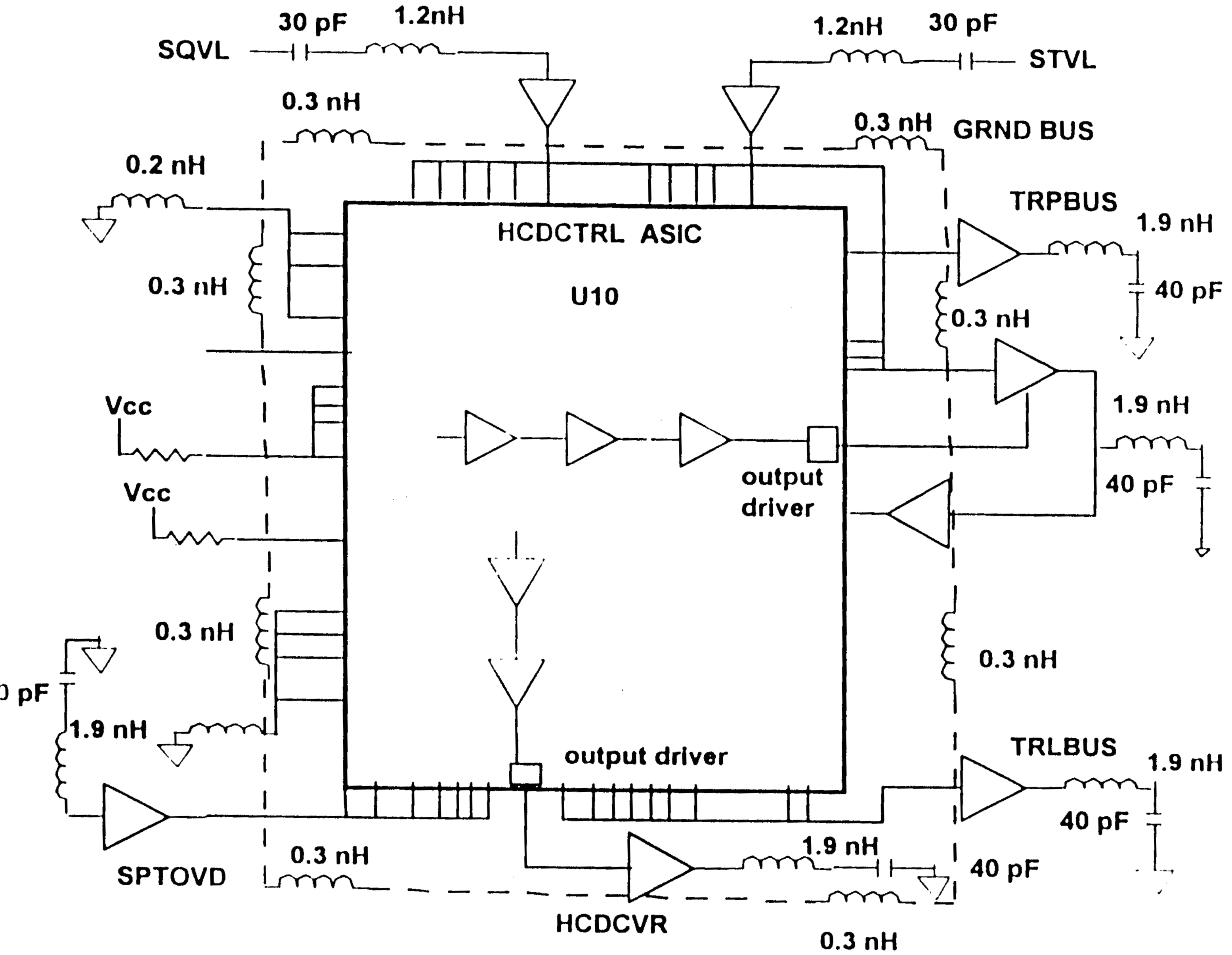


FIGURE 3. ASIC OVERVIEW OF ITS OUTPUTS LOSSES AND GROUND CONNECTION

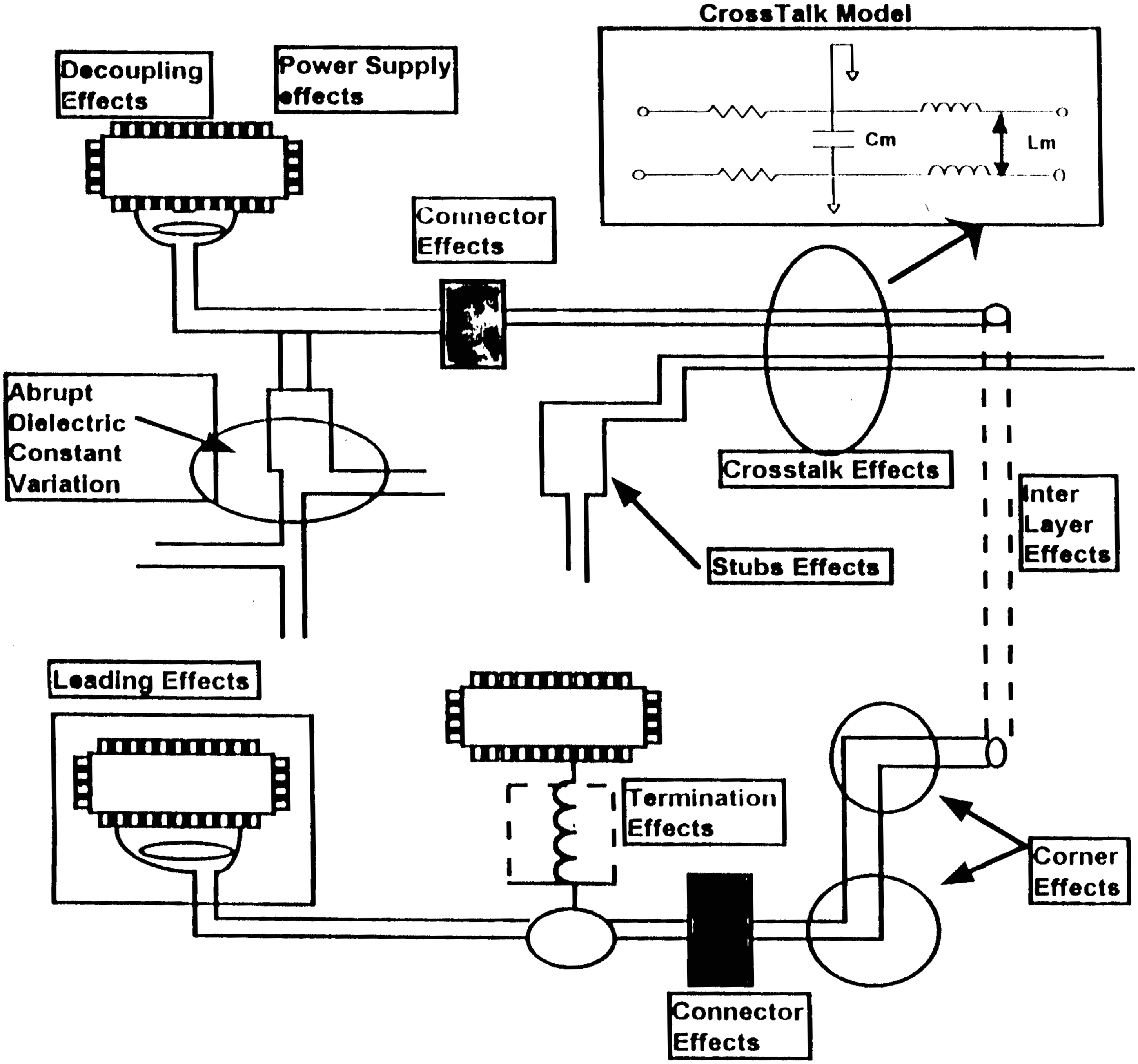


FIGURE 1. THE COMPLEXITIES OF INTERCONNECTS IN A PCB.

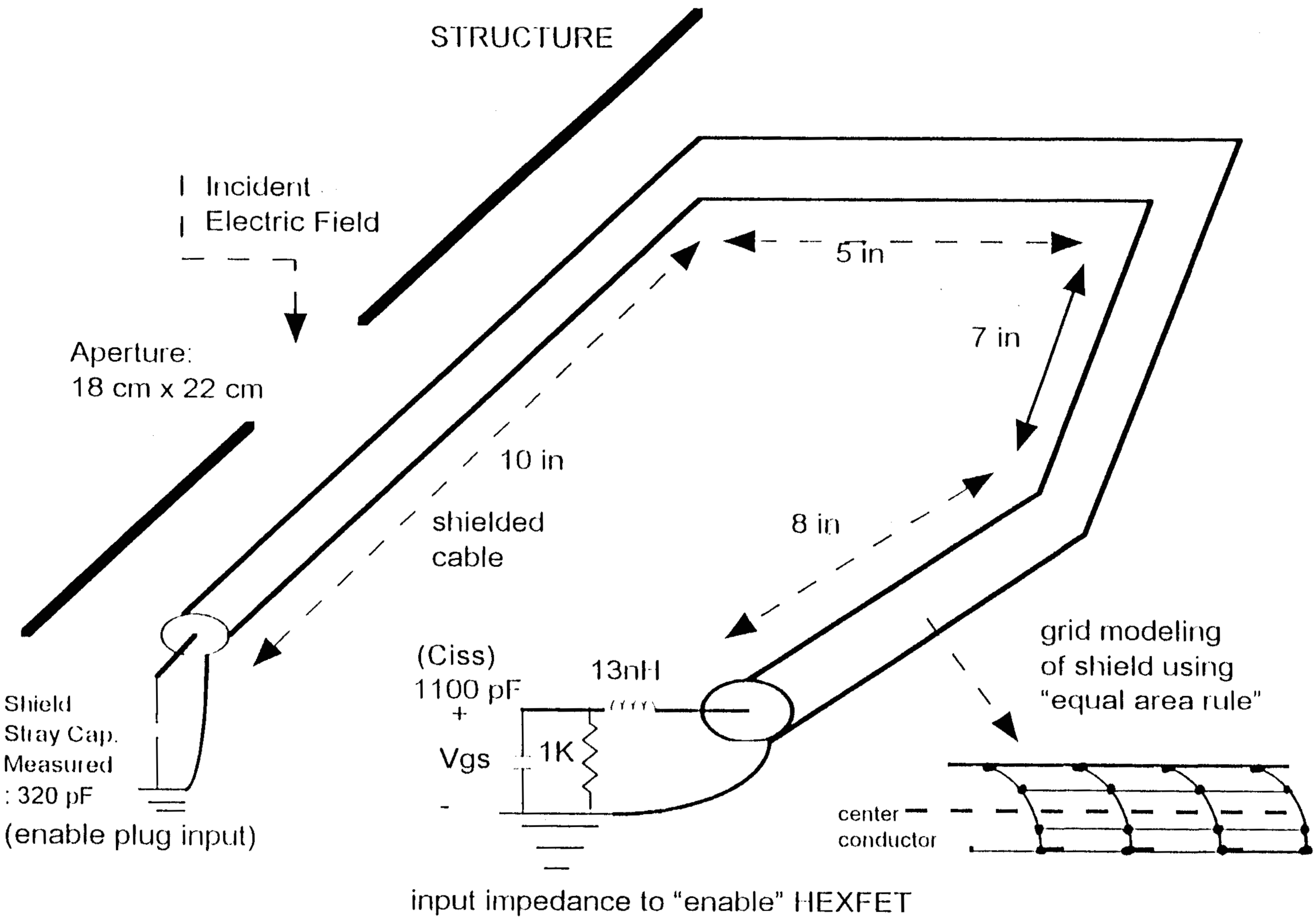
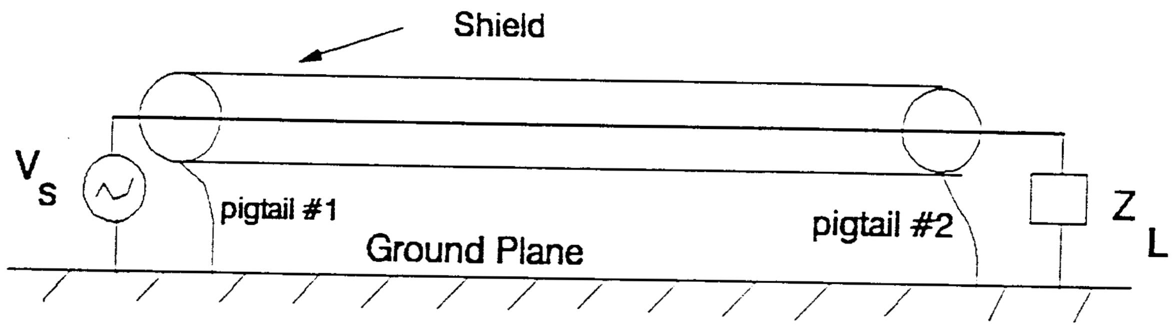
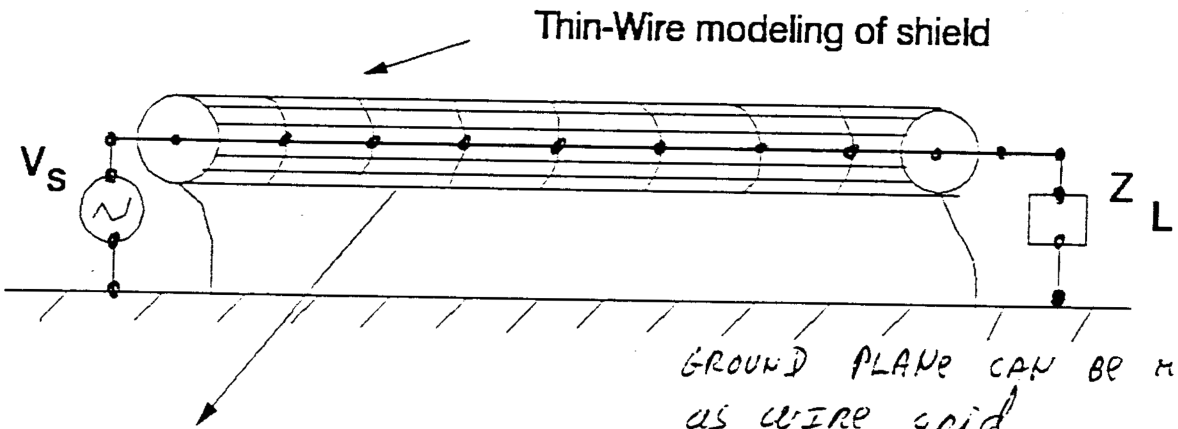


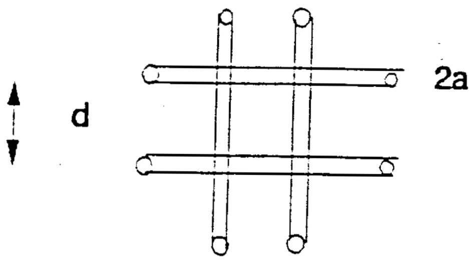
Figure 7. Method of Moments Modeling of Shielded Cable with Loads

RADIATION FROM A SHIELDED CABLE





GROUND PLANE CAN BE modeled as WIRE grid



$d = 2\pi a$ "Equal area rule"

segment length = L/10

Figure 4. Modeling a Shield for Method of Moments

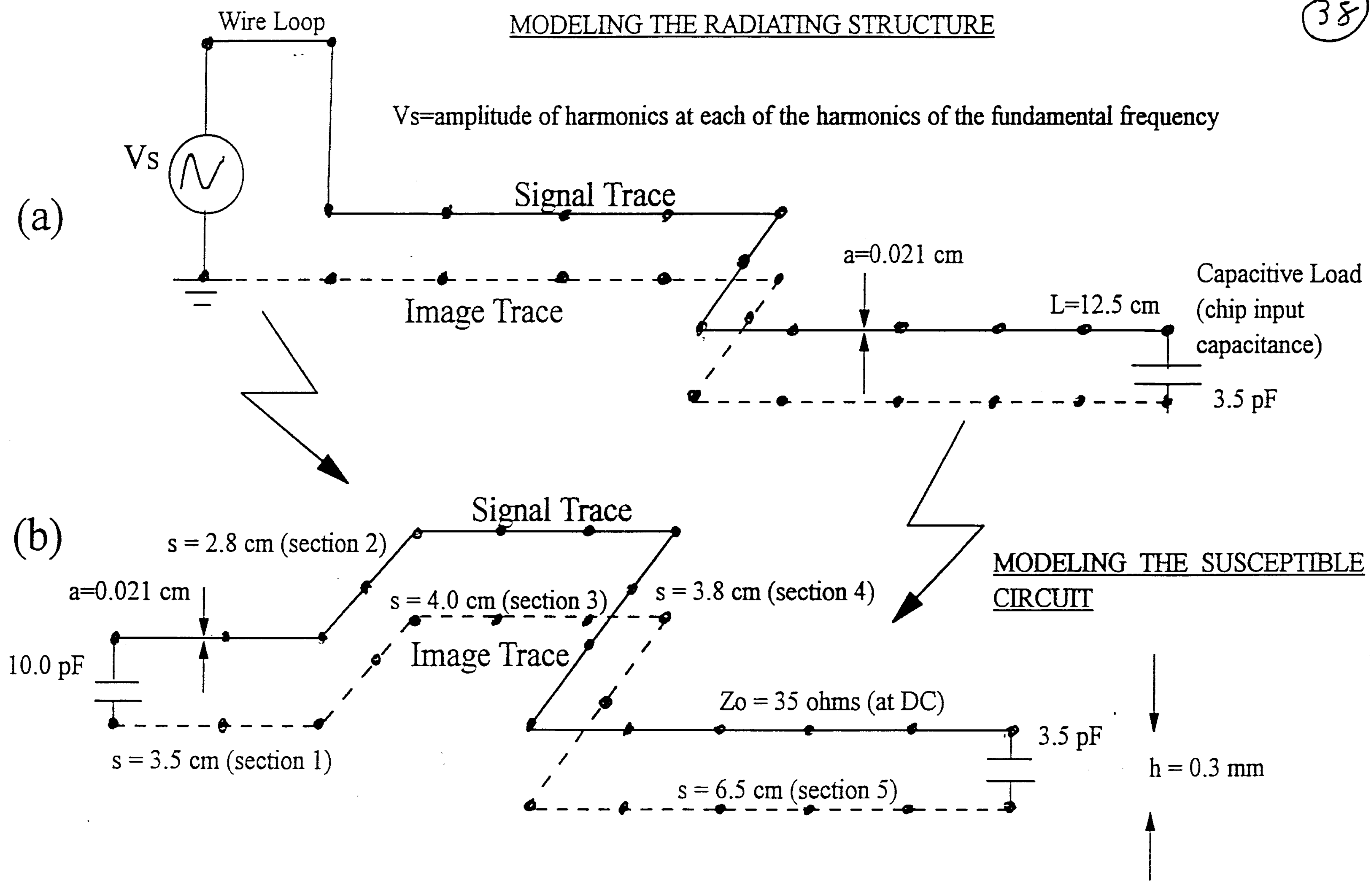


FIGURE 6. (a) METHOD OF MOMENTS MODELING OF RADIATING STRUCTURE,
(b) FIELD-TO-LINE COUPLING ON SUSCEPTIBLE CIRCUIT .

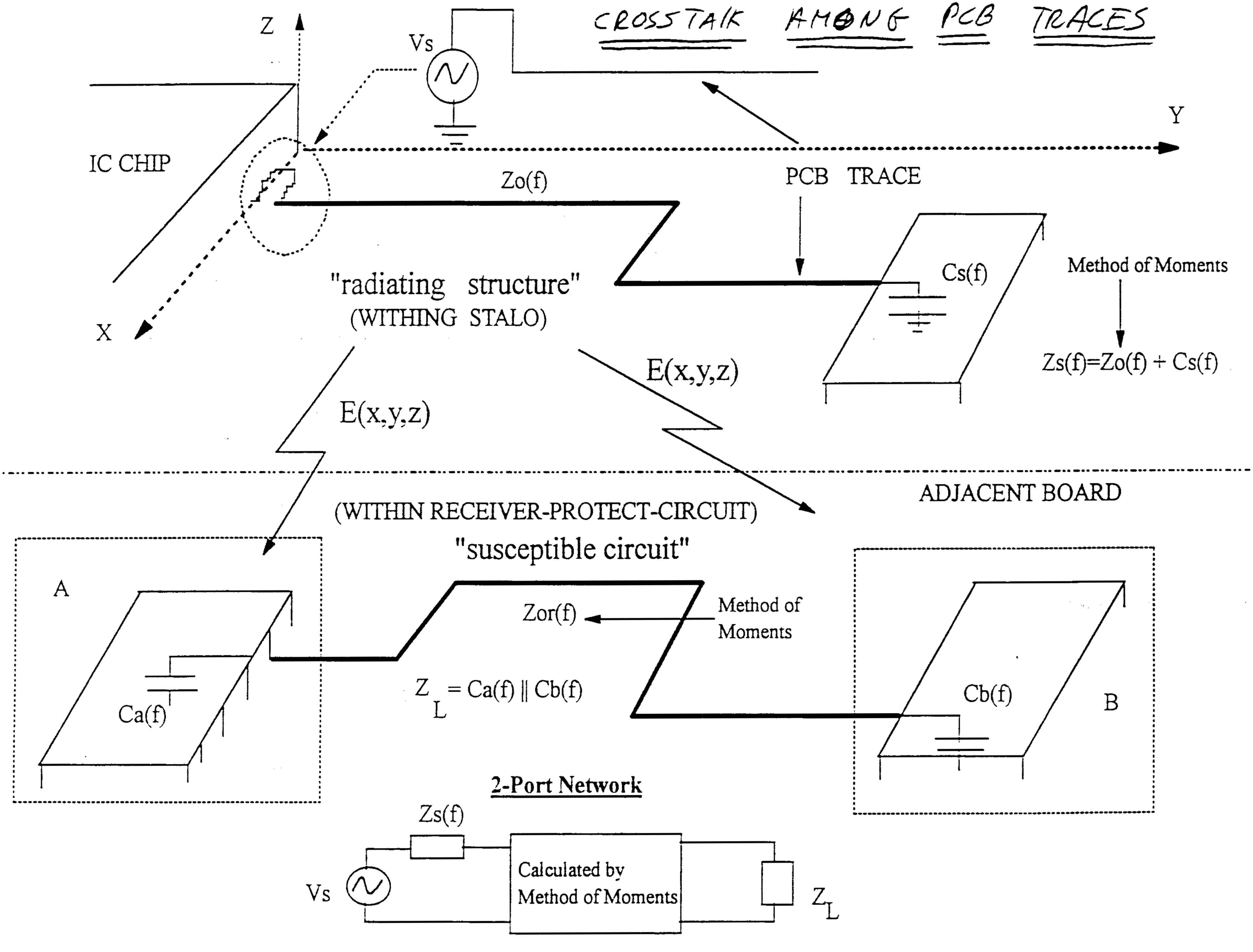
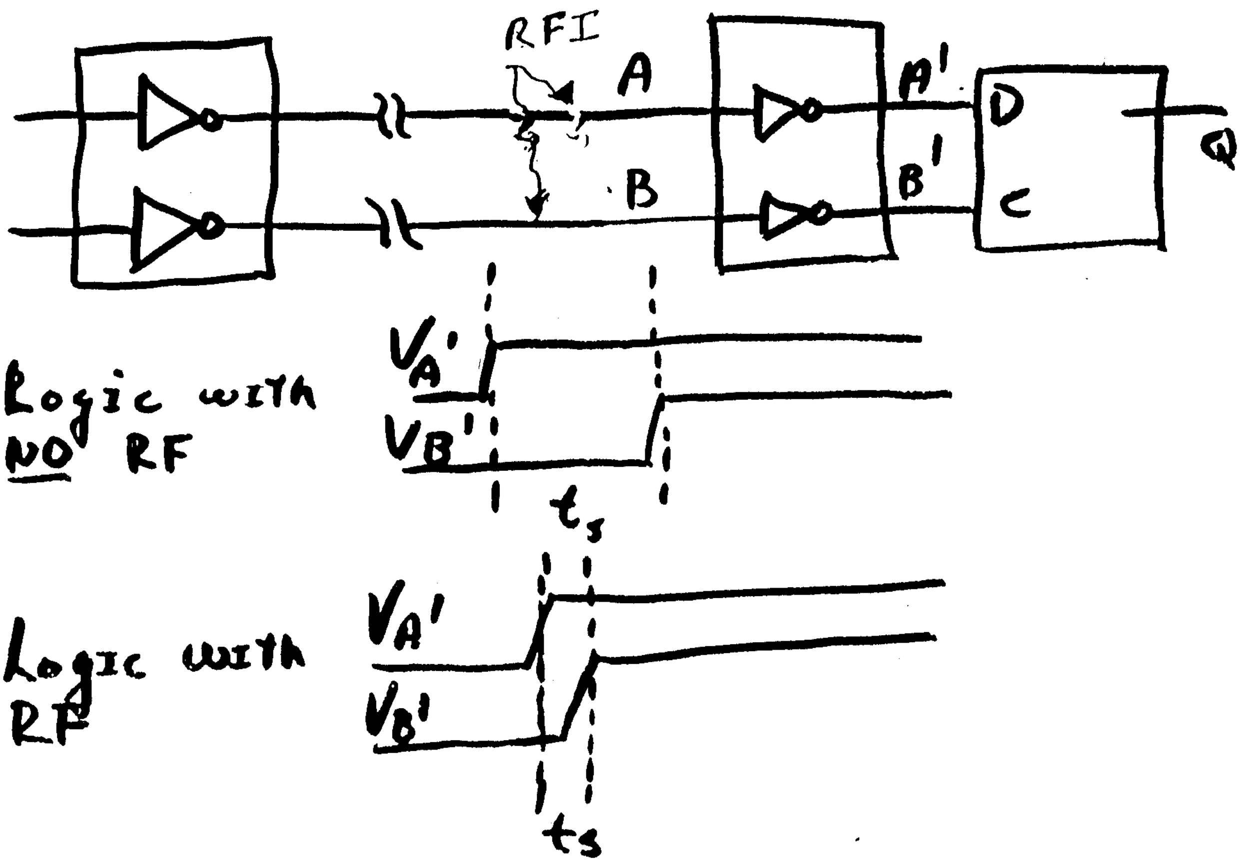


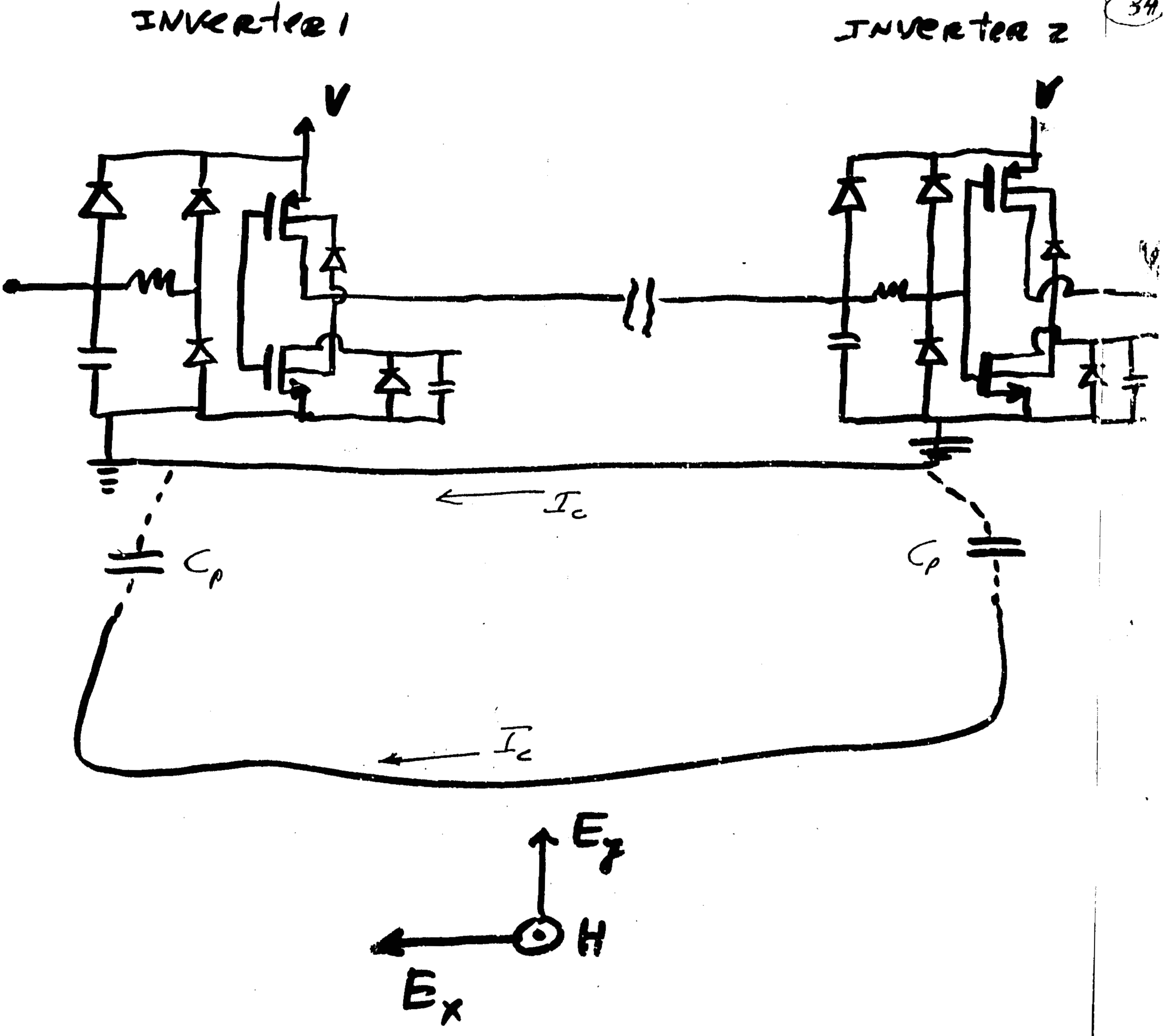
Figure 5: RADIATING AND SUSCEPTIBLE CIRCUITS IN PCBs

3) RF induced currents can cause "skew" timing problems in digital circuits.



skew time = max(t_s with RFI − t_s without RF

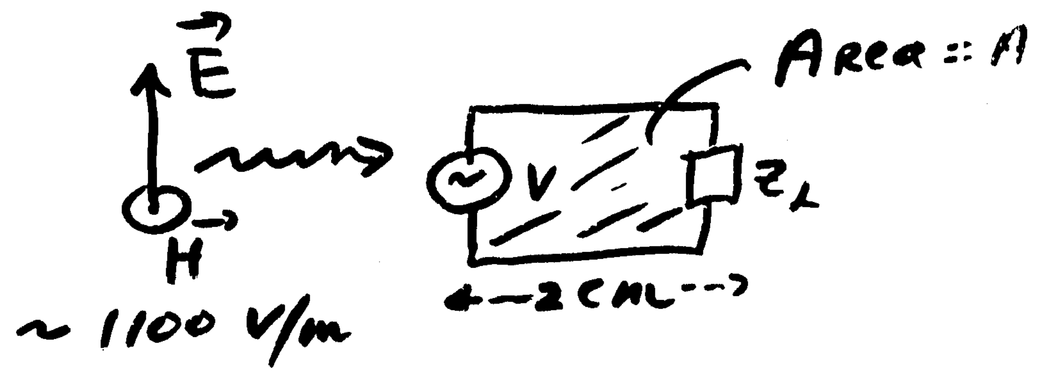
skew times depend on
1) phase of RFI signal at t_r of FF
2) change occurs if $t_s \le t_{setup}$ of F
3) output Z of inv. and input Z of FF



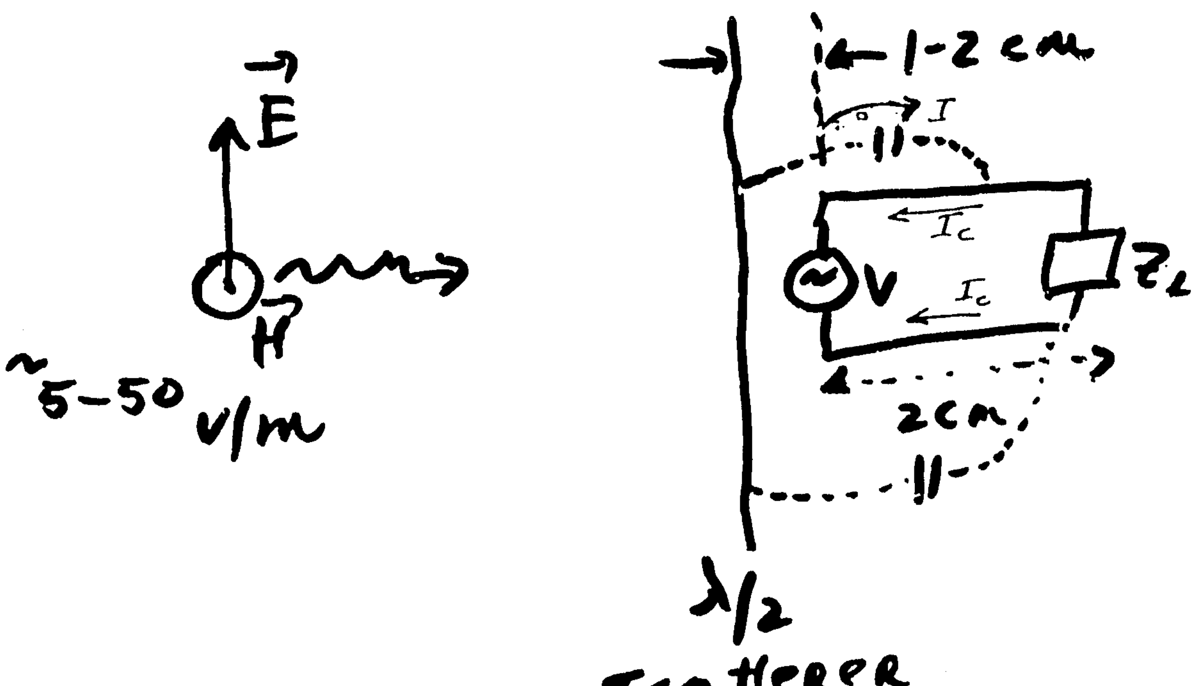
3) Poor grounding or poor signal connect[ion] can create large loops which will create large common mode currents when an incident field is incident.

Some Fundamentals

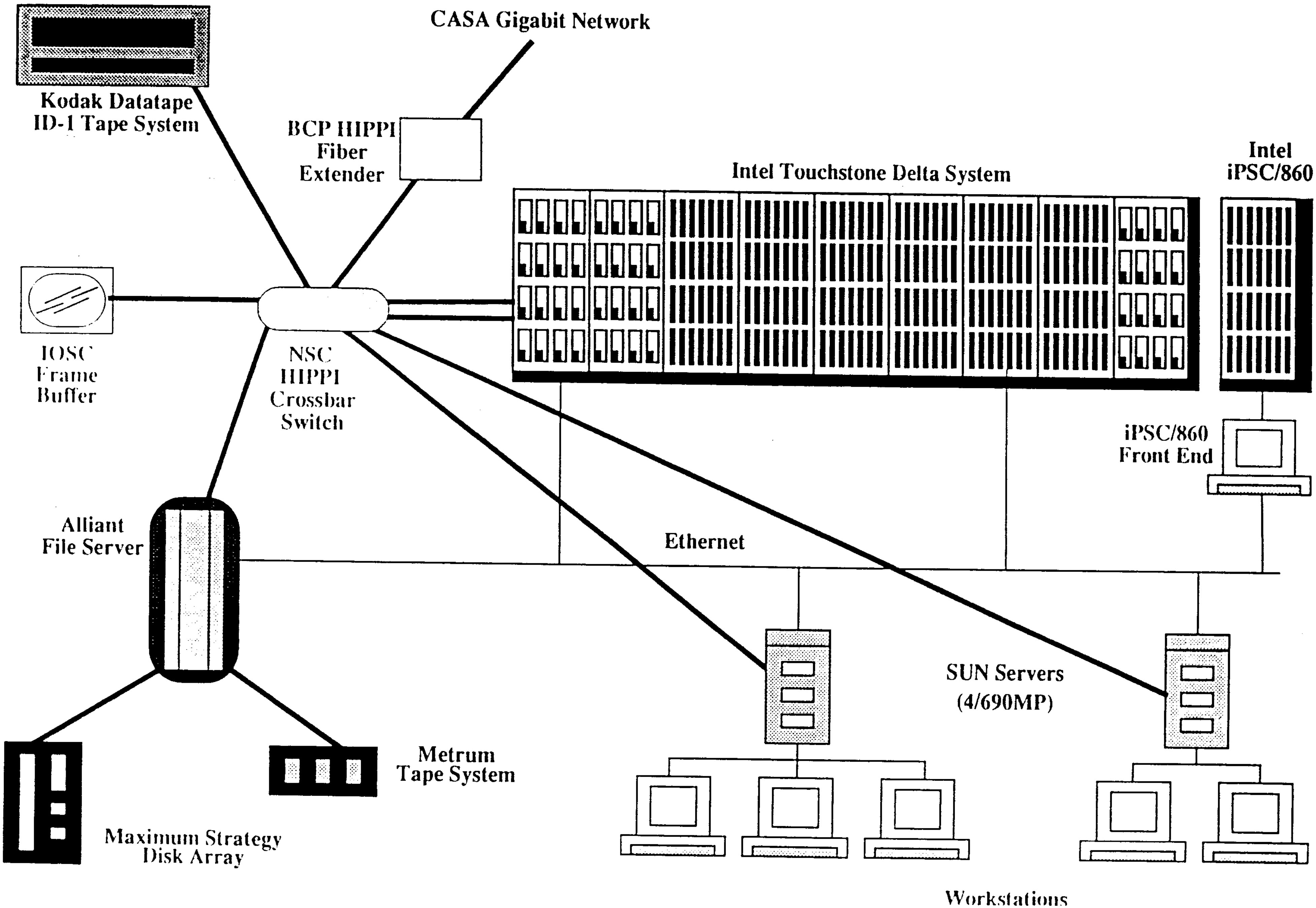
1) It takes a very "large" field to induced coupled current noise on a small PCB loop



2) A "large" scatterer, closed to the susceptible circuit can induce upsets (i.e sufficient coupled noise current) EVEN if the incident field is small.



CSCC Computing Environment



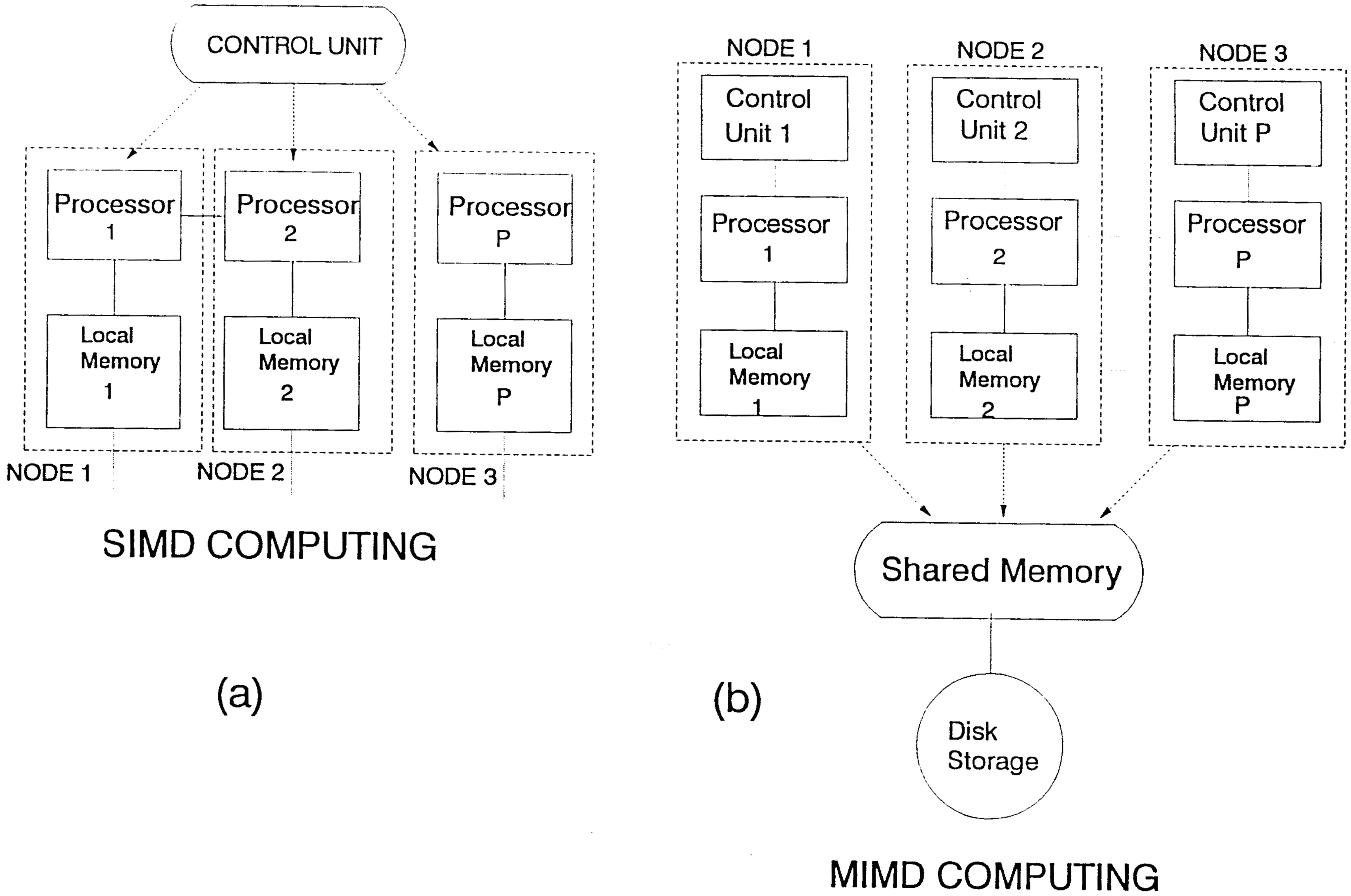


Figure 6. COMPARING SIMD AND MIMD COPUTING ARCHITECTURES

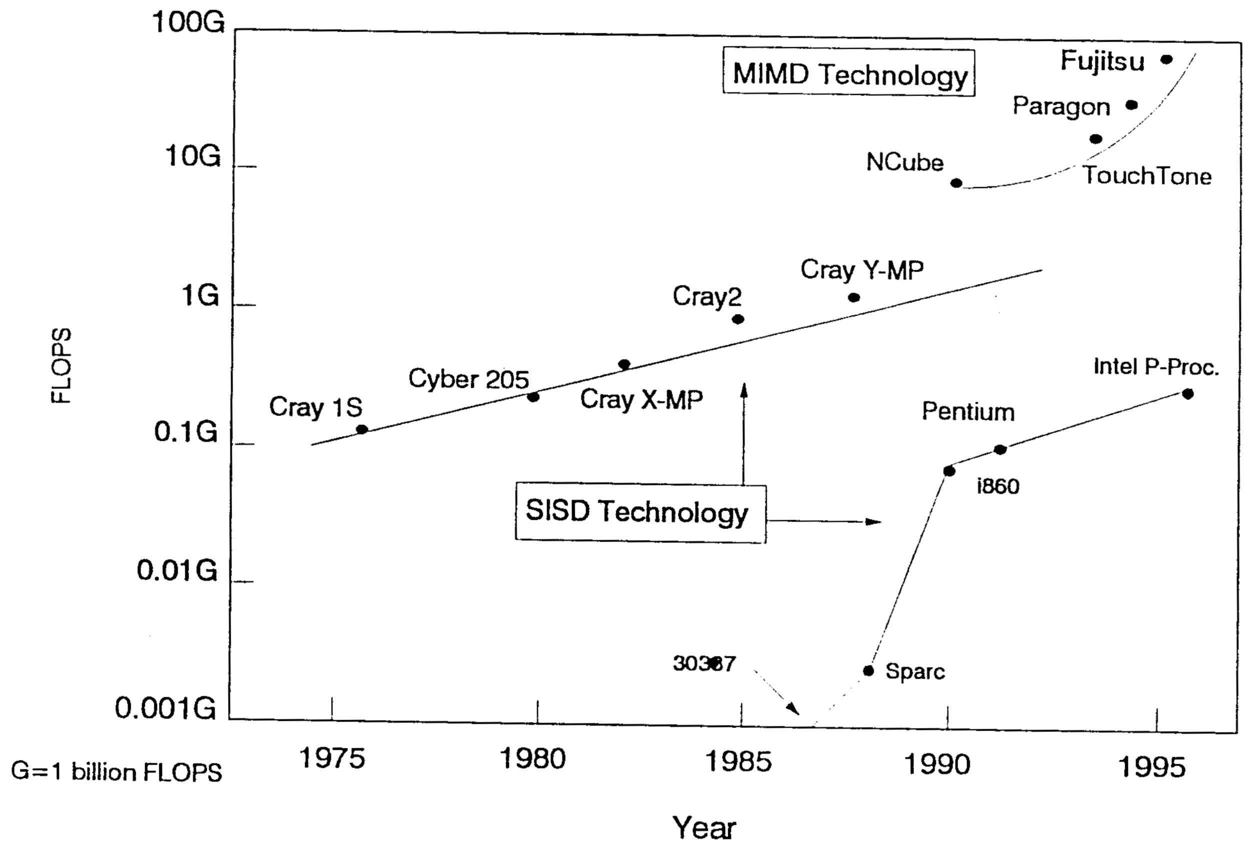
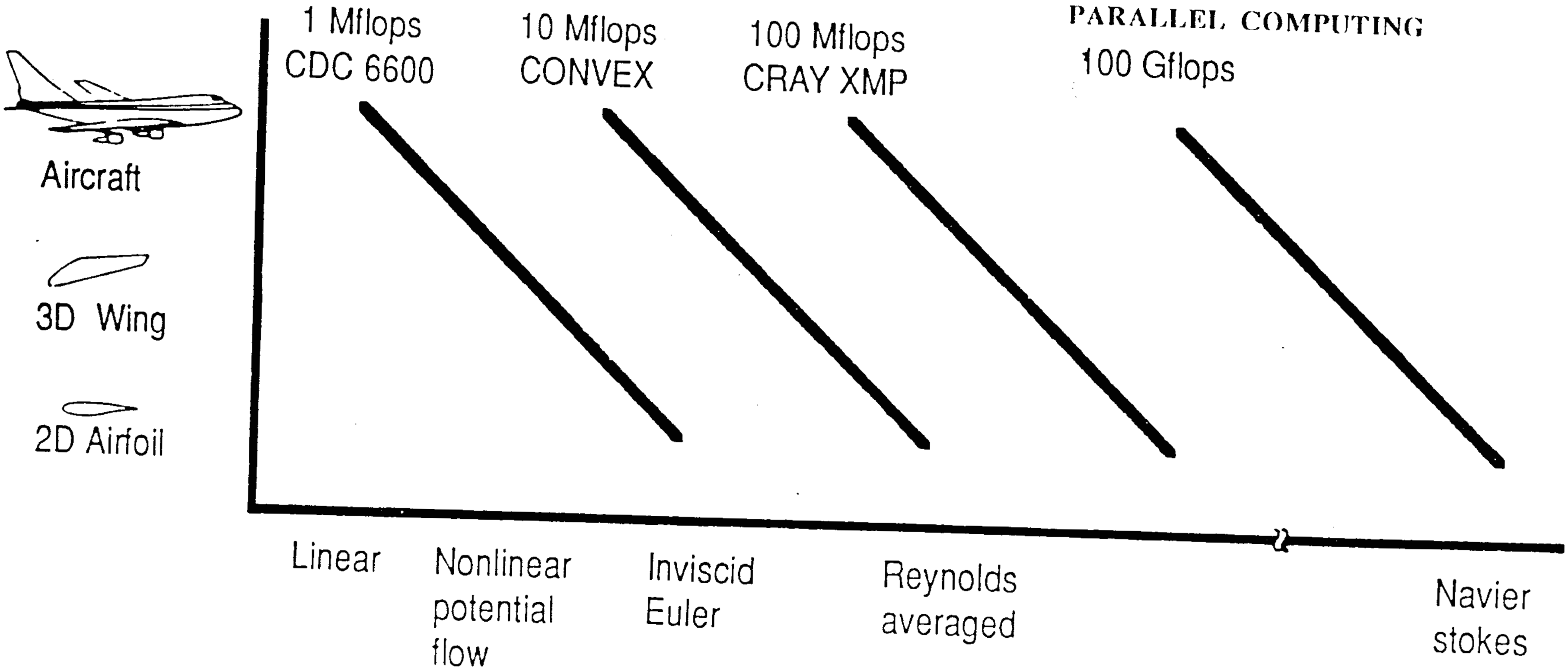
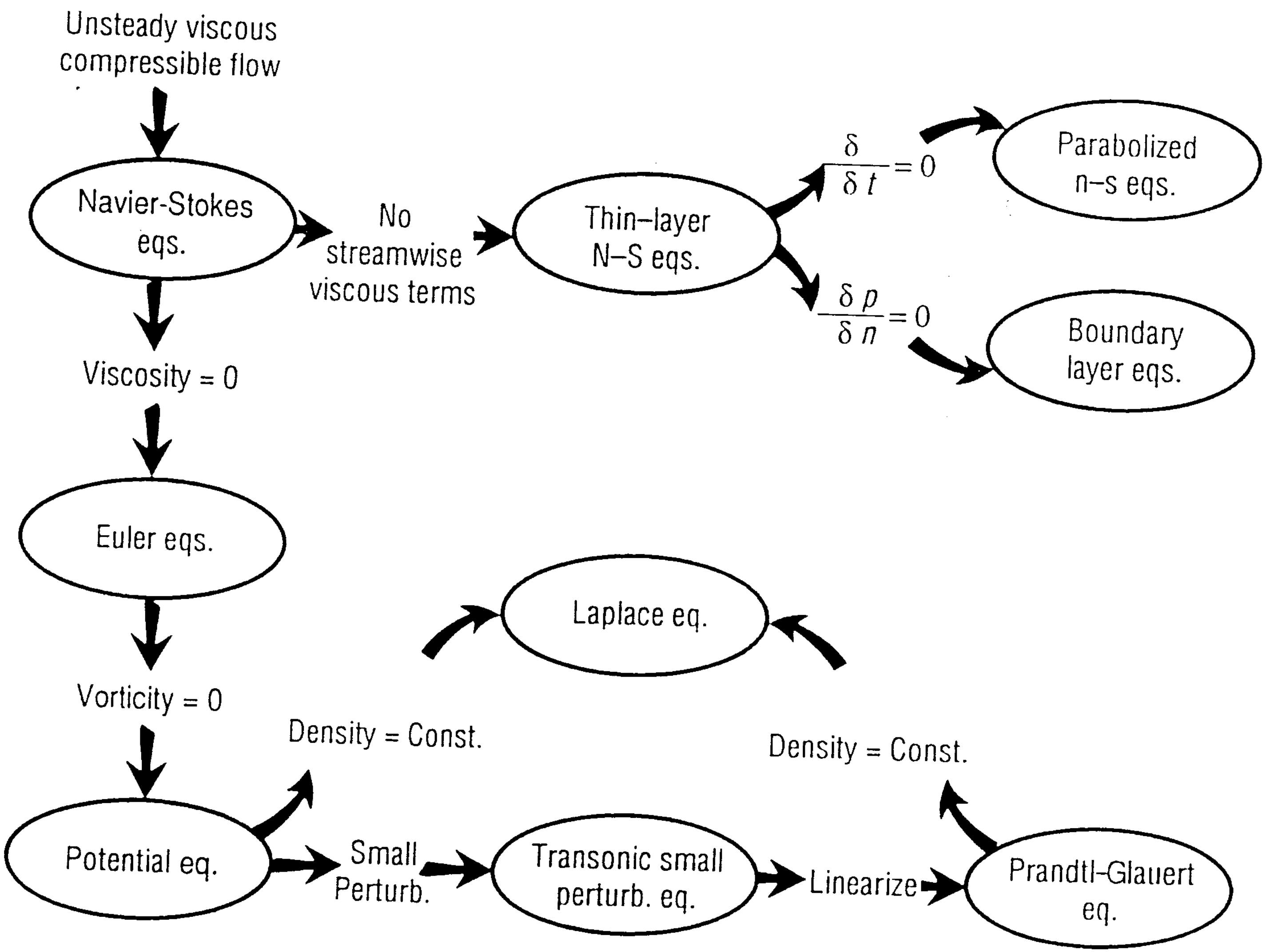


Figure 5. Peak Performance of Several Computer Technologies



COMPLEXCITY OF PROBLEMS THAT CAN BE TREATED WITH DIFFERENT COMPUTERS



EQUATIONS OF FLUID DYNAMICS FOR MATHEMATICAL MODELS OF VARYING COMPLEXITIES

COMPUTER POWER HAS ADVANCED GREATLY SINCE THE INTRODUCTION OF THE UNIVAC-1...

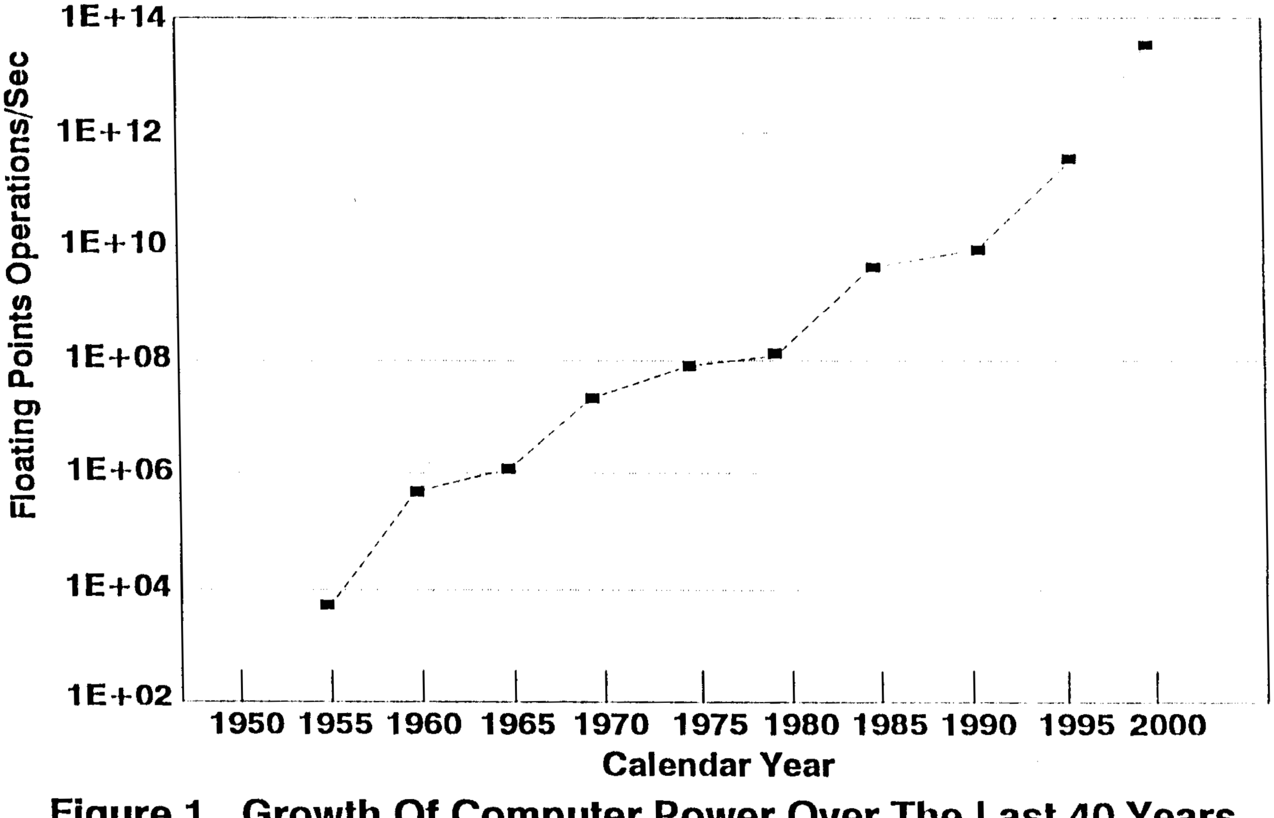


Figure 1. Growth Of Computer Power Over The Last 40 Years

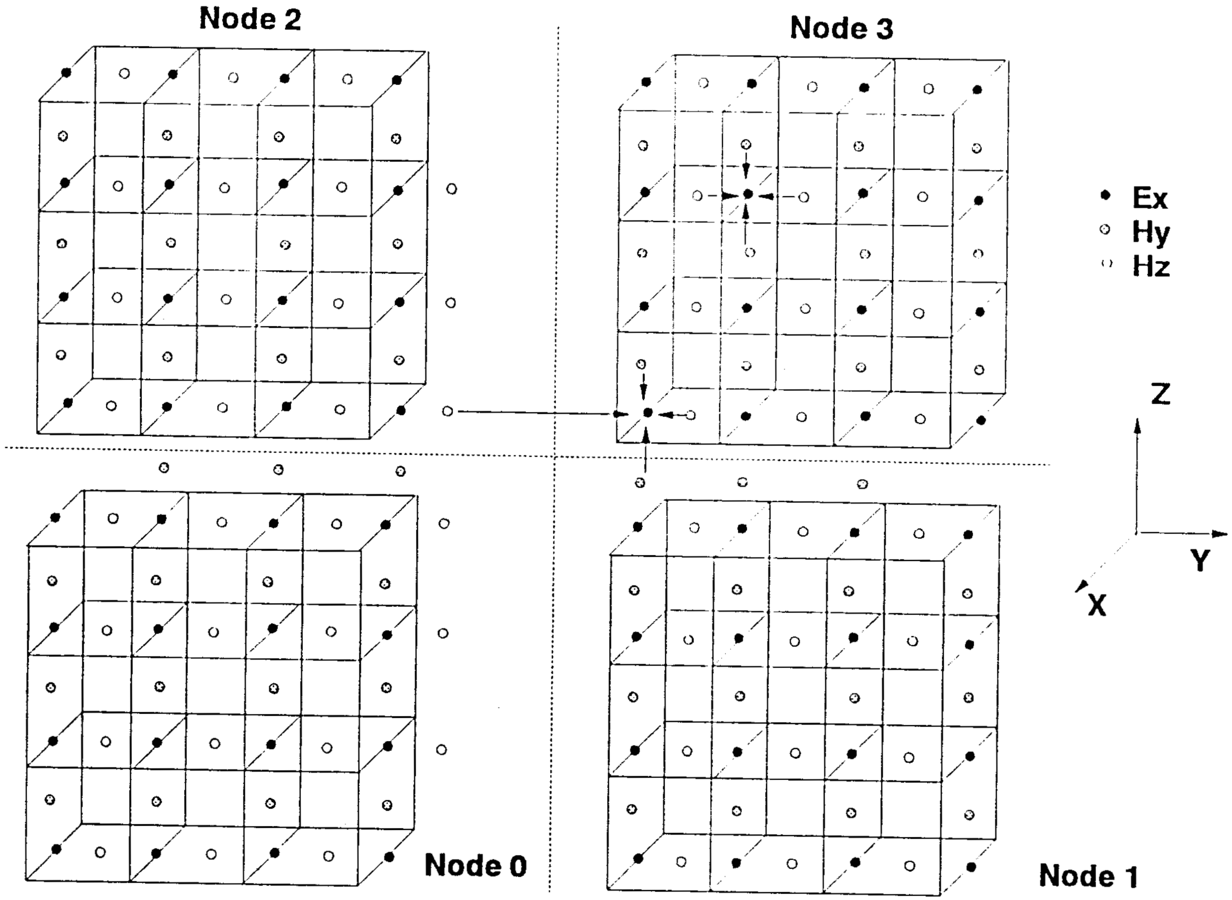


Figure 10a Lattice decomposition among four nodes for updating Ex

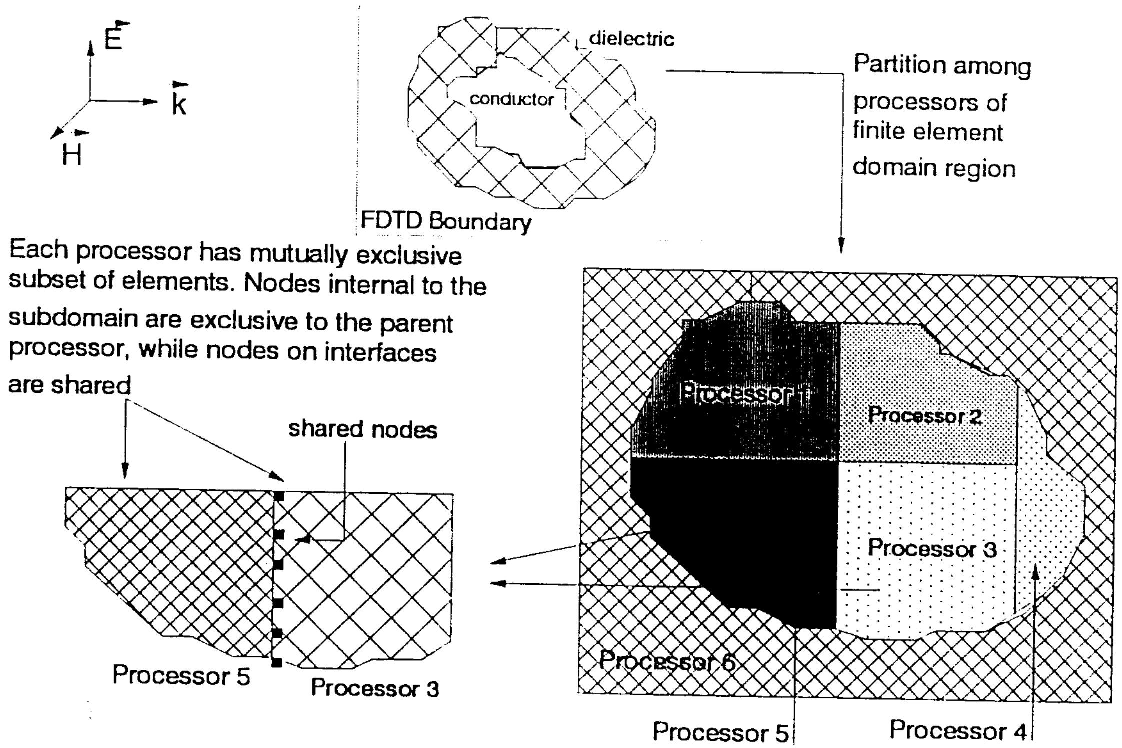


Figure 9. FDTD DISCRETIZATION IN PARALLEL COMPUTING

Conclusions

RAY'S AXIOMS ON EMC MODELING

1) Good test(s) may be worth 100 models (1000 models for ignorant modelers)

2) If you don't know what is going on. Do not model.

3) (collorary to # 2). Garbage in produces nothing but garbage (it does not matter how good and how much money you spent on your software).

4) The validity of code results depends more on the identification of the relevant physical processes and the soundness of approximations than on the sophistication of the MOM code or the size of your computer.

5) NEVER buy a MOM code (or really any code) without comprehensive documentation of the underlying equations, principles, approximations, and validity ranges. To do the contrary ranges from useless to dangerous.

6) Buying software to solve engineering problems is not an alternative to learning how to solve engineering problems.

7) Extensive analytical benchmark testing of new or existing technical software is critical because bugs are everywhere. NEVER accepts for validation of vendor's results of his benchmarks as the ultimate rationale. Develop your own and test them.

8) If you simulation brings forth an amazing potentially-publishable result, look for a numerical instability.

9) Beware the illusion of simplicity. Codes that appear to have all the data at hand and to make all the decisions for you (specially in EMC) are often based on questionable approximations.

10) Beware of EMC miracle workers: persons/vendors who claim their software (and technical expertise in modeling) will solve all your EMI problems.