REVIEW OF STACK CSP TECHNOLOGIES

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ABSTRACT

CSP is an emerging technology with significant potential growth in stacking. Many of the stacking techniques for conventional packages could be implemented for CSP once materials, process, and system development for finer features are developed. In the stack package technology, several packages of the same kind such as TSOP, SOJ (small outline J-lead), and a mixture with CSP are stacked in a vertical direction. This paper will review both conventional and the most recent stacking technologies for CSPs.

Introduction

Two approaches have been used to increase electronics density, i.e., the total memory capacity available divided by the space occupied on PWB (printed wiring board). Density increases have been achieved by the following techniques:

- Increasing density of memory chip and packaging. The chip scale packaging (CSP) approach is an example of size reduction through package shrinkage without increase in the memory chip density. Size reduction in memory chip has been achieved through advancement of photolithography technology and use of new materials and techniques enabling finer feature die circuitry.
- Stacking memory/packages on the board using the standard technology. Stacking bare dies and multichip modules (MCM) normal to the board can increase the memory density without sacrificing the board space. Stacking based on MCM technology has been widely adopted for increases in density. Similar approaches are being adopted by many manufacturers using TSOP (thin small outline package) and CSPs to further increase density.

This paper will briefly review MCM technology development at JPL. Then, the most recent development for CSP stacking with examples of peripheral and grid CSP stacks will be presented. Refer to Al-Sarawi et al [1], for a review of the status of MCM and bare die not discussed here.

3D MCM Development at NASA/JPL

Recent changes within NASA's exploration program favor the design, implementation, and operation of low-cost, light weight, small and micro-sized spacecraft, with multiple launches per year rather than several missions per decade. To meet the current and future needs of NASA's JPL, the 3D stacking

technology (including 3D chip stacking, horizontal and vertical space cube MCM stacking) have been investigated. Figure 1 shows the trend for the 3D packaging architecture which was validated under the Advanced Flight Computer (AFC) for the NASA's New Millennium Program (NMP).

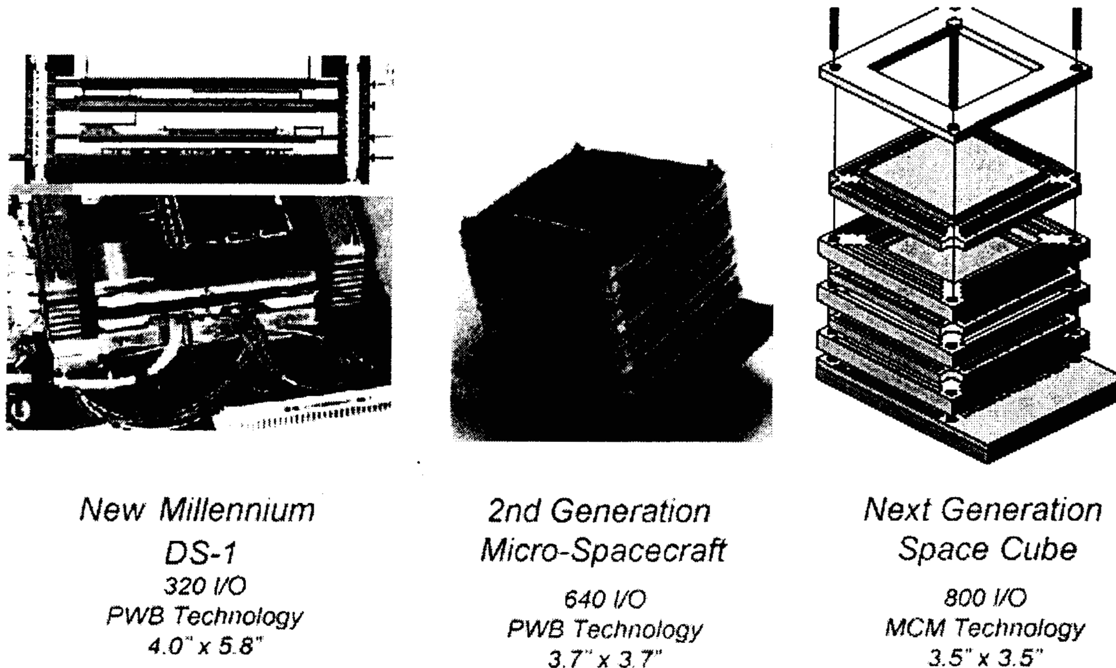

Figure 1 3D MCM for space applications

The qualification tests on the AFC 3D MCM included vibration, thermal vacuum, thermal cycling, and accelerated aging. This technology was an important development step towards further integration of avionics for the NASA's Deep Space System Development Program [2].

The vertical space cube is one of the next generation of 3D stack which builds on:

- Stacking MCM Packages
- Elastomeric Interconnects
- 200 I/O on each side of the stack, 3.5 by 3.5 inch package
- Double sided package

The most recent 3D MCM is the horizontal mount cube which was validated under the outer planet technology (X2000) of NMP [3]. The X2000 objectives are to advance the state of the art in spacecraft system development every three years with its first engineering model delivery by the year 2000, hence X-2000. Two of NMP's missions are the ST4/Champollion - a Comet Lander, and a Europa Orbiter. These missions incorporate the X2000 avionics architecture with a low cost system. The architecture will integrate different instruments, propulsion modules, power sources and telecommunication for multiple missions. The goal is to develop a modular building block design with standard interfaces enabling a high level of system integration. System on a chip (SOC) is the next generation of the integrated system.

STACK CSP

Direct stacking of bare memory chip can be costly and there are several issues that are yet to be resolved. These issues are similar to those issues when CSPs were compared to bare die. For example, lack of known good die, difficulty in handling, testability, and high assembly cost are a few. Nevertheless, this approach has been adapted by NEC using area array with interposer, and Fujitsu with die stacking and followed by packaging in CSP.

In the stack package technology, several packages of the same kind such as TSOP, SOJ (small outline J-lead), and a mixture with CSP are stacked in a vertical direction. This category of stack technology include:

- Peripheral
  - Conventional TSOP, SOJ, and SOC (small outline C-lead) are stacked in the vertical direction. Bare die stacking in conventional package.
  - CSPs of the same types are stacked or a mixture of CSP and conventional leaded packages are stacked.
- Area Array
  - Chip Scale package.
  - Flip chip bare die are stacked and then stacks interconnected by peripheral solder bumps.
  - Bare die are stacked internally with wire bond and then packaged in a grid CSP.
  - CSPs are stacked with the stacks interconnections by peripheral solder bumps.

CSP is an emerging technology with significant potential growth in stacking. Many of the stacking techniques for conventional packages could be implemented for CSP once materials, process, and system development for finer features are developed. Examples of leaded and CSP stacks advantages and disadvantages are summarized in Figure 2. This figure also illustrates two categories of stack technologies. There are a limited number of the stack packages are currently available or being developed. These include:

- Staktek [4] which uses stacking of conventional SOJ and TSOP packages
- Samsung Electronics [5] which uses stacking of conventional SOJ
- Fujitsu [6,7] which uses conventional SOC lead package and memory stacks in a grid CSP
- Hyundai [8] which uses stack chips packaged in a conventional SOJ package
- LG Semicon [9] which stack their BLP (bottom leaded package) leadless package [10] on the top of a conventional small outline L-lead package (SOL)
- NEC [11,12] which uses flip chips on substrates which are stacked through peripheral solder bumps
- Micron Technology [13] which uses an area array stack design

Examples of Fujitsu, LG Semicon, NEC, and Micron technologies are presented.

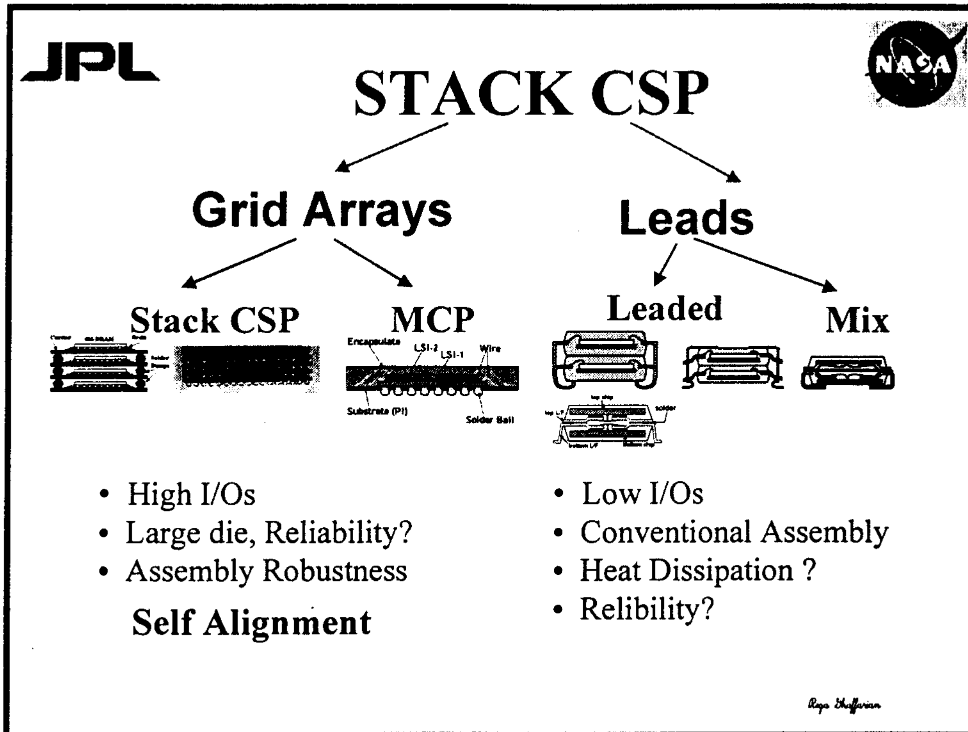

Figure 2 shows both illustrates representative CSP technologies from area array and leaded categories.

STACK SON (Small Outline no-lead)

Fujitsu developed a small outline no-lead (SON) package which later it evolved to be the small outline C-lead (C-lead). Both packages are peripheral and aimed for low pin counts (<50) such as memory devices. The C-lead, similarly to the TSOP stack package, was stacked to form a three-dimensional packaging module (3DPM) as shown in Figure 3.

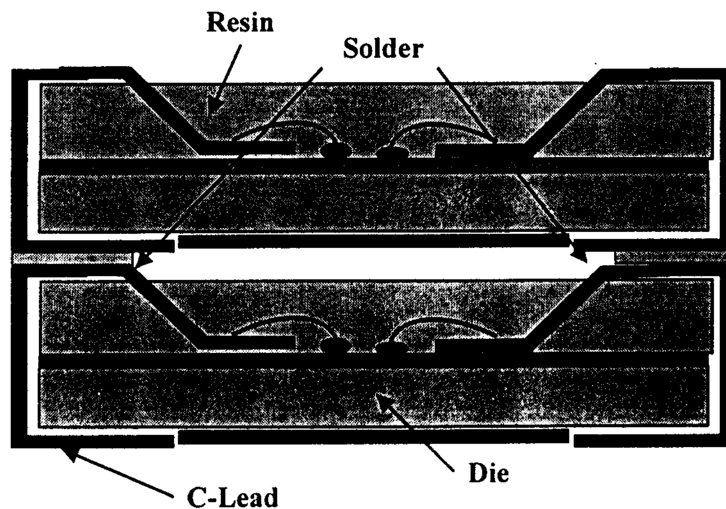

Figure 3 Fujitsu's three dimensional packaging module

Electrical simulation modeling showed that SON and SOC have better electrical performance than a conventional TSOP. The improvement was attributed to their shorter height and length than TSOP. Thermal performance for SON is also better than TSOP. This is not true for SOC and TSOP. In either case, the copper lead configuration has better thermal characteristics. The four stack (Figure 9) showed the best performance both for Cu and alloy 42.

The SOC single packages were subjected to thermal cycling and the pressure cooker (PCT) test. It passed 1,000 thermal cycles in the range of –65°C to 150°C and 168 hours of PCT at 121°C and 85% relative humidity. In addition the solder joint thermal cycling behavior of the SOC 3D packages on FR-4 were compared to its single SOC package and TSOP on a double sided PWB. Table 3 lists cycles to failures for these packages. All packages passed 500 thermal cycles in the range of –55 to 125°C with the least damage (cracks) for the SOC stack version [6].

D2CSP STACK

The D2CSP developed by LG Semicon is a stack package for 128 Mb SDRAM with two 64 Mb SDRAM in which a bottom leaded package (BLP) was stacked on top of a leaded package (Figure 1 under Mix category). The compliant leaded package permits improvement of the board reliability of the BLP package in the stack form. The D2CSP can be used for high-end application systems, e.g. servers and work stations. In addition, the concept of D2CSP can be extended to accommodate a higher density module with an overall lower cost.

The D2CSP meets the JEDEC level I requirement since it passed preconditioning test (IR reflow test). This means that D2CSP can be stored for a long time prior to SMT assembly without potential of popcorn cracking during reflow process. This high crack resistance stems from the high reliability of the BLP package design. [10]

The ease of surface mount assembly was shown by assemblying of two hundred twenty two daisy chain D2CSPs on four layers, FR-4, 1.27 mm thick. Solder paste was 63Pb/37Sn eutectic and printed using a 0.15 mm stencil thickness. After solder reflow in a convection oven, all samples were visually inspected as well as by X-ray. Except for only eight devices failing due to wire bond failure, the rest packages remained in good condition.

Solder joint reliability was assessed by accelerated thermal cycling test assemblies. The test condition was –65 to 125 °C, 2 cycles per hour. The solder joint failure criterion was 20 % resistance increase. Assemblies survived 1,500 cycles with no failures.

3DM (Three Dimensional Memory Module)

Area array stack memory developed by NEC has flip chip die on interposer with additional large peripheral solder bumps for interstack interconnection. Figure 4 depicts a four module configuration. This package has four times the memory of a conventional TSOP and has a slightly larger foot print. One type of first-level interconnection is a gold stud bump which is a joint by forming thermal compression. Even though these bumps do not require solder and flux, they require a high temperature ceramic substrate to surviving the high temperature bonding process. In another type, a solder bump

with a lower reflow temperature requirement (instead of a stud bump) was used to reduce the memory exposure to elevated temperature during solder reflow. In addition, copper core ball bumps were used for the peripheral interconnections, in order to control stack space and avoid PWB contact to die. Similarly to other flip chips, dies were underfilled to enhance first-level reliability interconnection.

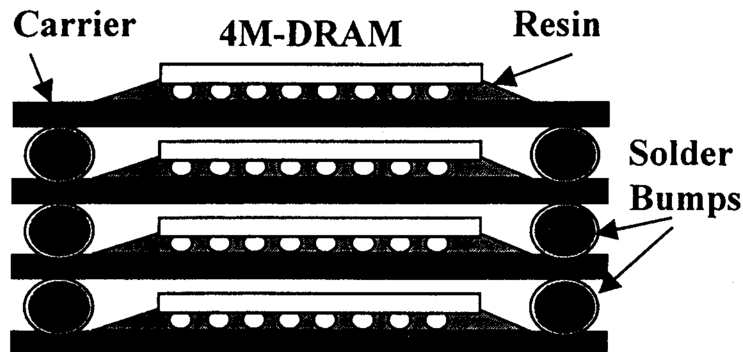

Figure 4 NEC 3D Memory Module, 4 packages

Reliability tests were performed on single as well as 3D modules with different die sizes [11. Environmental tests performed included: heat test (HT) at 125°C, thermal cycle test (T/C) in the range of –40°C to 125°C with 30 minute cycle duration, and a pressure cooker test (PCT) at 110°C, 85% humidity, in a 1.2 atm. For the smallest die size, environmental behavior of the single and 3D modules were the same. This was not true for the larger dies. For the modules with the larger dies, the 3D version had inferior thermal cycling behavior. The single module survived 750 T/C whereas the 3D version showed signs of failure at 100 cycles with the majority of module failures at 500 cycles. It was determined that the weakest link was indeed the peripheral inter stack interconnection. Peripheral balls have the largest distance to neutral point (DNP) and therefore maximum CTE mismatch strains.

The second level solder joint reliability for the small die module was evaluated by assembly on DIMM epoxy board, similar to inter die substrates. These were subjected to 3,000 thermal cycles. There were no solder joint failure of any interconnection, i.e., between dies, peripheral inter stack interconnections, or solder joints on DIMM. It was concluded that high reliability of system interconnection is possible.

MCM version of this technology on ceramic substrate was used for a RISC (reduce instruction set computer) for application in a high performance workstation. The design consists of a D/L (deposited organic thin film on laminated printed-circuit board) base substrate, a glass ceramic based organic thin film multilayer build up CSP and a 3Dimentional glass ceramic memory module. This package is in its prototype stage and is being considered to be used for various workstation and supercomputer applications.

3D SBGAs (Stackable Fine Pitch Area Arrays)

Micron Technology Inc. has considered several stacking technologies for DRAM. A stackable fine pitch area arrays (SBGA), similar to the NEC stacking, is one of this approach as shown in Figure 5.

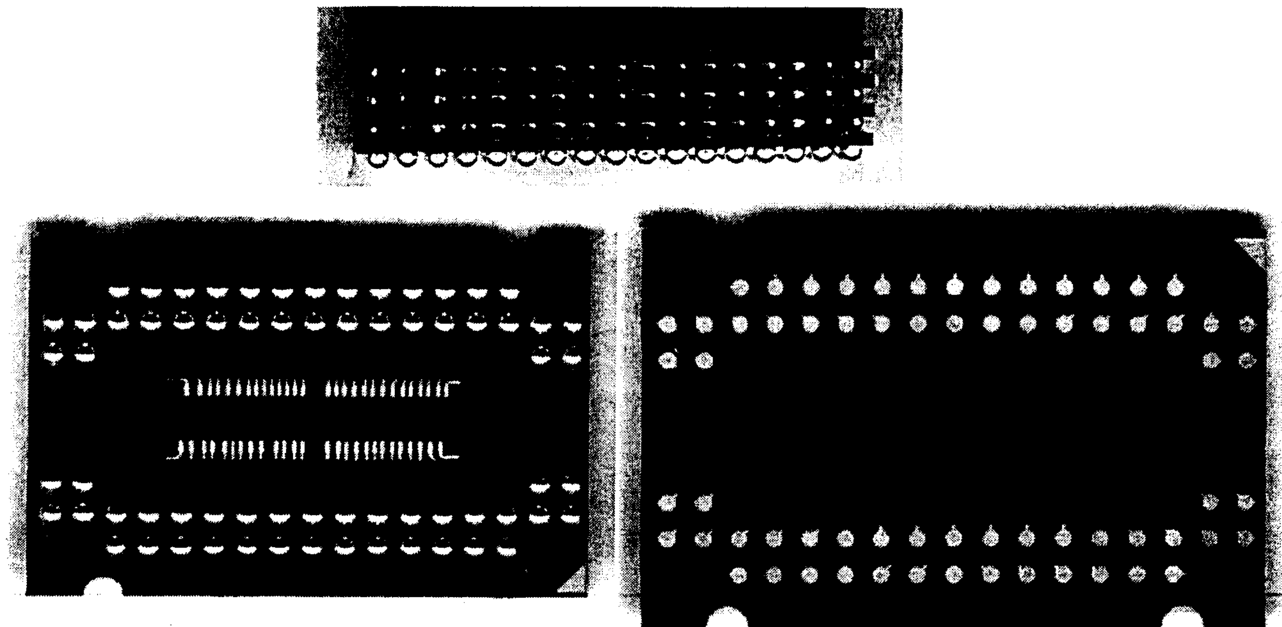

Figure 5 4D stack memory design by Micron

An SBGA is the stacking of one array upon another. The stackable FBGA package is configured such that conductive elements are placed along the outside perimeter of a semiconductor device (integrated circuit (IC) device) mounted to the SBGA. The conductive elements also are of sufficient size so that they extend beyond the bottom or top surface of the IC device. Wire interconnects connect the IC device in a way that does not increase the overall profile of the package. Encapsulating material protects both the IC device and the wire interconnect, as the conductive elements make contact with the SBGA positioned below or above to form a stack. A memory chip is mounted upon a first surface of a printed circuit board substrate forming part of the SBGA. Lead wires, or bump interconnects, are used to attach the IC device to the printed board substrate and encapsulant is used to contain the interconnect within and below the matrix and profile of the conductive elements.

Additionally, certain pins on the SBGA in the stack require an isolated connection to the PC board. An example of such a requirement is when an activation signal for a particular IC device within the stack must be sent solely to that device and not to any of the other devices within the stack. This isolated connection connects to an adjacent ball on a different FBGA stack above or below that particular isolated connections. In common pin layouts of devices stacked together, each device requires an isolated connection to the PC board.

This provides for a stair step connection from the bottom of the FBGA stacked array to the top that allows each device, from the bottom one to the top one, to have an isolated connection from each other. This allows IC devices to be stacked one upon each other while maintaining a unique pin out for each pin required in the stack.

STACK MCP (Multi-Chip Package)

Fujitsu's MCP uses stacked die as shown in Figure 6. The Stacked MCP (Fine Pitch BGA) has the following characteristics:

- Package is FPBGA with 8x8 (56 balls, excluding non-connected balls), 0.8 mm pitch
- It requires 30% less board space than two separate TSOPs
- Stack can be configured to have Flash and SRAM combination of 8x8, 8x16, and 16x16 bit memory
- Flash and SRAM memory can extend up to 128 Mb for the same package pin configuration

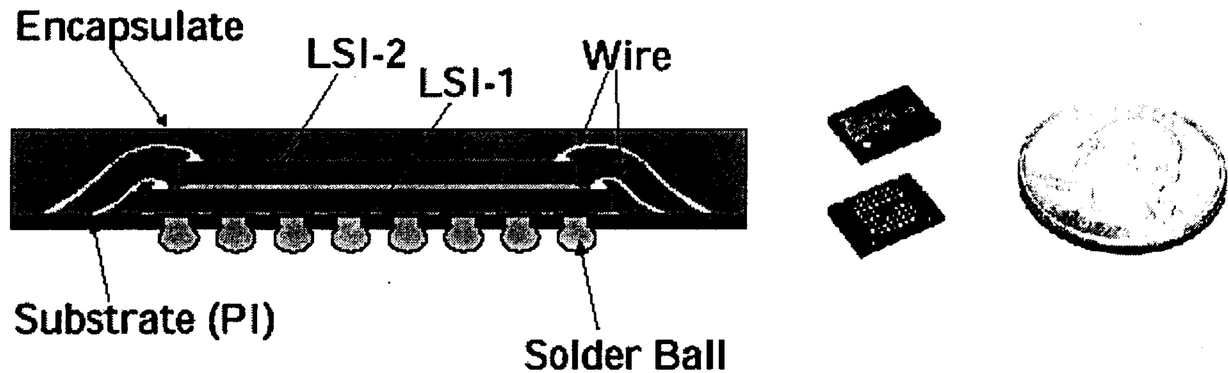

Figure 6 Fujitsu's Multi-Chip Package

Currently, there is an active proposal on registration for a Low Profile Fine Pitch (FBGA) Stack MCP family[7].

DISCUSSION

Package/die stacking technology enhances most aspects of electronic systems such as size, weight, speed, yield, and power consumption. Their reliability and robustness could also be improved if the faulty package/die is systematically eliminated during the stacking assembly. Currently, stacking is limited by a number of factors. Some of the limitations such as thermal management, stem from densification, others are due to the current technological limitations, such as via diameter, line width, via pitch, and line spacing. It is expected that the effect of such limitations will decrease as the packaging technology advances.

The main issues in stacking are quality and density of the inter-stacking interconnects, electrical, mechanical and thermal characteristics, design tool accessibility, reliability, testability, rework, special set up and package cost, known good die (KGD), and fabrication time. These factors determine the selection of a stacking technology for an application. Since most stackings are designed for special applications, they lack standardization as well as information accessibility generated by the stack manufacturers. These issues have been resolved for the cases where standard packages are stacked.

MCM technology developed for the high end application is now being duplicated using miniature feature of new emerging CSPs for low I/O, high volume application. Multi chip package having two or more

die stack or spread are used to further increase density and functionality. Similarly to other stacking technology, system reliability, heat dissipation, and generation of additional electrical parasitic are key areas of concern for stack CSPs.

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