A Boundary Scan Test Vehicle for Direct Chip Attach (DCA) Testing

Heather Parsons
Saverio D’Agostino
Genji Arakaki
Jet Propulsion Laboratory

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Topics

Background: Direct Chip Attach

Test Methods

What is boundary scan and how does it work

How is it currently being used

Usefulness to others
Background: What is Direct Chip Attach?

Equivalent to Chip-On-Board

Bare die bonded directly to the printed wiring board

Wire bonded

Non-Hermetic Packaging

To validate an encapsulation or passivation technology for New Millenium Deep Space - 2 (DS-2) and other flight projects

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Background: DCA Objectives

To design a substrate that
- gives a realistic understanding of how the environment affects powered devices
- provides information about the reliability of passivation technology

- Span wide range of part types

- Testing
  - Fast
  - Automated
  - Repetitive
  - Log data
Test Methods

Daisy Chain
- simple for solder joints or connectors
- non-powered devices
- don’t know exactly what interconnect has failed

Boundary Scan
- IEEE Standard (JTAG)
  - Standardized
  - Commercially available
- powered devices
- digital test
- determine failure at interconnect level
  - short
  - open
Boundary Scan Chip
Board Design

Boundary Scan Devices

Memory Chip

Mosfet

SIR Patterns

Sandia Test Chip NAT01

Sandia Test Chip ATC 2.5

A to D Converters

U1

U2

U5

U4

U3

TDI

TDO

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Direct Chip Attach
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Devices on Board

Packaged Parts
- Boundary Scan Chips
- Resistors
- A to D Converters

Bare Die
- A Memory Chip
- Several Schottky Diodes
- MOSFETs (Both N and P Channel)
- Sandia Test Chips
  - ATC 2.5
  - NAT01
- SIR Patterns
Boundary Scan Test

- Diodes - Series connected with resistor
- Mosfets - N and P channel configured as inverters
- SIR Patterns - Voltage divider will show non-zero value if current flows
- ATC2.5 / NAT01 - A to D Converters will sense change in voltage divider
Test of Static Memory (SRAM) by Boundary Scan

- Boundary Scan used to write to SRAM
  - Boundary Scan Chip 1 feeds addresses
  - Boundary Scan Chip 1 feeds data inputs

- Boundary Scan used to read SRAM
  - Chip 1 feeds addresses
  - Chip 2 reads Data outputs

- Data shifted out - verified

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The Boundary Scan Test System

Asset
- Hardware Card
- Interface Pod
- Windows Software
The Boundary Scan Test System

Scan Path ATPG: Test results for entity dcabd3. This test detects:
- Stuck-at-0 on the TDI/TDO data path.
- Inoperative TCK.
- Inoperative TMS.
- Incorrect scan path length.

Pattern Is Constant 1

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Step 1. Expect the value normally captured by the BYPASS/IDCODE registers.
No failures detected.
Step 2. Expect the pattern shifted through the BYPASS/IDCODE registers.
No failures detected.
Pattern Is Constant 0

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Step 1. Expect the value normally captured by the BYPASS/IDCODE registers.
No failures detected.
Step 2. Expect the pattern shifted through the BYPASS/IDCODE registers.
No failures detected.
Pattern Is Constant 0110

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Step 1. Expect the value normally captured by the BYPASS/IDCODE registers.
No failures detected.
Step 2. Expect the pattern shifted through the BYPASS/IDCODE registers.
No failures detected.
INFO MAX064: C:\ASSET23\DcaAsset\DCAbrd\Macros\Scanpath3.mac(247) Program ran successfully.

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- Uses Macros to program test
- Compares test data out to data expected
The Boundary Scan Test System

LabVIEW

- Logs time, date, and other relevant information when there is a failure
- Continuous testing

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Successfully able to test

diodes
mosfets
SRAM
Future Tasks

- LabVIEW up and running
- Continuous testing in thermal and HAST chambers
- Testing all different types of new Packaging technologies

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Boundary Scan use for DCA

- test at interconnect level
- automated testing that logs failures

Boundary Scan as a valuable resource to testing new technologies