ADVANCED INTERCONNECT ROADMAP
FOR SPACE APPLICATIONS

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Lissa Galbraith, Ph.D.

JPL
National Aeronautics And Space Administration
California Institute of Technology
Jet Propulsion Laboratory
NASA Electronics Parts and Packaging Program
Quality Assurance Office 506
INTRODUCTION

• Past: NASA CODE AE Parts & Packaging Functional Initiative Program: Effective Integration of Critical & Complex Electronic Packages & Technologies

• Now: NASA Electronics Parts & Packaging Program (NEPP)
  ▪ Parts, Packaging, Radiation Testing, Information Management

• National Roadmap of NEMI includes
  ▪ IPC, NSIC Magnetic & Optical Storage, SIA, OIDA, USDC Display

• Technology Challenges

• Recommendations for Research Directions

• Technology forecasts
FORECASTS

- Package, Wafer, Flip Chip, and Hybrid Assembly Integrated into SMT

- Increased Use of Multiple Technologies in One Package such as Optoelectronics and MEMs

- Increased integration of power devices

- PBGAs Retain Highest Volume of BGA Use

- Increased Use of Flip Chip In Package (FCIP), Requiring:
  - Low Cost Bumping, Copper-based Silicon
  - More Cost Effective Substrates, Better Bare Die Testing
  - Shorter Underfill Time
  - More Efficient Rework
FORECASTS, continued

- New Packaging Materials Meeting Greater Moisture Resistance

- Improved Underfill Materials: Fast Processing and Curing, Low Stress, Fine Gap, and Compatible with No-clean Fluxes

- Reduced Wicking Process Time for Underfills and Coatings Using Injection or Vacuum Methods

- Greatly increased implementation of integrated passives

- Increased high frequency applications (≥ 1GHz)
FORECASTS, continued

EXAMPLES

- Continued NASA Research in HDP Use in Extreme Environments
  - DS2 Mars Microprobe Penetrator Tip COB Si Carbide Structure
  - 80K g at tip impact into Mars soil

- X2000 First Delivery
  - HDP (MCM) Packaging Built into Integrated Avionics Structure
## Technology Challenges

<table>
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<tr>
<th>Performance Needs</th>
<th>Packaging Response</th>
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<tbody>
<tr>
<td>Increased Bandwidth</td>
<td>Higher Total Gate Count</td>
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<td>Higher Number of Gates in CPU</td>
<td>Decreased Wiring Delay</td>
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<tr>
<td>Increased Clock Frequency</td>
<td>Min Distance Between Chips</td>
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<tr>
<td>Min Memory Access Bottlenecks</td>
<td>Min Distance Bet CPU &amp; Memory</td>
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- Dense & Flexible Interconnects between Stacked HDPs
- Extreme environment polyimide flexible circuit reliability
- High Heat Dissipation Technology for SMT
- Improved Guidelines & Infrastructure for Packaging/integration Selection
RESEARCH DIRECTIONS

- Blind and Buried Vias for Dense Small Form Factor PWAs
  - Laser Drilled, Photoimaging, and Plasma Etching

- Improve Wafer Bumping for Flip Chip and Optoelectronics Packaging

- Better Understanding of Effects of Miniaturization on Electromagnetic Interference and Compatibility Within and Between Modules

- NIST ATP Microelectronics Manufacturing Infrastructure:
  - Wafer Technology, Semiconductor Packaging
  - Very High Density Off-Chip Interconnects
  - Chip to Board Integration
RESEARCH DIRECTIONS FOR CHIP ON BOARD (COB)

- Design Guidelines for COB Passivation Techniques

- Validated Test Regime for COB Range of Flight Environments

- Integration with Design Validation of Chip Scale Packages, COB, and Flip Chip

- COB Manufacturing Process Control Guidelines

- Copper Cladding for COB Site Preparation
RESEARCH DIRECTIONS FOR HDPs: MULTICHP MODULES (MCMs)

- Process Evaluation of Micro-via Technology Using Plasma, Laser and Chemical Etch

- Integration of passives into MCM-L, -D, -C
  - Multiple Dielectrics/Ceramics
  - High Precision Resistors

- Polymeric Materials Evaluation:
  - High Density Deposited and Thin Film Dielectric Coatings
  - Low-K Dielectrics for High Frequency Applications
  - Integrated Thin Film Passive Logic & Thick Film Polymeric Sensors

- Laminate versus Ceramic Substrate Performance Evaluation and Usage Guidelines
RESEARCH DIRECTIONS FOR HDPs: MULTICHIP MODULES (MCMs)

PROBLEM EXAMPLE

DS1 Ion Propulsion System Packaging Challenges

- Stacked HDPs (MCM): Layers Connected with Vertical Gold Fiber in Silicone Polymer

- During Environmental Testing:
  Developed a Permanent Cold Set Which Led to Intermittent Opens between Layers

- Dropped Use of the Stacked HDPs (MCM)
RESEARCH DIRECTIONS FOR MICROELECTROMECHANICAL SYSTEMS (MEMs)

- Failure Mechanisms as a Function of Design, Materials, and Mission Length

- MEMs Materials Usage Mission Length & Environment Guidelines

- Critical Points for Inspections & Process Controls for MEMs Manufacturing

- Non-invasive Inspection & Test Methods for MEMs Manufacturing and Final Products

- System Level Quality & Reliability Methodology Development
RESEARCH DIRECTIONS FOR PHOTONICS


• Space-ready Single-Mode Microwave Fiber Optic Link Qualification

• Frequency Shifter Qualification

• Integration and Validation of Optical/Electronic Back Plane for Electro-optic Assemblies

• Evaluation of -80° C to +85° C Range Fiber Optic Cable
RESEARCH DIRECTIONS FOR MATERIALS

- Analysis of Adhesion/bonding Techniques to Characterize Short & Long Term Performance
  - Long Term Environmental Exposure Aging of Bonding Materials

- Evaluation of Test Results for Eutectic, Diffusion, Epoxy, Interdiffusion, Braze, and Solder Adhesions/bonds
  - Correlation of Results with NDE Such as Ultrasonic Holography

- Correlation of Materials, Manufacturing Processes, and Defects to Bonding & Overall Product Reliability
  - Effects of Partial Bonding
• Application of Thermoset Adhesives
  ▪ Epoxies Cured at Room Temperature
  ▪ UV & Other Radiation Cures
  ▪ Low Dose X-ray Cures

• Evaluation of Conformal Coatings which Penetrate Beneath Components without Volatile Solvent Carriers
  ▪ Rework
  ▪ Removal Using Micro-CO₂ Blasting

• Higher capacitance, high K materials
  ▪ Relaxer dielectrics
  ▪ Improved frequency response
• Resolution of No-Clean Fluxes & Solder Paste Issues
  ▪ Electrical Interference of Residue
  ▪ Interference with Conformal Coating
  ▪ Undetected Solder Balls
  ▪ Fluxless Solder Attachment in Nitrogen/Argon Atmosphere
  ▪ Validation of aqueous flux use

• Encapsulants & Coatings Which Do Not Require High Temperature Curing
  ▪ Meeting NASA Outgassing & Adhesive Requirements
    NASA JSC SP-R-0022A