Integrated Avionics System (IAS), Integrating 3-D Technology On A Spacecraft Panel

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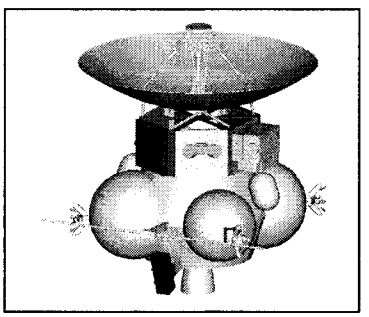
Abstract

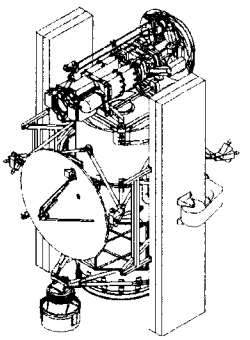
As spacecraft designs converge toward miniaturization, and with the volumetric and mass challenges placed on avionics, programs will continue to advance the "state of the art" in spacecraft system development with new challenges to reduce power, mass and volume. Traditionally, the trend is to focus on high-density 3-D packaging technologies. Industry has made significant progress in 3-D technologies, and other related internal and external interconnection schemes. Although new technologies have improved packaging densities, a system packaging architecture is required that not only reduces spacecraft volume and mass budgets, but increase integration efficiencies, provide modularity and flexibility to accommodate multiple missions while maintaining a low recurring cost. With these challenges in mind, a novel system packaging approach incorporates solutions that provide broader environmental applications, more flexible system interconnectivity, scalability, and simplified assembly test and integration schemes. The Integrated Avionics System (IAS) provides for a low-mass, modular distributed or centralized packaging architecture which combines ridged-flex technologies, high-density COTS hardware and a new 3-D mechanical packaging approach, Horizontal Mounted Cube (HMC). This paper will describe the fundamental elements of the IAS, HMC hardware design, system integration and environmental test results.

Introduction: The advent of small, low-cost space missions, has brought with it a need for new, advanced technologies, which can enable missions to utilize smaller launch vehicles and lighter payloads. The Advanced Deep Space System Development Program (ADSSDP), is comprised of three elements: Outer Planet Technology (X2000), the Center for Integrated Space Microsystems (CISM), and Advanced Radioisotope Power Source Program (ARPS). This makes up part of the Outer planets New Millennium Program (NMP), a National Aeronautics and Space Administration (NASA) initiative for a new class of smaller missions.

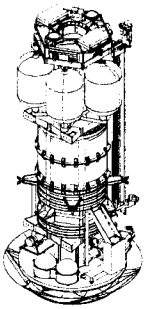
The principle objective of the program is to provide an engineering model of the spacecraft system by the year 2000. The engineering model, dubbed the X2000, is the basis for the first series of missions. The program will continue to advance the "state of the art" in spacecraft system development with new engineering model every three years to benefit the missions that follow. Two of NMP's currently targeted interplanetary missions are the ST4/Champollion - a Comet Lander, and a Europa Orbiter. The scheduled launch periods for those missions are April 2003 and November 2003, respectively. These missions are incorporating the X2000 avionics architecture.



Europa



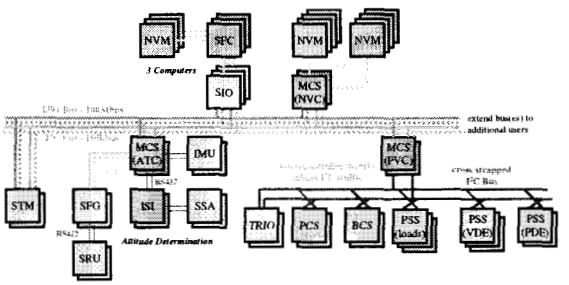
ST4 Carrier



ST4 Lander

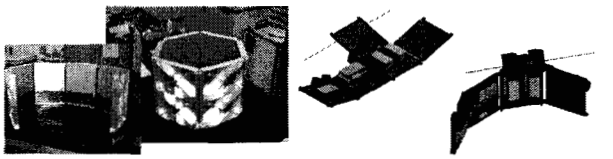
Architecture: The combination of the New Millennium packaging technology with the X2000 system architecture will produce a product capable of meeting a wide range of mission requirements with a low system recurring cost. The architecture is capable of integrating different instruments, propulsion modules, power sources and telecommunication into a multiple mission platform. The goal is to develop and validate a modular building block design with standard interfaces, enabling this high level of integration with the foresight for future systems on a chip.

The electrical mechanical architecture is configured to accommodate three different bus configurations. A PCI Bus to handle the high speed Command and Data Handling functions. Signals are propagated across a Z-axis connection system. (Described in the mechanical architecture). The 1394 "firewire" Bus will provide the high data rate for science data acquisition. A third bus, I2C, is a low power bus that is used to accommodate power switching, pyro and temperature sensor interfaces.

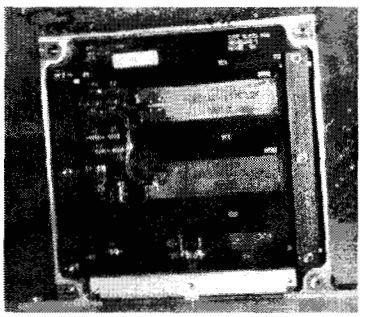


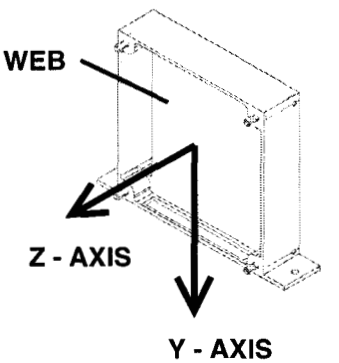
Both the 1394 and I2C signals propagate through an Y-axis connection system, and across an embedded bus which replaces the traditional spacecraft harness. (Both connection systems are described below.)

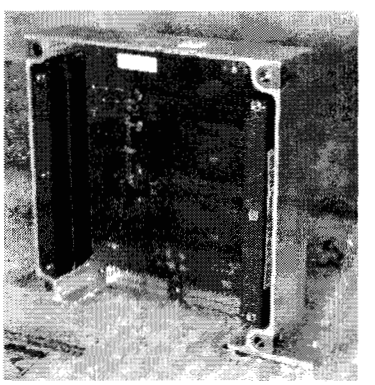
The mechanical architecture takes advantage of the technology synergism of the 3-D stack design developed for the X33 and Deep Space 1 programs. The mechanical configuration is made up of three major components. The Horizontal Mounted Cube (HMC), houses the command and data handling, power and attitude control electronics. The Embedded Bus, provides the system interconnectivity for the spacecraft. The third component, made up of a structural panel, integrates all three components. This structure is a load-carrying member of this system, and is used to conduct heat from the HMC to its radiative surface.



Features incorporated in this panel, provide access to the backside of the embedded bus, which maintains rework capability. Interchangeability between engineering or flight subsystems, which provides flexibility for the system design team to develop a spacecraft configuration independent of the Avionics. These components create the Integrated Avionics System (IAS). A unique multi-configurable system, which is designed across several engineering disciplines. The mission design, and the spacecraft, is optimized to reduce the workload and shorten the development, integration and test activities.



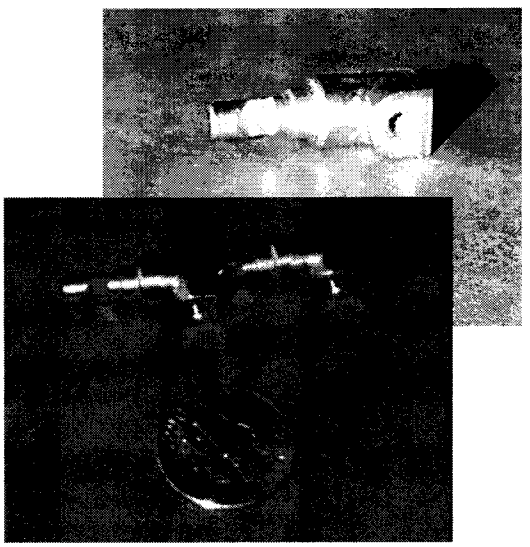




Key Technology Development: The Horizontal Mounted Cube (HMC) implements a packaging architecture that strives for modularity between subsystems, and scalability, by orientating frames, termed slices, mounted horizontally as opposed to the traditional vertical mounting. Each slice is made up of a 4.0 in ^{2} x 0.50-inch aluminum frame, machined to create a cavity and two mounting feet. The slice width's can accommodate three configurations: A singlewide version, a doublewide and a double-sided version.

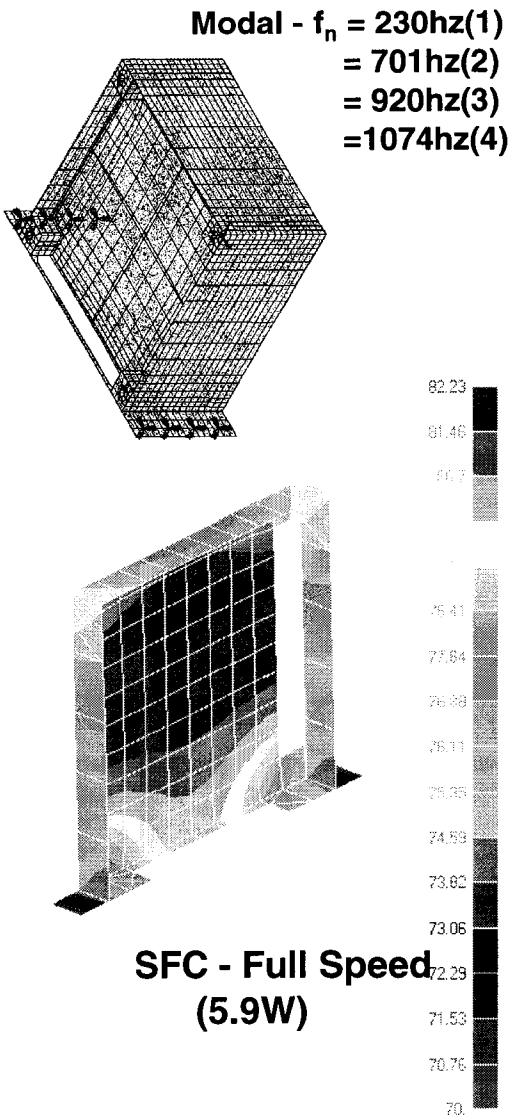
The machined cavity in the frame forms a web. The web serves three functions. First, provides for the attachment of the printed wiring board assembly (PWBA), second as a thermal conduction path. Third, two openings are incorporated along two edges, which provide for the z-axis connections between adjacent slices.

Each slice is captured to the adjoining slice using a guide pin retention design. This device acts as a guide for aligning adjacent slices. Clamping is achieved with a #4-40 set screw, which rides on a machined incline. Four guide pin - retainers are located on each slice, one in each corner. The combined clamping force can be well over 100 pounds depending on the screw torque.



The design becomes scaleable by adding any number of additional slices to maximize mechanical spacecraft constraints for a centralized architecture or as few as four slices for a distributed system. In reverse, slice removal is accomplished by removing its associated four setscrews, on both adjacent slices, and sliding away the slice to removed. This eliminates disassembly of the entire module and only effects the associated slice.

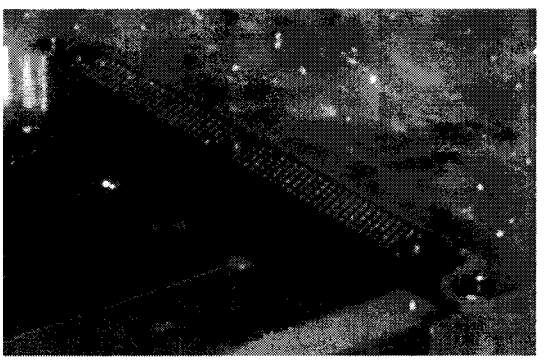
With the slices mounted in a horizontal configuration, the two mounting feet, machined as part of the frame, provide the dynamic and thermal paths for each slice. The web, described earlier, provides for the attachment of the printed wiring board assembly is done using a film adhesive by ABLESTIK. This film adhesive serves two roles. Its thermally conductive, specifically designed for bonding materials with mismatched coefficients of thermal expansion. Its conductivity of 0.87W/m ^{0} C, provides the medium for conducting the heat from the printed wiring board assembly to the web. The combined properties of the printed wiring board, the high bond strength with low shear modulus of the bond, and the size of the web, create a system capable of natural frequencies approaching 1000 hertz.



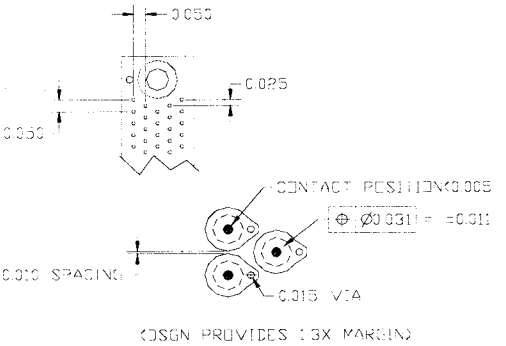
Since the HMC design provides for a two-axis interconnection scheme. The relationship between the printed wiring board (PWB) and the four guide pin-retainers plays a key role in the alignment relationship between slices and between slices to the embedded bus. The PWB is located within +/- 0.010-inch true position of the guide pin-retainers. This is accomplished with a process developed for the Mars pathfinder design. The tooling is designed to provide PWB to frame alignment and seconds as a bonding fixture. The fixture, frame, and PWB are laminated together under pressure and temperature.

The slice to slice, and slice to embedded bus, connectivity are accomplished using COTS hardware. Two Cinch CIN-APSE, 248 contact high-density solderless connectors are used for the z-axis, or slice to slice connection. A Teledyne Kinetics 112 contact high-density solderless connector is used for the y-axis, or slice to embedded bus connection. Both were selected for their $-100\ ^{0}C$ plus, cold temperature capability.

The Cinch connector shown in the following picture is made up of a "plunger / fuzz-button / plunger" construction. Mounts on the component side of the PWBA, with three 2mm flat head screws. The frame and PWBA construction allow the connector to extend above the assembly. When joining slices are mated together, the Cinch connector protrudes through the opening in the adjacent web and makes contact with copper and gold plated pads on the opposing slice or PWBA. Alignment between adjacent slice is provided by the close tolerance of the guide pin – retainer design. The tear shaped copper and gold contact pads are designed to accommodate any additional misalignment concerns. This pad also provides the inner board layer connection with via's located within the pad design.



The Teledyne connector shown in the next photo is a right-angled connection system. Its



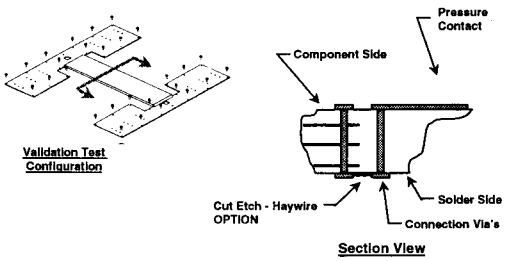
uniqueness comes from its ability to make two perpendicular solderless connections. The one edge of contacts mounts to the component side for the PWBA, and is captured in place using three 2-56 flat head screws. The connector aligns its self to the bottom edge of the frame using a guide pin built into the connector and self-aligns to a mating hole located in the PWBA. The connector is positioned to straddle the mounting feet. The perpendicular contacts provide the connection to the embedded bus. This creates a third axis I/O capability, which enables the HMC to become a plug and play architecture.

Per slice I/O capability in the current configuration is 608 connections, with the maximum contact count of 856. Both connectors have current carrying capability of 3 amps. This makes the power system robust and maintains design flexibility.

Embedded Bus Technology: The system interconnection design for the IAS creates the ability to interconnect components in all three dimensions without the use of a conventional harness. Yet providing a unique approach for maintaining system level rework capability.

The embedded bus incorporates three key design features. 1. The electrical approach for accommodating the 1394 Bus signals. 2. Provides for a reliable mechanical alignment design between the y-axis connector and the embedded bus. 3. Develop a

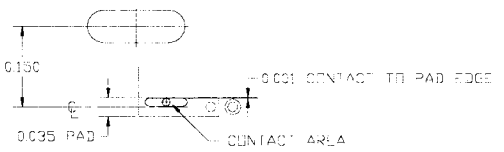
method for maintaining rework capability at all levels of integration.



The interconnection approach incorporates a standard polyamide, multi-layer, ridge-flex construction. The configuration provides for a twenty four-slice HMC assembly, logic to drive the 1394 bus and panel to panel interfaces. Twenty-ones of the twenty-four slices make up the y-axis interface to the 1394 and I2C Bus. IPC-D-317, design guide lines for high speed techniques was used to implement the 1394 bus signal propagation. The two approaches selected, incorporated a coincident straight and parallel pair schemes. These methods satisfied the capacitance requirements of an equivalent 1394 twisted shield pair system.

The mechanical alignment between the HMC's y-axis connector and the embedded bus is confined only to the relationship between the connectors centering pin and the circuit pad configuration on the bus. This is defined as the short axis or pitch of the connector contacts. The pad design provides for the appropriate pad width to accommodate the worst case slot edge to pad edge tolerance of +/- 0.009 true position. Well within PWB manufacturing tolerances.

SHORT AXIS TOLERANCE

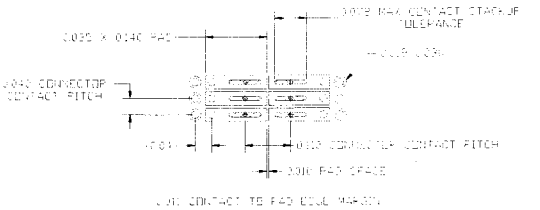


The total HMC slice to slice tolerance stack up defines the long axis tolerance. The pad design provides for the appropriate pad length to accommodate the worst-case tolerance build up of the 24 slice configuration. The long axis control only requires positional control to a selected slice. The circuit pads and HMC mounting hole provide for the balances of the tolerance.

System Integration: The HMC module assembly is lowered onto the bus relying on the y-axis center pin to guide the y-axis contacts to the circuit pads on the bus. The IAS now a completed testable subassembly. All signals are accessible through the panel. The panel is integrated to the spacecraft.

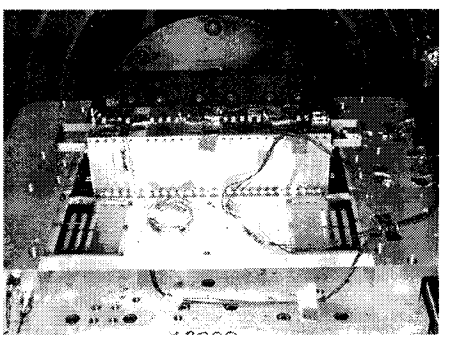
Validation Test: Dynamics and thermal test were performed to ensure that the X2000 baseline packaging techniques are structurally sound, provide sufficient thermal dissipation, and transmit electrical

LONG AXIS TOLERANCE



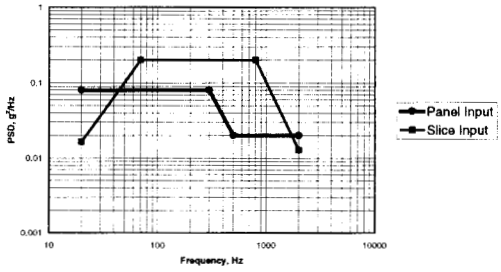
signals adequately based on flight predicted operating extremes.

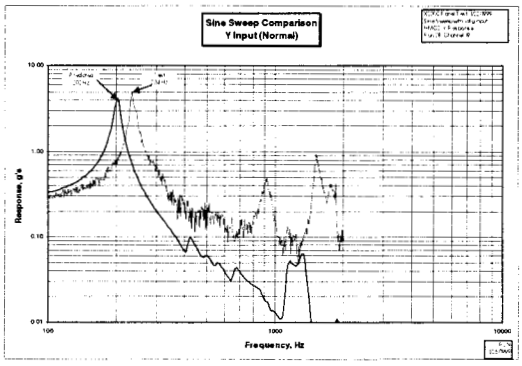
The dynamics test included instu testing of the Y and Z-axis connectors. Eight circuit paths threaded through over 11,000 pin contacts covering 91% of the total I/Os in the system. The IAS was instrumented to detect open pulses within 11ns. The primary testing was high-level random, augmented by low-level sine sweep for model correlation and detection of changes in response along with simulated pyrotechnic shock. The input levels shown are inputs to the panel.



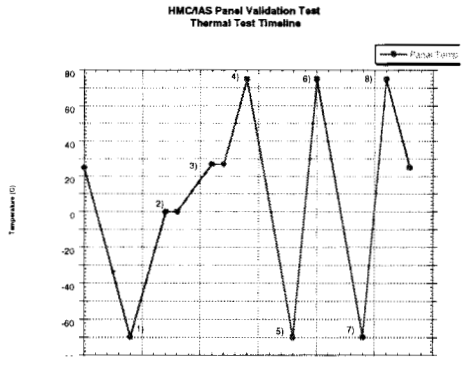
A simple finite element model of the panel was used to estimate the response of the panel and the electronics module. Since the electronics module was relatively stiff compared with the panel, the electronics module was simply modeled as a rigid body. This simplified model provided a reasonable

estimate of the module response, as shown in this plot of the measured and predicted response on the electronics module normal to the panel for a low level (¼ g panel input) sine excitation.





Thermal vacuum test was performed over a 3-day period in February 1999. The main objectives of the test was to: 1) verify electrical continuity of the Y-axis & Z-axis connectors as the entire panel was cycled 3 times over the qualification temperature range of -70°C to +75°C. 2) determine the thermal performance of the prototype panel by measuring the temperatures of the panel and avionics slices at two different 3-D stack power levels (nominal and high).



A thermal test timeline indicating the temperature of the slice-to-panel interface during the entire test is shown in the figure above. The test began with a cold qualification test point (at -70°C), continued with two steady state performance test points (at stack power levels of 19W and 57W) and finished up with the remaining 3 temperature cycles between 75°C and -70°C.

The thermal performance of the 3-D stack and the IAS panel in the test agreed fairly closely with thermal analysis predicts. The analytical thermal model predicted the actual slice interface temperature within 10°C in the nominal power case and within 1°C in the high power case. Adjusting the longeron-to-panel thermal conductance in the model will improve model predictions. The maximum temperature rise from the slice interface to the middle of the flight computer PWB in the high power case (for a slice dissipation of 8.0W and a stack dissipation of 57W) was 20°C. The maximum flight computer PWB temperature in this case was 43°C. The 3-D stack and the IAS panel have been proven to efficiently reject heat to an external environment sink.

Conclusion: The dynamic and thermal environmental tests performed, validated that packaging design can meet or exceed predicted performance. The instu dynamics test results indicated no opens during the entire test duration, and the thermal vacuum test proved the 3-D stack and IAS design have been proven to efficiently reject heat to an external environment.

The ADSSDP packaging architecture maintains a level of flexibility that can be customized to create both a central or distributed system. The three dimensional solution provides a more flexible system interconnectivity, scalability, and simplified assembly test and integration options. The low-mass modular design combines high-density packaging techniques, COTS hardware, along with standard technologies to create a product flexible to accommodate multiple missions.

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