

# **Advanced Packaging Technologies used in NASA's 3D Space Flight Computer**

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## **Abstract**

*During 1995-1997, NASA's New Millennium Program developed the 3D Flight Computer technology for validation on its first Deep-Space 1 mission launched in October 1998. Whereas, the computer was not delivered on schedule for inclusion on the spacecraft, it was delivered, integrated and space qualified at JPL. This computer is characterized by the aggressive use of advanced packaging technologies: 3D chip stacking, multichip modules, and 3D MCM stacking. This development represents an important technology milestone towards the further miniaturization of all spacecraft avionics into an integrated architecture.*

**Keywords:** 3D packaging technologies, flight computer, avionics.

### **1. Introduction**

Starting in the early 90s and throughout the decade, NASA has initiated a series of research tasks as well as flight projects with the specific focus on advanced packaging technologies for the miniaturization of spacecraft micro-electronics. In this paper, we describe in more detail one such effort by a consortium of government, industry and academia. The consortium developed the 3D Flight Computer as part of NASA's New Millennium Program (NMP) Deep-Space 1 (DS1) mission, which was launched in October 1998.

Unfortunately, due to schedule problems, the 3D Flight Computer did not get included on the DS1 spacecraft, and was replaced by an off the shelf flight computer. However, all of the qualification steps required for flight launch were performed on the flight computer engineering models (two of them) which were integrated and tested at JPL.

In this paper, we describe the packaging technologies included in the design of the 3D Flight Computer. They include a) advanced chip stacking technologies

into 3D die-cubes; b) multichip module technologies (MCM); and c) stacking of MCMs into a stacked 3D architecture. Qualification steps have been performed on all three selected technologies. Moreover, as part of the broader qualification approach we have developed extensive analytic models as well as mechanical test verification vehicles to fine tune the analytic models.

This paper is outlined as follows. First we give a broader picture of recent efforts at NASA's Jet Propulsion Laboratory to develop and insert advanced packaging technologies into deep space missions (flight projects). This process, as will be discussed in Section 2, can be characterized as very difficult and slow. Following this, we describe in detail the 3D Flight Computer architecture in Section 3, and packaging technologies in Section 4. Our concluding remarks are described in Section 5.

## 2. Advanced Packaging Technologies for Deep-Space Systems

The following is a list of deep-space projects at JPL that have recently been developing or using advanced packaging technologies for avionics miniaturization.

- Advanced Flight Computer (AFC), 1992-95, and flight experiment in 1996;
- Mars Environmental Survey (MESUR) Network study in 1993;
- Mars Pathfinder Flight Computer, launched in 1996, landed on Mars in 1997;
- New Millennium Deep Space 1 3D Flight Computer, 1995-97, delivered but no flown;
- Space Cube architecture, 1995-96, delivered for flight on X33 in 1999;
- X2000 First Delivery Project Horizontally Mounted Cube (HMC), 1997-98, descoped.

The Advanced Flight Computer (AFC) research task was the first at JPL to pursue an aggressive multichip module packaging approach [1]. JPL developed, in partnership with TRW, a 32-bit flight computer with 33 die packaged in a single large multichip module (4 by 6 inches AIN package), to include: the CPU, FPGAs, EEPROMs, and 20 SRAMs stacked 2-high. The MCM silicon substrate and die-stacking was performed by nCHIP. This module was also developed into an Advanced Packaging Experiment and launched on the SSTI spacecraft in 1996. The spacecraft unfortunately failed soon after launch.

In 1993, NASA performed its first comprehensive study of the benefits of advanced packaging technologies on the complete spacecraft system, as part of the planned Mars Environmental Survey Network mission [2]. 3D MCM stacking approaches were considered from TI, Honeywell, and GE for all spacecraft digital avionics. The study quantified at the system level the 'ripple-effect' from the reduction of the avionics mass, volume, and power, which gave a strong incentive for the use of advanced packaging technologies. Meanwhile, Lockheed Martin developed the Mars Pathfinder 32-bit, RAD6000 VME single board computer with commercial DRAMs stacked 4-high for a total of 128 Mega Bytes in two hermetic modules. This computer was later used by the NMP/DS-1 as a replacement for the 3D Flight Computer.

Two additional efforts have been made towards higher system level integration using advanced

packaging. Bolotin at JPL developed the Space Cube architecture [3], and Hunter the Horizontally Mounted Cube (HMC) [4]. The Space Cube is unique in its use of stacked square modules to provide a rich set of inter-slice interconnection strategies. It was delivered as an experiment to the X33 Reusable Launch Vehicle for sub-orbital flight in 1999. The HMC approach was developed by the X2000 project to integrate all digital and analog avionics into a common architecture tightly coupled to the spacecraft bus. Unfortunately, this exciting technology was 'descoped' in favor of the standard Compact PCI backplane architecture.

Despite many attempts at JPL to develop, integrate and deliver advanced packaging technologies to flight projects, this process still remains very difficult. Some of the roadblocks include: complexity of integration and test, and the lack of a commercially supported advanced packaging standard which can also be applied to space.

## 3. NASA's 3D Flight Computer

The New Millennium Program developed the 3D Flight Computer, in partnership with industry and academia. From industry, Lockheed Martin developed the computer and local memory module (slice); TRW the non-volatile memory slice; Boeing the I/O module; and Space Computer Corporation developed the 3D MCM stacking architecture [5-6]. From academia, Georgia Tech developed the 3D MCM stack testability approach [7]. This group was part of the broader Integrated Product Development Team (IPDT) which included the Air Force Research Labs (AFRL), Sandia National Labs (SNL), MIT Lincoln Labs, and other industry members such as Honeywell, Hughes, etc. The flight computer architecture is shown in Figure 1 below. Also shown in Figure 1 are the two flight experiments which were actually delivered on time, and flown on DS1: the ultra low power, and the Power Activation and Switching Module (PASM) experiments. The 3D flight computer is unique in its aggressive pursuit of several new approaches.

1. Advanced packaging technologies: chip stacking, MCMs, and 3D MCM stacking
2. Use of exclusively commercial off the shelf interfaces: VME, PCI, 1773, JTAG
3. Use of high-bandwidth interfaces: local memory PCI, PCI/VME, 20 Mbps 1773.

Higher level of integration also enabled new software approaches; that is, the local memory module included a total of 400 Mega Bytes of DRAM storage

(320 MB data and 80 MB of error correction code) which allowed for more memory-intensive Artificial Intelligence (AI) software to be used. Furthermore, the high-bandwidth inter-module interface allows for a scaleable, distribute fault-tolerant architecture, as opposed to a tightly coupled and cross-strapped approach.

#### **4. Computer Advanced Packaging Technologies**

The 3D Flight Computer combined a set of advanced packaging technologies available from industry, which were then integrated and space-qualified at JPL. Most of these technologies were previously developed under DOD research and development programs, and not by NASA. The packaging technologies are broadly grouped into three areas:

1. 3D chip stacking
2. Multichip modules which may include some of the 3D chip stacks
3. 3D MCM stacks with Z-axis interconnects

The primary motivation for this aggressive insertion of advanced packaging technologies is the higher level of integration resulting in the reduced system mass, volume, and power. Moreover, the 3D module stacking approach was intended to break away from the legacy approach of a backplane architecture which was bulky, power intensive, and I/O pin limited. Z-axis interconnects were to provide a more compact interconnect approach (that is, modules can be brought closer together); and provide more I/O across the complete perimeter as opposed to one side only. The main drawback of the proposed approach was due to the compressive nature of the Z-axis interconnect which made integration and test more complex. Moreover, scaleability of this packaging approach is not well understood.

#### **3D Chip Stacking**

In Figures 2-5, we show 3 different views of the 3D Flight Computer packaging approach, followed by 3 pictures of the actual computer. In Figure 3, one can clearly see five 3D memory DRAM cubes. Each cube consists of a stack of 48 DRAM die. Since 16 Megabit die were used, and 40 of the 48 die are actually connected (the rest are spares determined after assembly), each cube represents a total of 80 Mega Bytes of local memory. Such a dense packaging approach is still unprecedented even in the commercial world. Thus, the single local memory slice represents a total of 400 Mega Bytes of local DRAM storage. 80 Mega Bytes are used for error

detection and correction code, leaving 320 Mega Bytes as the effective program storage size. Each DRAM cube has a DRAM control ASIC attached to the bottom of the package.

3D chip stacking is also used in the non-volatile memory module using 4-high stacks of 16 Mega bit Flash memory. The total size of the non-volatile memory module is 128 Mega Bytes. TRW, the provider of this memory module, stacked packaged parts as opposed to bare die, using the STAKTEK approach.

#### **Use of MCMs and 3D MCM Stacks**

An early-on requirement of the packaging approach was to allow the 3D integration of different forms of MCMs. Therefore, as proposed by Space Computer Corporation (SCC), an MCM is integrated onto a printed circuit board which has provisions for 3D interconnects. The MCM can be either mounted directly onto the PCB or recessed into it, with a heat-sink underneath. The heat-sink would conduct the heat to the perimeter, down the edges of the stack, and to the thermal plates underneath.

The 3D computer has a total of 4 modules integrated into the stack: 1. CPU module, 2. local memory module, 3. non-volatile memory module, and 4. the I/O module. The I/O module included the 1773 fiber-optic high-speed serial interface which is shown in Figure 2 in the bottom slice of the stack.

The Z-axis interconnect uses an elastic compliant material with wire interconnects. The elastomers are held together in ceramic holders which also define the minimum distance between the modules. This Z-axis interconnect carries all the data and control signals between slices, including the high-speed Peripheral Component Interface (PCI) running at 33 MHz and 3.3 volts rail-to-rail voltage.

#### **Qualification Results**

The engineering module flight computer integrated at JPL was space qualified, including the following tests:

- random vibration showed no electrical or mechanical failures;
- thermal vacuum testing validated the thermal analytic models, and showed no electrical or mechanical failures;
- thermal cycling exposed some of the more difficult problems at low temperatures (-26 degree Celsius) which required that new

elastomeric materials be evaluated. The choices that were evaluated included single and double row ETI, and Ampliflex. The ETI materials showed open electrical connections at low temperatures which disappeared at higher temperatures. The Ampliflex material, however, was operational in the -50 to 80 degrees Celsius temperature range, and was thus selected as the elastomeric material for flight.

- accelerated aging: the Ampliflex material showed no opens after a temperature soak at 150 degrees Celsius. The ETI material displayed both opens and higher resistance at higher temperatures (soak at 125 degrees C).

## 5. Conclusions

NASA's New Millennium Program developed the 3D Flight Computer for validation on its first flight, the Deep Space 1 mission. This computer is characterized by advanced technologies, including an aggressive insertion of advanced packaging technologies. Unfortunately, the 3D Flight Computer was not delivered on schedule for insertion into the spacecraft. However, the computer was integrated and qualified at JPL for use in deep-space. Advanced packaging technologies included the use of 3D chip stacking, use of MCMs, and 3D MCM stacking into a highly integrated stacked architecture.

## 6. References

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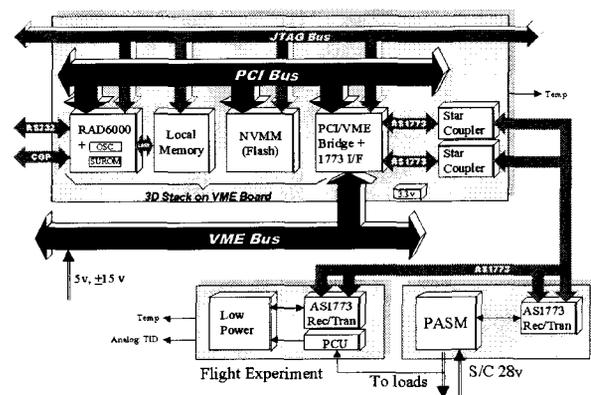


Figure 1: Microelectronics NMP-DS1 Block Diagram

# 3-D Stack with Side Plates Removed

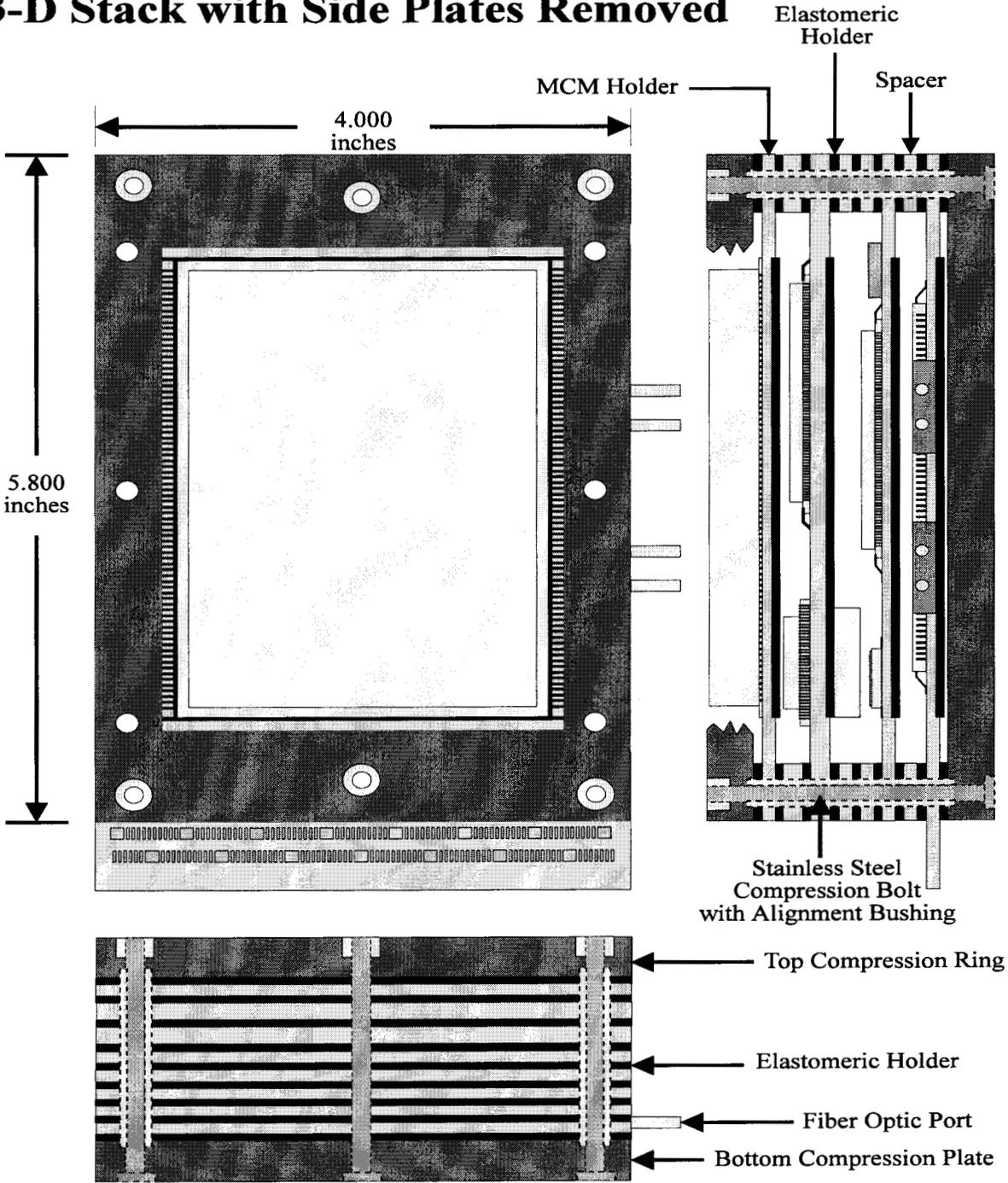
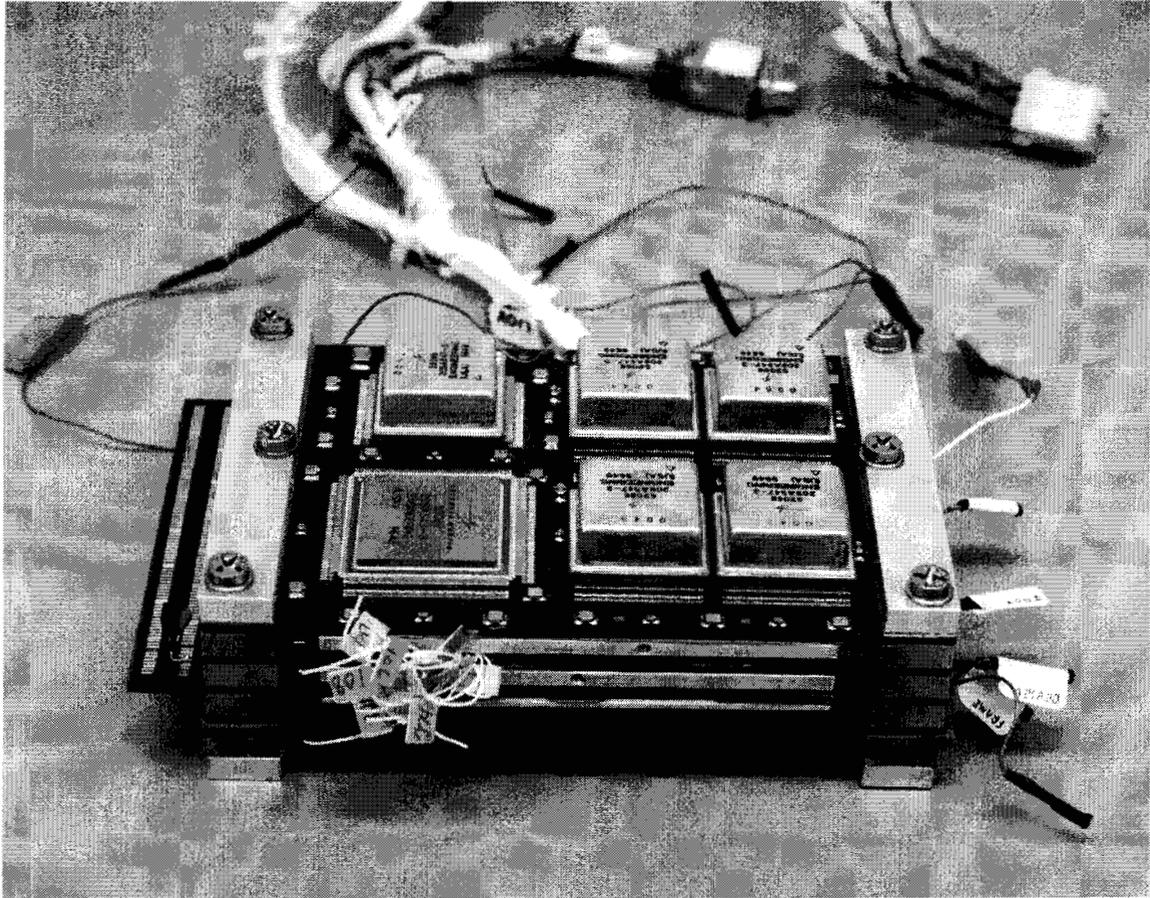
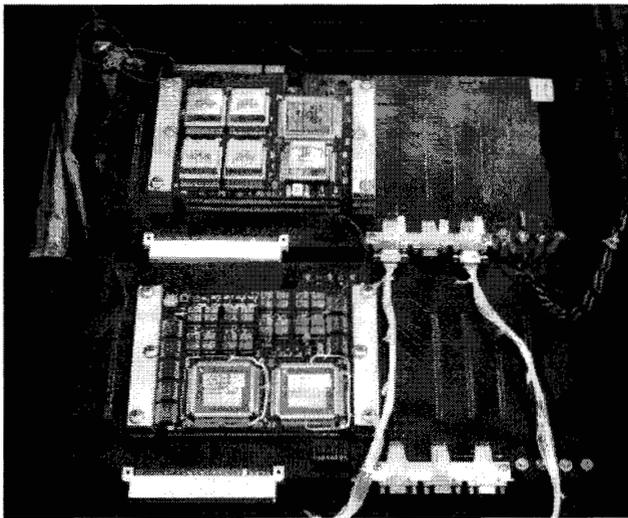


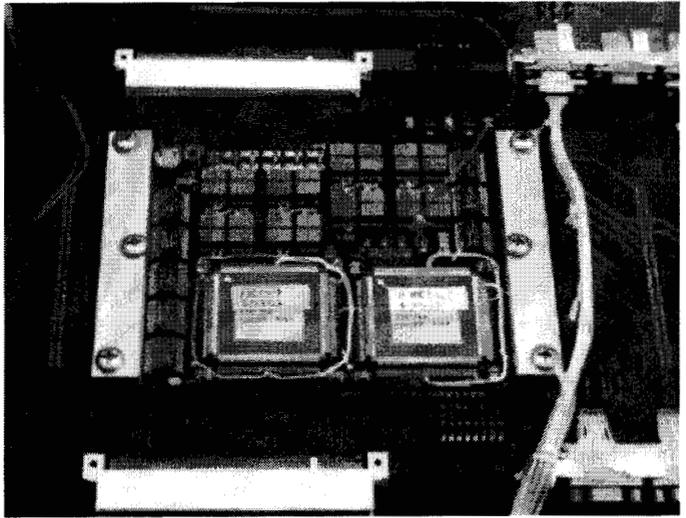
Figure 2 - 3D Stack with Side Plates Removed



**Figure 3 - 3D Flight Computer**



**Figure 4 - Slices of 3D Flight Computer**



**Figure 5 - Slice of 3D Flight Computer**