

Two-dimensional Active Pixel InGaAs Focal Plane Arrays

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ABSTRACT

Switching and amplifying characteristics of a newly developed two-dimensional InGaAs Active Pixel Imager Array are presented. The sensor array is fabricated from InGaAs material epitaxially deposited on an InP substrate. It consists of an InGaAs photodiode connected to InP depletion-mode junction field effect transistors (JFETs) for low leakage, low power and fast control of circuit signal amplifying, buffering, selection and reset. This monolithically integrated active pixel sensor configuration eliminates the need for hybridization with a silicon multiplexer, and in addition, allows the sensor to be front illuminated, making it sensitive to visible as well as near infrared signal radiation. Adapting the existing 1.55 μm fiber optical communication technology, this integration will be an ideal system of optoelectronic integration for dual band (0.5-2.5 μm , Visible/IR) applications near room temperature, for use in atmospheric gas sensing in space and target identification on earth. In this paper, 4x4 test arrays will be described. The effectiveness of switching and amplifying circuits will be discussed in terms of circuit in preparation for two dimensional InGaAs active pixel sensor arrays for applications in multifunctional, transportable shipboard surveillance, night vision and emission spectroscopy.

Keywords: Two-dimensional, Low power, Dual (Visible/IR) responses, InGaAs PIN, InP JFETs.

1. INTRODUCTION

Efforts to combine the InGaAs PIN photodiode detector technology on InP substrate with the InP JFET technology¹⁻² for monolithically integrate detector arrays and readout circuits were made. The monolithically integrated sensor array with active pixel readout technology has been recognized as the future space mission technology of a miniaturized smart imaging system. This array eliminates the need for hybridization with a separate silicon readout chip. The Jet Propulsion Laboratory has been working with Sensors Unlimited of Princeton, New Jersey to produce such a sensor for a low leakage, low power mobile imaging system. This monolithic sensor array is front-illuminated, providing near-IR to visible response. It largely eliminates the problem of the high charge transfer efficiency, allowing the construction of large yet highly reliable Infrared focal plane arrays (IR FPAs). It can make use of high electron mobility at near room temperature inherent in InP JFETs to enable readout speeds unobtainable in a silicon readout.

IR FPAs have a wide range of industrial, scientific, and military applications.^{3,4} In general, an IR FPA consists of an array of infrared-sensitive photodetectors and associated readout electronics capable of converting, amplifying, buffering and multiplexing the signal charge from detector arrays. In a typical IR FPA array, the detector is fabricated from a narrower bandgap film in a III-V or II-VI material. For example InGaAs is epitaxially deposited on the front surface of a wider bandgap substrate, such as InP. This diode array chip is then "flipped" and bump-bonded with the patterned surface down, and the substrate up to a separate readout chip. This readout chip is almost always formed from silicon CMOS because of the high maturity of this silicon technology. Silicon circuits of great complexity can easily be designed and simulated since highly sophisticated design tools are available for this purpose. Commercial foundries are available to produce the chips at a relatively low cost with high yield. This hybrid structure, consisting of a diode array chip bump-bonded to a silicon CMOS readout, has worked well and has been exploited in IR FPAs spanning the wavelength ranges from 100 to 1 μm .

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However, this approach is not without its problems, and there is a need to explore alternatives. First, the hybridization adds steps to the sensor fabrication sequence that are expensive and sometimes challenging. Second, the coefficient of thermal expansion (CTE) of silicon is anomalous with respect to virtually every other semiconducting materials system. Since IR FPAs usually must be cooled for optimum performance (in order to reduce dark current), this difference in CTE causes a mismatch in the thermal expansion between the detector and readout chips, straining the electrical bonds between the chips. While the use of soft indium bumps has helped accommodate this strain, the CTE mismatch limits array sizes and reduces reliability, if thermal cycling is involved.

Perhaps more importantly, the standard hybrid approach is necessarily a back-illuminated design, and incoming optical radiation must pass through the substrate of the detector array. The bandgap of the substrate material then sets the short wavelength cut-off of the detector unless the substrate can be removed after hybridization. In sensors where removing the substrate is not cost-effective or practical, the hybrid approach severely limits the wavelength range of sensitivity.

Several developments in electro-optics have occurred that can be leveraged to take a new approach to IR-FPA structure. First, InGaAs sensors on InP substrates have been developed as an alternative to shorter wavelength HgCdTe. InGaAs provides a barrier equal to the full bandgap, as opposed to the midgap barrier in a metal gate transistor (MESFET).⁵⁻⁶ This greater barrier provides a wider logic swing for digital logic as well as reduced gate leakage for analog circuits. InGaAs, with a cut-off wavelength of 1.7 μm , is lattice-matched to InP and has been used to make high quality area arrays. By using super-lattice techniques to relieve the strain due to lattice mismatch, strain relaxed detectors of pure InAs on InP have also been demonstrated. These extend the cutoff wavelength to approximately 2.5 μm . InGaAs photo-detectors with InGaAs JFETs on InP have also been developed, principally for high speed communication applications.

An active pixel image sensor of InGaAs PIN which is monolithically integrated on an InP JFET was described¹ elsewhere as an image sensor that has one or more active transistors within the pixel unit cell. This is in contrast to a passive pixel approach that uses a simple switch to connect the pixel signal charge to the column bus capacitance. Active pixel sensors have demonstrated lower noise readout, improved scalability to large array formats, and higher speed readout compared to passive pixel sensors. In order to utilize these advantages of the active pixel sensors however, the technology should be further improved in its stability of the circuits as well as its fill factors prior to its application to space mission systems.

In this paper, we examine the characteristics of the monolithically integrated InGaAs PIN diode sensor array (4x4) with InP JFETs source-follower per detector-readout electronics. Individual discrete devices (the InGaAs PIN photodiodes and InP JFETs) have been redesigned, fabricated and characterized for improve of the pixel fill factor. These were followed by the development of prototype test cells consisting of the readout electronics for a single pixel. Very small prototype arrays (4x4 format) have been made by combining cells, using integrated select transistors to allow multiplexing. The switching stability of these sensors is discussed relating to the profile of the zinc diffused p^+ gate layer. The success of the metal contact covering InP PIN mesa photodiodes to the switching JFETs is described in terms of the fabrication technology of planarizing of the polyimide over the PIN mesa structure prior to the processes of gold plating and ion milling.

2. EXPERIMENTAL PROCEDURES

Test circuits needed to construct visible and near infrared signal processing were redesigned, fabricated, and characterized using a test vector generator, a semiconductor parameter analyzer, and a lock-in amplifier. The cross-section, as shown in Figure 1, was based on InGaAs/InP PIN mesa diode of a height, 1.8 μm above the InP JFET platform level, applied for the focal plane array.⁴

A Be-doped (10^{18} cm^{-3} , thickness=400nm) p-InP JFET backing layer was grown onto the surface of (100) InP: Fe semi-insulating substrate using gas source molecular beam epitaxy. An S-doped ($5 \times 10^{16} \text{ cm}^{-3}$, thickness=1.0 μm) n-InP channel

and contact layer ($5.5 \times 10^{17} \text{ cm}^{-3}$, thickness=100nm) were grown for the discrete JFET control. The n-InP contact layer was followed by a thick ($1.5 \mu\text{m}$) InGaAs detector absorption layer ($n < 1.5 \times 10^{16} \text{ cm}^{-3}$) and a thick (300nm) n-InP cap layer ($2 \times 10^{16} \text{ cm}^{-3}$) in succession for the completion of the PIN photodiode structure. The p^+ -InP of the PIN photodiode contact layer and the p^+ isolation region around the perimeter of the JFETs were fabricated in a sealed ampoule diffusion at 500°C using Zn_2As_3 as the source. The InP n-channel was completely surrounded by p-type regions formed by a p layer under the channel and a p^+ wall surrounding the device perimeter. In this configuration, the depletion region pinches off the channel from both top and bottom, thereby decreasing the switching voltage by a factor of two as compared with a conventional JFET with a single gate p-n junction. There were no exposed p-n junctions.⁴ Thus any surface leakage from the side-wall of the JFET mesa was eliminated.

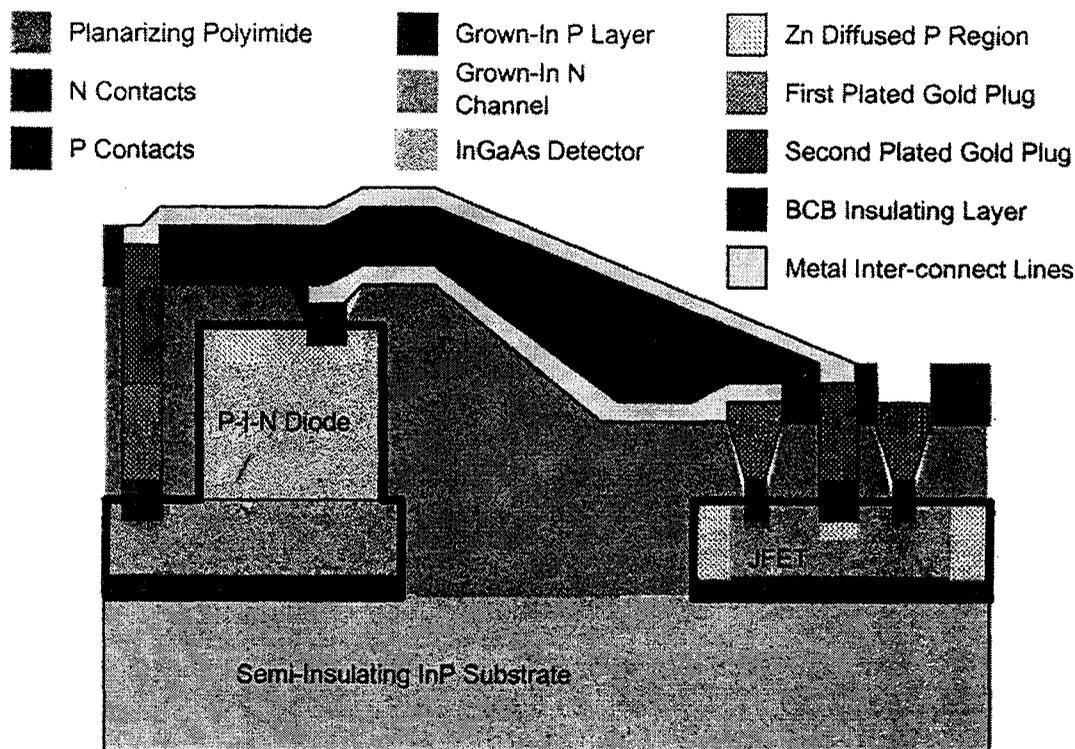


Figure 1. Cross section of the monolithically integrated InGaAs/InP PIN diode and InP junction field effect transistor platforms.

Figures 2a and 2b show an overview of the two-dimensional (8x8) InGaAs focal plane array fabricated on InP substrate and a magnified pixel with the source-follower per detector circuit, respectively.

The Reset pulse for the R_{st0} was held at 1 V until the pixel is ready for readout. Then the bias should be swung to -5 V. V_{dd} can range from 5 ~ 10V. The column driver of the C_0 for X selection was biased at 2V for the "on" state, and -5V for "off" state. The row driver of R_0 for the Y select FET and the output signal driver of the V_{in} were set at 0 V and -5 V for the "on" and "off" states respectively.

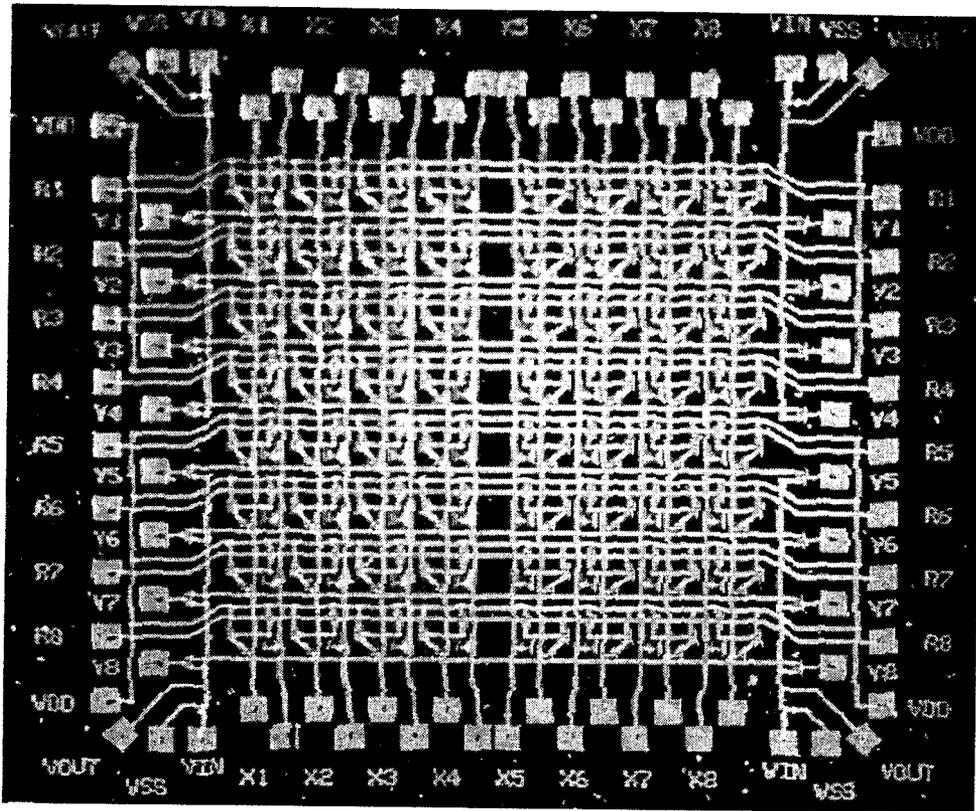


Figure 2a. An overview of the fabricated InGaAs focal plane array (8x8) on InP substrate.

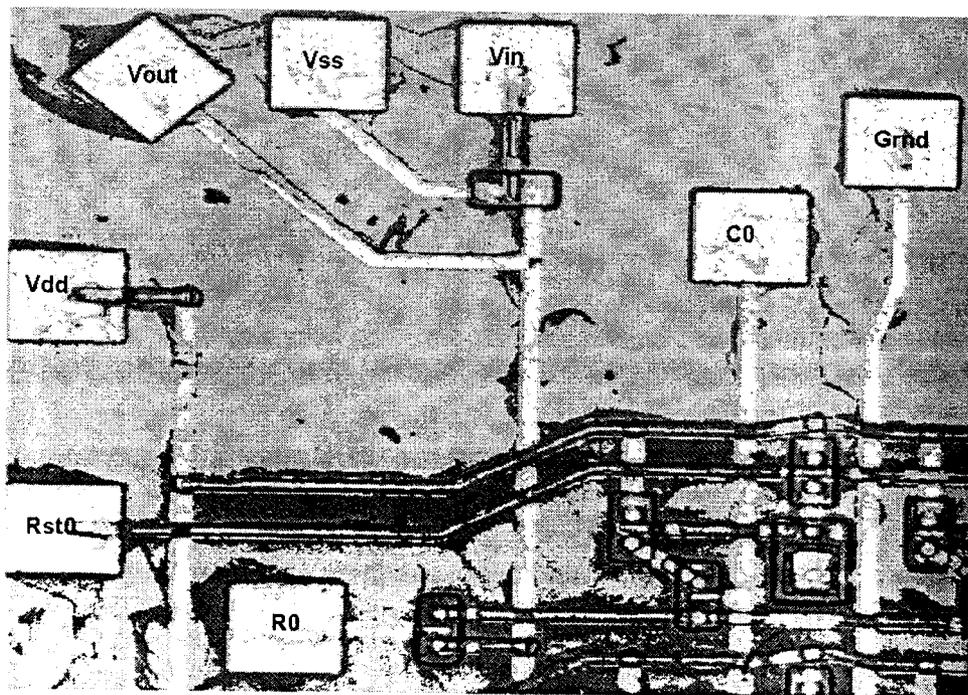


Figure 2b. A close-up view of a pixel with a source-follower per detector readout circuits.

2. RESULTS AND DISCUSSIONS

The incident light power of $59\mu\text{W}$ at 1540nm on pixels 1 and 2 show a 100mV signal corresponding to a responsivity of 1695 V/W as shown in Figure 3. The noise on the signal is $\sim 8\text{mV}$ peak-to-peak, corresponding to an rms noise of 1.33mV . The circuit's response to modulated light signals, ranging from 270 Hz to 2 kHz . This means that the noise of the pixels corresponds to $76\mu\text{V}/\text{Hz}^{1/2}$ at 300 Hz and the noise equivalent power (NEP) of $45\text{ nW}/\text{Hz}^{1/2}$. The response of pixel number 3 is about a factor of 2 less than the response of pixels 1 and 2. The trace below shows the device operated in pixel mode, where the reset FET is used as a load resistor. $590\mu\text{W}$ of light at 1540nm was focused on a single pixel. The output from the source follower was monitored on the scope. The resulting voltage shift of 150 mV corresponds to a responsivity of 260A/W . This responsivity depends upon the gate bias optimization voltage applied to the Rst0 FET, and the resulting channel resistance. Similar results were reported elsewhere in discrete JFETs with drain leakage current as low as 90 pA .⁴ The low leakage was probably due to the pinching structures both on top of and bottom of the n-channel, the completely closed side-walls of the p^- isolation layers and the lightly doped n-channel InP material.

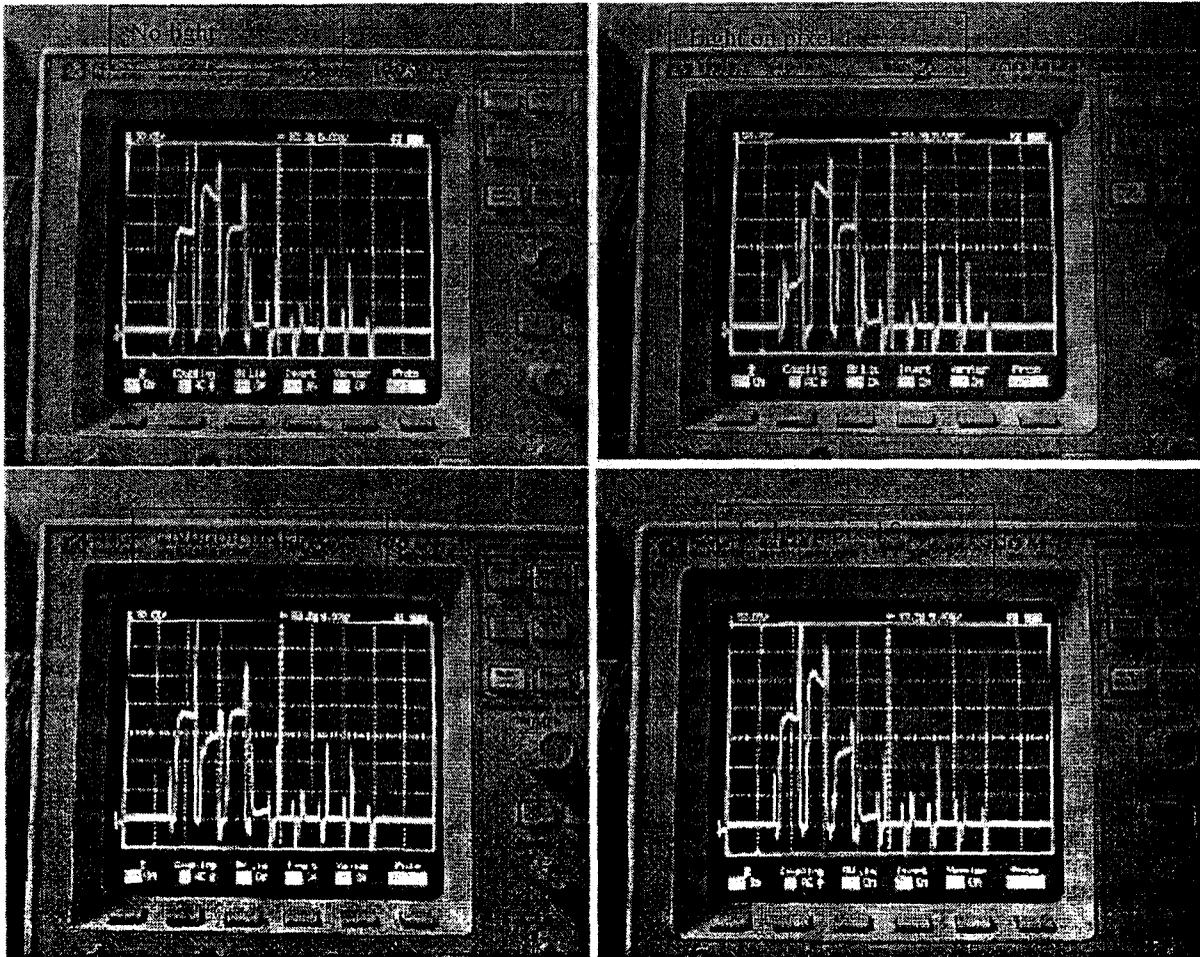


Figure 3. Pixel response of the arrays. The grid spacing is $50\text{ mV}/\text{div}$ and $5\text{ }\mu\text{sec}/\text{div}$.

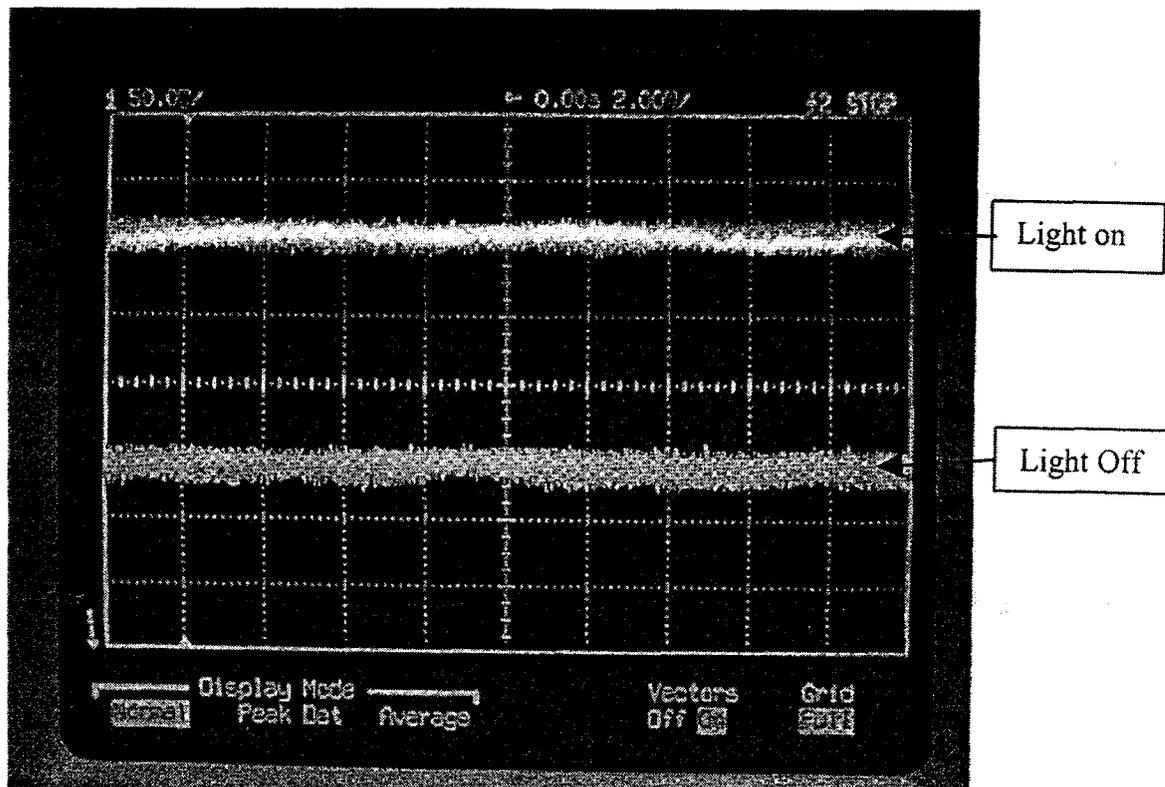


Figure 4. The responsivity and NEP of the focal plane array show 1695V/W and $45\text{ nW/Hz}^{1/2}$ at 1540 nm , respectively.

The detectivity of the hybrid InGaAs focal plane arrays (FPAs) was reported to be at least two orders of magnitude higher than that of the HgCdTe FPAs at room temperature. However, only less than 20% of the array was functional. Furthermore, the voltage swing of some failed converters appeared to be too small to utilize the component for the readout circuits. The voltage swing of some failed FET was improved more than order of two (2), yet the converter leaked severely when the reset voltage reached 1.5 V. Test results indicate that the most critical variable of the successful readout circuit was the gate dopant profile.⁷ The effectiveness of p^+ diffusion was also closely dependent upon the growing technique of the multi-layers, such as molecular beam epitaxial growth or molecular beam chemical vapor deposition. Further study is on the way to improve the metallic interconnection including the polyimide passivation layers.

4. SUMMARY

Excellent characteristics of the redesigned high fill factor InGaAs PIN integrated with JFETs SFD was achieved for the discrete components needed to construct the monolithic InGaAs PIN/InP JFET readout circuits. Fully monolithic visible/near-infrared 4×4 active pixel sensors were redesigned and fabricated for the improvement of the switching action and fill factors. In this layout InGaAs photodiode detectors can be individually controllable at each pixel level by biasing the gates of InP JFETs with a minimal voltage. The responsivity and NEP of the focal plane array at 1540 nm was found to be 1695V/W and $45\text{ nW/Hz}^{1/2}$, respectively. However, the stability of the circuit contacts should be improved further prior to space applications of these focal plane arrays. The critical variable of the readout circuits appeared to be the dopant distribution of the p^+ gate layer of the JFET switch. The step formation mechanism of the p^+ gate dopants of this material was identified in terms of diffusion element, temperature, and duration. Further study to improve the metal interconnects through and on the polyimide multilayers is on the way further improvement to raise the device reliability.

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