

Extreme Temperature (-170C to +125C) Electronics for Nanorover Operation

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Abstract— The design of the electronics control and data system for the extreme environment seen by a 1.3Kg, 1666 cubic cm nanorover is presented. The Muses-CN electronics is a low mass, low volume, low power electronics platform that must operate over the -170C to +125C temperature range and 1 AU free space radiation environment. The nanorover electronics is a 2.5 watt system that allows for 0.05 to 1 MIPS processing power and will control 10 motors for mobility and science measurements and robotic telemetry signals. Science instruments Infrared (IR) and Alpha backscatter (AXS) spectrometers along with an Active Pixel Sensor (APS) camera. Theoretical basis for a low power electronics system with space and commercial grade electronics parts operating in this temperature range is presented. System and component temperature results along with the unique packaging constraints of the Chip on Board assembly are also discussed.

TABLE OF CONTENTS

1. INTRODUCTION
2. MISSION DRIVERS PAST, PRESENT & FUTURE
3. THEORETICAL JUSTIFICATION
4. MUSES-CN ROVER DESIGN DRIVERS
5. DESIGN AND PHYSICAL IMPLEMENTATION
6. CONCLUSIONS
7. ACKNOWLEDGEMENTS

1. INTRODUCTION

Planned micro/nano sciencecraft imply low volume, mass and power resources. Smaller sciencecraft enable missions previously unfeasible and can translate into lower launch cost and the ability to fly more spacecraft per mission.

Space electronic components are specified to work over a -55C to +125C temperature range. This temperature range is even narrower (-40C to +85C) for some commercial parts. A large number of planned nano sciencecraft will not have the mass, volume or power resources needed to keep the avionics and instrument electronics warm in a space environment. To add mass, volume or power to keep flight electronics in the standard operating temperature range of flight and commercial components erodes the ability to produce nano-sciencecraft. Being able to operate the electronics for these systems below standard electronics temperature ranges helps enables this new generation of micro and nano-sciencecraft.

This paper will present the design environments of past spacecraft electronics and the needs of present and future nano-sciencecraft [1] electronics. We will then present the theoretical and empirical basis for the design of cold temperature operation of digital and analog electronic circuitry. We will next review the requirements of the

Muses-CN nanorover and its design [2],[3],[4]. Finally, the Muses-CN nanorover electronics implementation which allows for nanorover operations while addressing the mass, volume and power constraints of the Muses-CN mission will be presented.

2. MISSION DRIVERS – PAST, PRESENT & FUTURE

When coming from the paradigm of standard size spacecraft it is easy to assume that a standard electronics temperature environment will exist for micro and nano-sciencecraft. A comparison of normal size spacecraft with micro and nano size craft yields some insight into the temperature environments of much smaller spacecraft.

A look at traditional interplanetary spacecraft

The mass of traditional spacecraft from Mariner 2 to Cassini varied from 187kg to 2668 Kg., excluding fuel. The more recent of these spacecraft had power sources from 400 to 700 watts. Total spacecraft volumes varied from 5.4 to 27.2 cubic meters. [5] All of these spacecraft used space rated electronics parts that could handle the radiation environment of an interplanetary flight. If additional mitigation of radiation was needed for parts or systems, mass existed for shielding the components behind structural metal or specific dense materials.

Traditional interplanetary spacecraft have relied on heat surplus from electronics or RTGs to keep the spacecraft electronics warm. Thermal louvers help control the temperature of the space rated parts in the electronics systems not only within the military temperature range but in some cases at a fairly constant temperature that had a few degree variance after the spacecraft cruise stabilized.

Given the mass of standard spacecraft, additional tens to hundreds of kilograms in mass to allow for additional radiation or thermal shielding or larger power sources was a small fraction of the overall mass.

The resource shift

The magnitude of the margins on micro and nano-sciencecraft are much smaller. For example 10% margin of the Muses-CN mass, volume and power resources yields just 190 grams, 160 cubic centimeters and a quarter of a watt! [2]

While arguments can be made for the thermal insulation of such small systems as a way of the retaining heat, practical implementations that allow for interfaces from an isolated electronics area to sensors and actuators are often unrealizable for even the simplest of systems. Often the heat is conducted away by the very wires that are interfacing to the system electronics [6], [7]. Such heat paths can also limit the time available to science craft to use sensors that

want to stay cold for a long duration after a cooling period. An example of this is operating an IR sensor at first light, after having a long nighttime period to cool a heat reservoir that keeps the IR detector at a known temperature.

Opportunities for electronics systems that operate very cold

Given these needs, an approach was taken to investigate how possible it was to operate actual flight electronics at temperatures well beneath the standard temperature range of military and commercial electronics. We chose a practical limit of the temperature range easily reachable with liquid nitrogen in a temperature control chamber and arrived at -170C as a limit for the operation of electronics. Future investigations into operation with liquid helium sources are planned, but there are economic drivers to testing with liquid nitrogen over liquid helium.

With the lower temperature bound set, we investigated expanding the operating range of military rated electronics components and systems made from these components over the -170 to $+125\text{C}$ range.

JPL's Nanorover technology task worked toward two goals 1) to develop an operational rover 1/10 (to eventually 1/100) the size of the Mars Pathfinder Soujourner Microrover [8] and 2) investigate if standard integrated circuits would work over our new temperature range or if fully custom integrated circuits would be needed. The goal being to be able to operate our new nanorover on a Mars or an asteroid allow future sciencecraft operation in such temperature environments.

3. THEORETICAL JUSTIFICATION AND APPROACH

Part of the key to successful operation of electronics at extreme temperatures depends on the type of electronics components used. Bipolar transistors parts rely on thermal excitation to allow for conduction and are subject to carrier freeze out as temperatures are lowered[9]. Gain decreases and reaches zero as the temperature is reduced beneath manufacturers ranges, usually beneath -55C . Therefore bipolar transistors or parts that use bipolar transistors have a built in degradation beneath their specified temperature range. MOSFETs on the other hand offer an attractive alternative.

MOSFET operation

General operation of MOSFETS devices at extremely cold temperatures does not represent a degradation in functional performance as do bipolar devices. The gain of MOSFETS and MOSFET based devices actually improves as they are operated at colder temperatures. This is primarily due to the fact that the transconductance g_m increases as a function of temperature due to the mobility (μ_n) increasing as

temperature decreases.[10][11] The Threshold voltage (V_{TH}) also shifts as a function of temperature, but does not impede the transistor gain[11]. Equation 1 equation for shows the MOSFET channel current in the active region of the transistor[12].

$$I_{DS} = \mu_n C_{OX} / 2 W/L (V_{GS} - V_{TH})^2 \quad (1)$$

Looking at equation 1, we note that C_{OX} , W , L are constants of the device that is being tested. V_{GS} is dependent on the operating voltages of the MOSFET. This leaves μ_n and V_{TH} as variables. μ_n increases on the order of 3.7 to 2.2 cm^2/V -sec per a degree C for moderate to heavily doped substrates¹. V_{TH} changes on the order of 2.7mV per degree C. While the raising V_{TH} term can reduce the gain of equation (1) by 9.5% by varying the temperature from -55C to -170C, the mobility term increases gain (depending on doping concentrations) from 43% to 72% [10]. Thus the MOSFET gain is of order 33% to 62% greater at -170C then at room temperature.

Of importance here is that the transconductance increases as the temperature decreases even when the change in threshold voltage is factored in. Simulations and empirical measurements of various p and n channel MOSFETs were performed which support this model.

Figure 1 shows the simulation results on the MOSFET family of curves as a function of temperature.

Effects of temperature on an inverter—A complementary MOSFET (CMOS) implementation of an inverter is shown in figure 3. The effect of decreasing the temperature of the inverter, leads to decreased propagation delays due to the

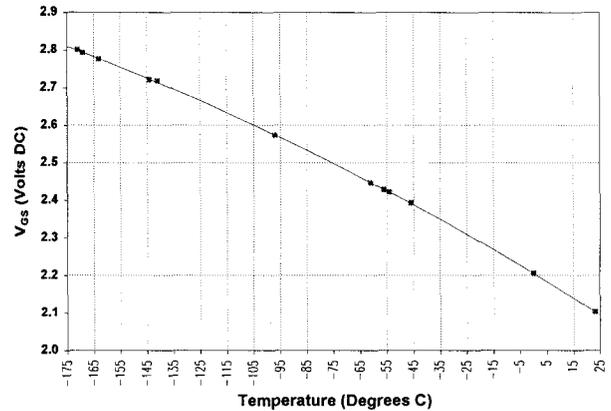


Figure 2a: Threshold shifts as a function of temperature in a n-channel power MOSFET

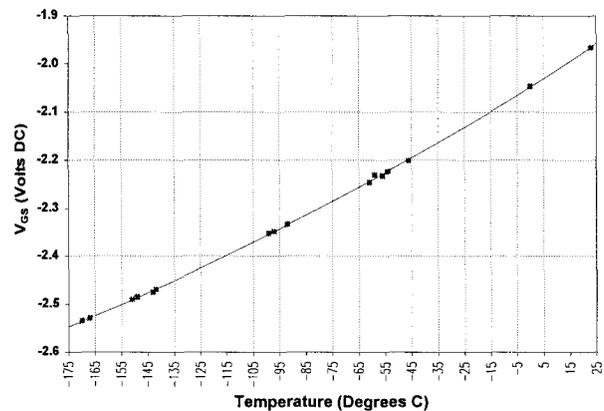


Figure 2b: Threshold shifts as a function of temperature in a p-channel power MOSFET

Figure 1: Simulation results of a family of curve changes as a function of temperature in a n-channel MOSFET

Figure 2a and 2b shows measured shifts in threshold voltage as a function of temperature for power MOSFETs.

Effects of colder than -55C operation on digital electronics

Expanding the effect of MOSFET gain to CMOS digital circuits we start by looking at the effect of temperature on the operation of an inverter.

increased gain, and decreased channel resistance of the internal MOSFETs at colder temperatures.

Figure 4 shows the effective equivalent circuit an inverter and helps to give some insight into the speed up of the digital signals through an inverter. As a practical matter the channel “on” resistance decreases as the temperature decreases. This coupled by the increased current supplied by the increased gain of the MOSFETs allows for the subsequent load capacitance (of the gates of driven CMOS logic) to charge or discharge quicker at colder temperatures.

SPICE simulations were run using the MOSFET models of the gate array used in our actual implementation. These MOSFETs were used to implement inverters and other logic functions for simulation. The graph of the decrease in

propagation delay as a function of temperature can be seen in Figure 5. These drives of the MOSFETs and load capacitance are those internal to the gate array. A propagation delay decrease to 66% in is shown from room temperature to -175C . Measurements were also taken to see the affect of decreasing temperature on a standard SSI

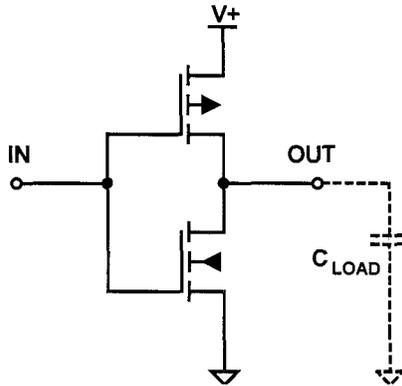


Figure 3: CMOS Inverter

CMOS (74C04) inverter. These results are taken at room temperature and at -170C . Figures 6a and 6b show the propagation delay decreased to 59% of room temperature value at -170C .

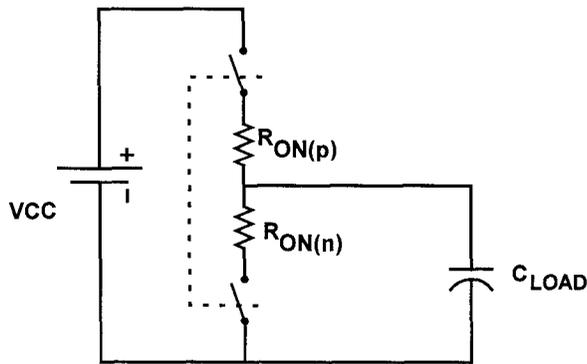


Figure 4: Simplified Inverter and load capacitance model.

To gain some more insight into the effects of decreasing temperature on CMOS logic, the transfer function of the inverter is plotted. This allows one to see the impact of the threshold voltage in the digital logic arena. Looking at the transfer function in figure 7 one can see the areas where the p and n channel MOSFETs are on as a function of threshold voltage. While the threshold voltages do increase relative to the voltage rails as temperature decreases, this only reduces the region where both MOSFET transistors are on. The curve is really a static curve as the transfer function does not really change as a function of temperature.

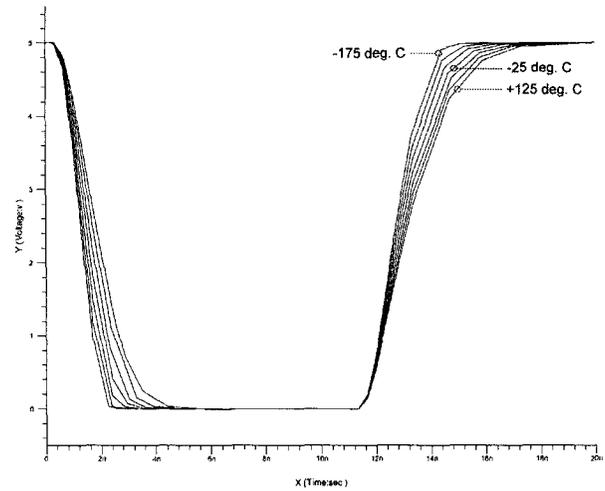


Figure 5: CMOS Inverter SPICE simulation showing propagation delay as a function of temperature

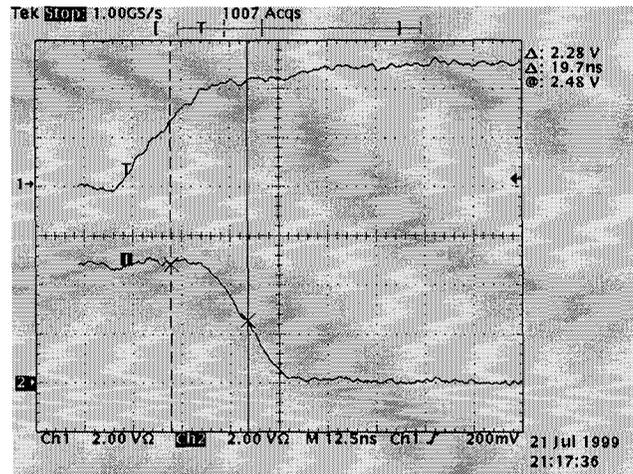


Figure 6a: 74C04 Inverter transitions at 5 volts, 23C.

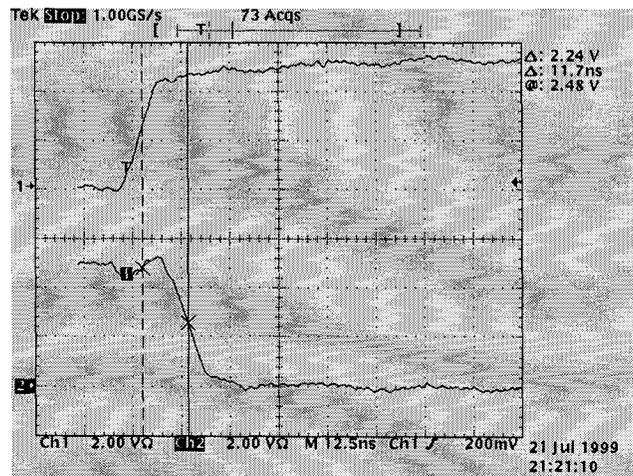


Figure 6b: 74C04 Inverter transitions at 5 volts, -177C

The affects on the inverter as a function of temperature generalize to combinational CMOS logic gates. This is useful from a system design point of view, whether the combinational logic is internal to a single chip or with use of CMOS components at a board level.

Figure 7: CMOS Inverter transfer function showing threshold voltage dependence on temperature

Effects of an inverter driving a D flip flop—Initial excitement of increase speed in CMOS devices is mitigated by the fact that faster response time of an gate driving a D flip flop may present hold time violations on the D flip flop. If the D flip flop remained at room temperature and a combinational gate driving it decreased it's operating temperature to -170°C the possibility for a hold time violation occurring does increase. In practice, there are a number of mitigating circumstances, primarily the fact that all aspects of CMOS devices are speeding up as the devices are cooling down.

D flip flop hold time analysis for Gate array flip flops—When the digital circuitry (combinational logic and flip flops) is incorporated into an integrated circuit (gate array or ASIC) there are two ways to analyze for hold time propagation.

The first approach we used was to simulate equivalent combinational logic and flip flops using the MOSFET models from the manufacturers line. Even though the models for the flip flops are not given, the models that we made (see figure 8) with appropriate load and routing capacitance had the same order of magnitude negative hold time (and other parameters) as the flip flop parameters given by our gate array manufacturers. Our circuit models tracked the gate array manufacturers estimate equations over the standard temperature range. These models were then tested over the extended cold temperature range and showed that the negative hold times actually got more negative as temperature approached -170°C .

In reality the hold time requirements of the flip flop will track (to some fidelity) the decrease in the propagation delay applied to the D input. Using models for the D flip

flop, D gate delay and clock tree one could simulate all inputs arriving at the flip flop inputs over temperature. This was the first iteration of our second approach to analyzing hold time at the extreme cold temperatures. Timing analysis was then done using the new simulation derived parameters at cold temperature. A second set of extrapolated timing parameters were obtained by comparing the decrease of the propagation time of an inverter constructed out of the MOSFET parameters for the line at -170 and -55 and using

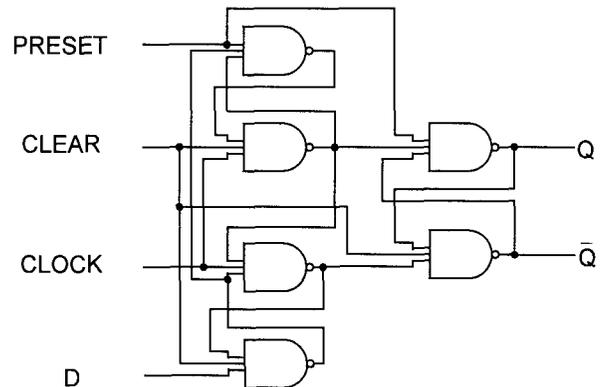


Figure 8. D Flip Flop circuit model.

this as a scaling factor for the D flip flop parameters. Equation 2 allows for calculation of the hold time presented to the D flip-flop input being analyzed in figure 9. This calculated available hold time can then be compared with the hold time requirement of the D flip flop.

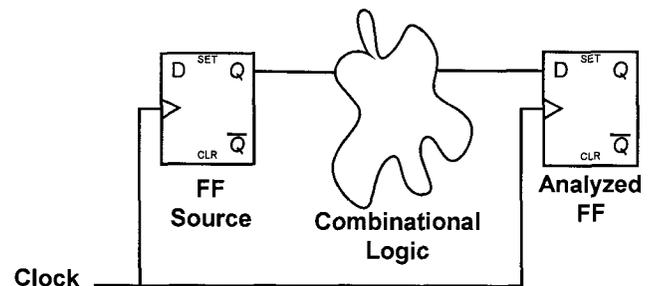


Figure 9. D Flip Flop simulation test circuit.

$$t(\min) = t(\text{rise/fall}) + t(\text{clk_q}) + t(\text{line}) - t(\text{skew}) \quad (2)$$

Using this approach, the hold time from simulation and extrapolated driving values compared favorably with the extrapolated hold time requirements of the D flip flop (which was still a negative hold time) and with a worst case 0nS hold time.

A even more conservative approach utilized the extrapolated parameters used in equation 2 a with positive flip flop hold time, and zero delay in the combinational logic and associated routing.

D flip flop hold time analysis for board level flip flops—

At a board level, all flip flops are can be analyzed with an approach similar to those used at the Integrated circuit level. At the board level we are adding wait states as needed to make sure that worst case timing is satisfied.

A unique approach can also be used at a system level to correct for propagation delay for parts that one does not control the internal design. It is possible to make up for lack of margin on synchronous designs by lowering the operating voltage of the entire digital system. This will slow back down the propagation delay to the levels seen at room temperature. Figure 10 shows the same inverter operating at -170°C with the operating voltage lowered to 3.9 volts. One can see that the propagation delay is back to 20.5ns, comparable with the 19.7ns seen in figure 6a. We also successfully showed that this approach can be used with complex commercial processor which fail to operate at cold temperatures due to internal speedup of the component.

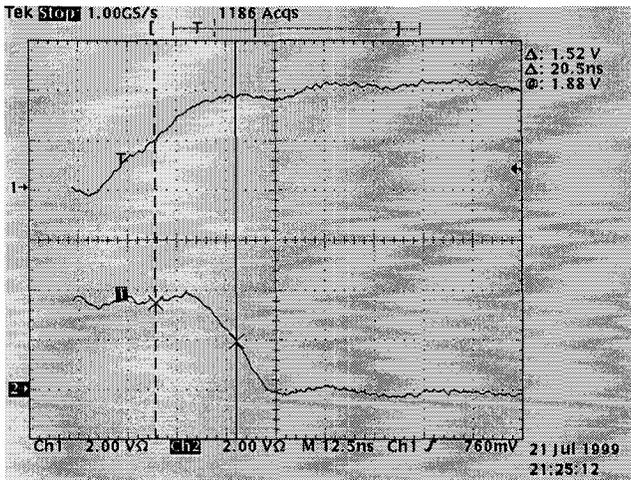


Figure 10. The Muses-CN Rover top level interface.

All told, these techniques allow use of standard digital combination and synchronous logic components already employed in spacecraft electronics design and if the technologies pass simple criteria, allow one to extend design operation well beneath the parts/systems cold temperature range.

Effects of colder than -55°C operation on analog electronics

Again, MOSFETs and CMOS analog circuits are preferred for use at extreme cold temperatures. As was the case of obtaining exact flip flop models from digital integrated circuit manufacturers, getting exact internal circuit representations for analog components is very involved, and perhaps not possible. The approach taken by our team was to thoroughly as possible to verify that the analog component device was as much as possible all MOSFET

based, and then to measure parameters over the extreme cold temperature range.

Below is a listing of components tested and accepted for use in extreme cold, 50Krad radiation environments.

POWER MOSFETs—Commercial power MOSFETs were first looked at for their small size consideration. The threshold voltage was characterized over the extreme cold temperatures, and general operation at cold temperature over time and cycling. After cold temperature operation was verified, radiation testing of the MOSFETs to a total ionizing dose of 50Krad. The MOSFETs actually operated up to 75Krad total dose. While this was surprising, the low threshold voltage used by these parts implies a thin gate oxide between the gate and channel which reduced the area for trapped charge[13], and gave them the relatively high total dose numbers for a commercial process. With power MOSFETs characterized over temperature and radiation, a component that allowed for both power control and general purpose amplifier exists for use at cold temperatures.

Analog Multiplexer—A rad hard MOSFET based 16 to 1 analog multiplexer was tested over temperature. Figure 11 shows a block diagram of the Analog multiplexer. Given that the multiplexer utilized MOSFETs for the actual analog signal switching and had CMOS logic buffering the switching MOSFETs, the previous MOSFET/CMOS cold temperature work supported testing of this part over temperature. Even though the part appeared to pass all the gates, one can never get the exact circuit to analyze, and extreme cold temperature testing has been an efficient way to find if there are any temperature sensitive components and or design practices in place.

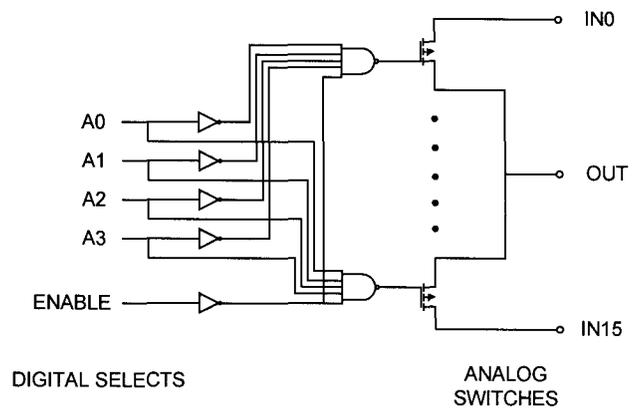


Figure 11. The Muses-CN Rover top level interface

In the case of the Multiplexers that we selected, all worked fine down to -170°C . Gain, linearity, and even “break before make” switching were tested. The gain and linearity were well within standard specification ranges at cold temperatures. The break before make test showed, that while the period of time between breaking of one

connection and the making of another did decrease slightly, that break before was not violated at cold temperatures.

Analog Switch— A rad hard MOSFET based analog switch was tested over temperature. Figure 12 shows a block diagram of the Analog multiplexer. Given that the analog switch utilized MOSFETs for the actual analog signal switching and had CMOS logic buffering the switching MOSFETs, the previous MOSFET/CMOS cold temperature work supported testing of this part over temperature. Again gain, linearity, and “break before make” switching were tested. Again, gain and linearity were well within standard specification ranges at extreme cold temperatures. Also again, “break before make” was not violated at extreme cold temperatures.

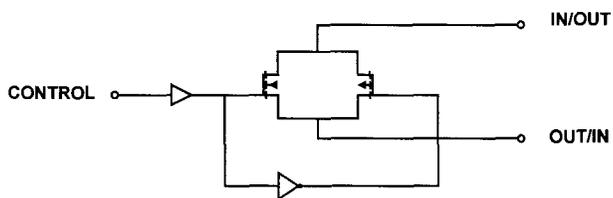


Figure 12. Analog Switch block diagram

Operation Amplifiers—In the case of the CMOS Operational Amplifiers, a number of interesting challenges arose. The first was that there was no radhard CMOS operational amplifiers to be found. This prompted radiation testing of the two candidate CMOS operational amplifiers in parallel with cold temperature testing of these amplifiers. While one op-amp had good radiation numbers (>100Krad)[14], it exhibited non-linear amplification, and eventually severe distortion at extreme temperatures. This was due to the final stage class AB amplifier MOSFETs not tracking over temperature. The second operational amplifier worked great down to -170°C and below. Gain product bandwidth actually increased down to -170°C . At issue was the radiation susceptibility at 10Krad total dose. Other candidate commercial CMOS operational amplifiers were tested cold, and those with final push pull stage amplification showed distortion at cold temperatures. Given this situation and with schedule, budget, or resource reserves to fabricate a custom CMOS operation amplifier, we chose to shield the op-amps with tantalum to allow for operation over the 50Krad radiation range.

Analog Component: Voltage Reference—A 2.5 volt bandgap reference had been tested for previous work over the -125 to $+25$ temperature range[15]. These previous test results (shown in figure 13) show that the reference does decrease slightly from 2.487V at room temperature to 2.448 volts at -125°C . We expanded the cold temperature testing range to -170°C and saw the same monotonic decrease down to about 2.432 volts. As seen in figure 13 the voltage decrease was monotonic over the extreme temperature

range. Testing began after a cold soak of 45 minutes, and the temperature was then increased. While the parts are monotonic and repeatable, calibration is recommended for each part.

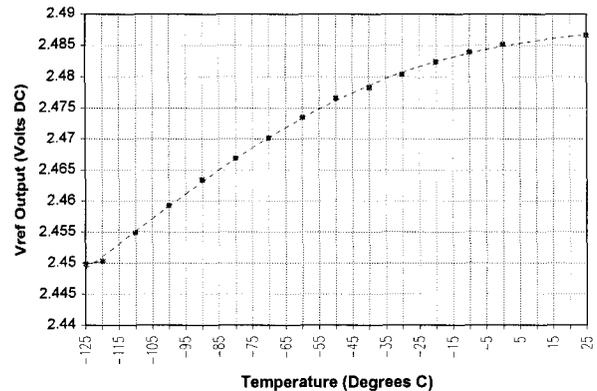


Figure 13. LM285 voltage reference as a function of temperature.

Analog Component: A/D Converters—Cold temperature testing on a number of CMOS A/D converters was performed. All performed well over the extreme temperature environment. In the end, design interface considerations were made for a serial interface 14 bit CMOS A/D converter. Again, radiation shielding was selected to overcome the total dose limitations, 17Krad for the selected part. Integral and differential non-linearity tests while successful to 14 bits at room temperature, were only accurate to 12 bits in the extreme cold temperature range. All A/Ds tested were successive approximation type converters which had internal resistor or capacitor trees use with their internal DACs, they also had the capability for external voltage reference.

Effects of colder than -55°C operation on passive components—Testing on resistors, capacitors, inductors and nano-D connectors were also performed in an effort to come up with an understanding of component variations at extreme temperatures that would allow component selection. Considerable attention was paid to effects of cycling on these components as the fabrication process are very different then those for Silicon. An overview will be given here as a detailed paper is being currently worked.

Resistors showed very little change as a function of temperature, and adhered specified PPM change in resistance per degree C over the extreme temperature range. Cycling of 40 cycles did not show significant changes for carbon and thin film resistors.

Capacitors in general showed a decrease in over the extreme temperature regime, but the decrease could be controlled via which capacitor type was selected. Tantalum, glass and

ceramic capacitors were tested over temperature and above 80 cycles. No variation in capacitance was observed or detected in statistical testing of the capacitors measured over 80+ cycles [15].

Inductors also showed a decrease in inductance over temperature and care needed to be afforded the core material and core winding.

In general the variation of the capacitors was not an issue for decoupling capacitors. For circuits where the capacitive and inductive reactances were important for circuit operation, values were usually chosen for worst case cold temperature operation. In these cases, either circuit demands did not mind the increased value of inductance or capacitance at room temperature, or close loop feedback inherent in circuit operation compensated for device changes.

NanoD connectors worked incredibly well when cycled 10 times over the -170 to $+125$ C temperature range. The test was constantly monitoring contact resistance on a number of different size connectors available, from 9 pin to 65 pin. The contact resistance varied slightly over temperature but had no measurable variance in resistance at any given temperature over the ten cycles observed. [17] No discontinuities were observed. The nano-D connectors were chosen due to volume and mass constraints, and the need for the interfacing the large number of interface signals (>600) in a small volume.

Available components and design philosophy for electronics design over -170 to $+125$ C

Given the theoretical and empirical justification for using digital and analog active devices, along with various passive devices we now have the components to design electronics to operate over the -170 C to $+125$ C temperature range. In general the design philosophy utilized in this design effort was one of implementing function digitally where ever possible. That is at the extremes of MOSFET operation, and not in the active region. Consciously not depending on analog parameters: C's, L's, R's and open loop gain where ever possible. Where needed, try to design the circuits so that the temperature variation of the passive, and the values of the passive components are bounded by a minimum or maximum needed value. For example, PWM control of variable voltage supplies or motor control instead of DACs or analog control of motors.

This toolkit of electronics components not only handles the cold temperature operation, but it also covers a radiation environment of 50Krad. Changes in radiation levels seen by the science craft will entail further shielding, which will only get one so far, perhaps 150Krad in the volumes anticipated, or development of custom components for the commercial components. It should be noted that the military

parts have TID numbers in the 300Krad to 1Mrad ranges over there standard temperature ranges. At constant extreme cold temperatures there is greater chance of trapped charge due to radiation staying trapped. Without thermal agitation, the charge is less likely to anneal out. In our case we expect to have temperature cycles from the extreme cold to the $+100$ C range which will mitigate this situation.

There is one last issue that should be brought up. That is lifetime issues due to hot carrier injection.[18], [19]. Hot carrier injection, a phenomenon that allows for imbedding of carriers from the MOSFET channel into the gate oxide causing build up of charge and eventually non function of the MOSFET, is usually associated with MOSFET geometry's. In an environment where the temperature is extremely low, the increase mobility allows for ballistic trajectories of the carriers into the gate oxide.

Our models conservatively imply a minimal 8 month lifetime. Our testing of the prototype computer board which has the largest number of dense small feature size components shows no errors over 3 days of continuous operation and monitoring. We are currently only slating this electronics for missions with time frames on the order of 2 to 4 weeks when the electronics will be operating and therefore subject to hot carrier injection We have tests in the future to characterize electronics operation at constant extreme temperature operation over months.

4. MUSES-CN MISSION DRIVERS

Application of theory to a flight rover:

Specific environmental needs of the Muses-CN Nanorover

After the demonstration of a prototype nanorover and cold temperature techniques, a flight opportunity arose on the Muses-C asteroid mission from ISAS[19]. The flight opportunity had the following mass, volume, power and radiation constraints on the Muses-CN rover, and are presented in Table 1.

Table 1: Resource constraints of Muses-CN

Resource	Rover Body	Electronics
Volume	14 x 14 x 8.4 cm	12.0 x 12.6 x 2.1cm
Mass	1.9 Kg	~582 grams
Power	2.5 Watts	2.5 Watts
Radiation	-	50 KRad
Operational Time	2 weeks	2 weeks
Asteroid Rotation	19-38 hours	19-38 hours

These constraints coupled with the mechanical and electronics volume and mass needs to allow for mobility of

this nanorover clearly point to a sciencecraft design with minimal mass, volume and power for thermal control. The Muses-C Asteroid mission will perform sample return and deployment of the nanorover on Asteroid 1982SF39 in 2003.

A general review of the requirements of the electronics for the Muses-CN rover are shown below in a bulleted list, and pictorially in Figure 14.

- Overview of rover electronics requirement
 - Computer with low power and sufficient memory
 - Analog signal chain & A/D
 - 64 channels (science and telemetry)
 - 10 brushless motor drivers
 - 3-phase PWM drive with hall feedback
 - A bi-directional 9600 baud radio interface
 - General digital interface to implement science control and mobility.
 - External access (ground and spacecraft) interface
 - Switching regulator Power supplies
 - Operation only from solar cells in nominal mode

- This allows for interfacing and control of:
 - 10 brushless DC motors.
 - 8 for mobility (4 for wheels & 4 for struts)
 - 2 for optics
 - A 256x256 CMOS Active Pixel Sensor
 - A 256 channel IR spectrometer
 - An Alpha Backscatter spectrometer
 - 14 temperature channels
 - 6 solar sensors (one for each body side)
 - A bi-directional 9600 baud radio interface
 - 20 power switches for power management.
 - Control of system clock to allow for power management of digital electronics
 - Operation from a 2.5 watt solar panel.

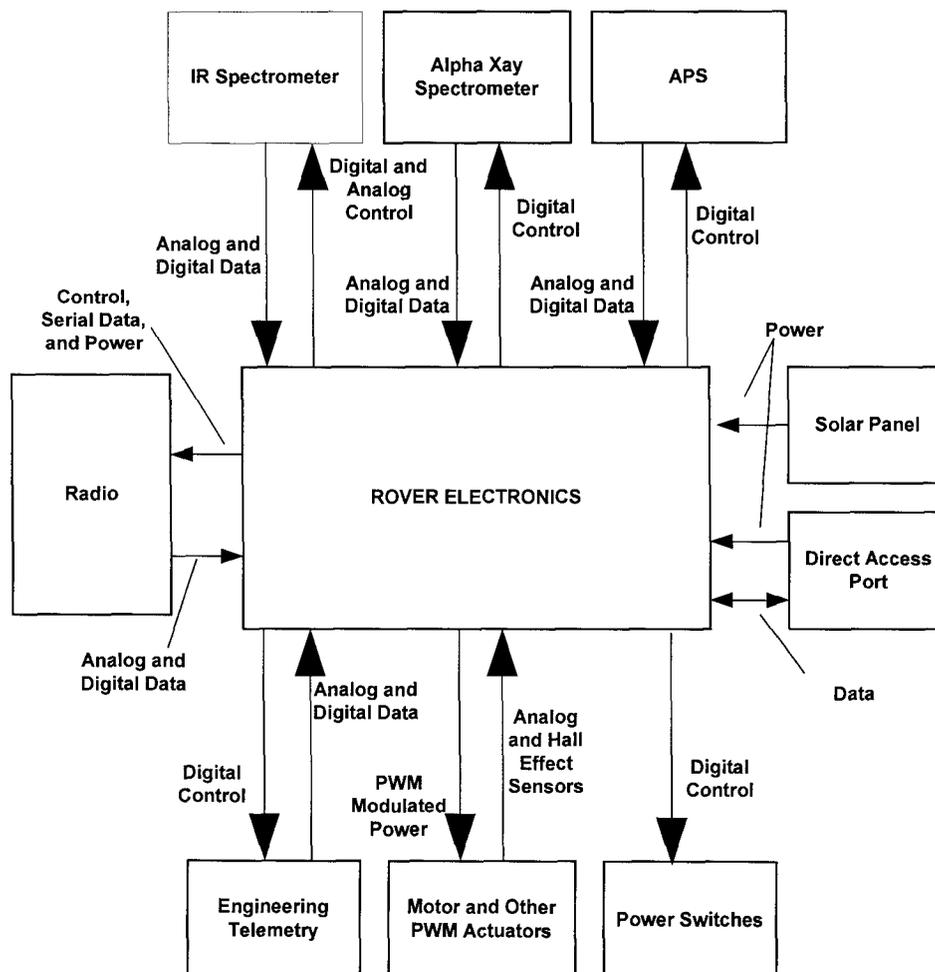


Figure 14. The Muses-CN Rover top level interface.

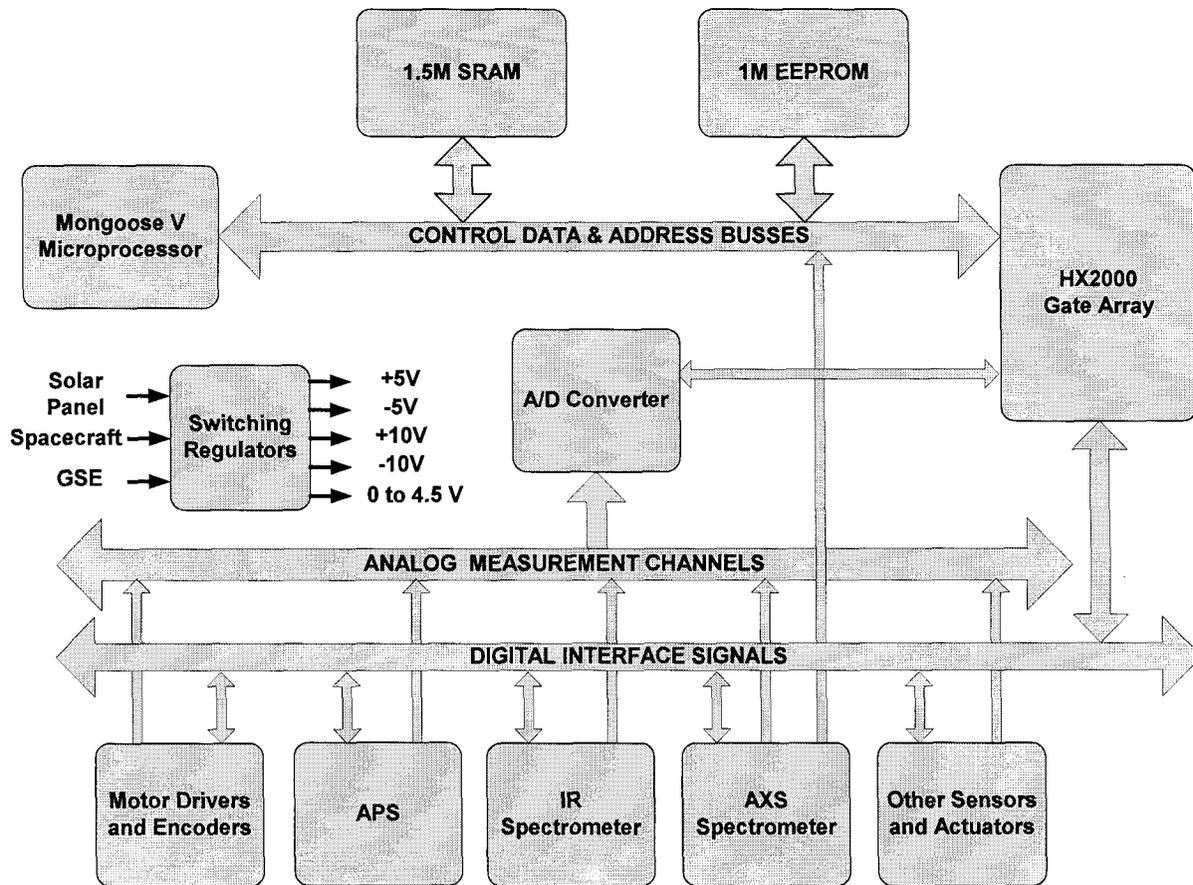


Figure 15. A block diagram of the Muses-CN electronics.

5. DESIGN AND PHYSICAL IMPLEMENTATION

Electronics Design Implementation

Figure 15 expands on the implementation of the rover electronics box shown in the block diagram in figure 14. The design implemented uses the approach and technique described earlier, CMOS and MOSFET devices, digital control where ever possible, and thorough modeling and testing of analog design.

The choice for a 32 bit processor allows for more power efficient operation when using the metric of instructions per joule. The idea was to maximize the power consumption for computing and data movement on an instruction basis. Memory size was determined for ability to control the rover and storage of the science for either overnight or immediate transmission. Operation on the asteroid will imply periods where the asteroid is not illuminated and therefore the rover will not have power. EEPROM was the storage medium of choice for nonvolatile data storage.

Interface between the CPU and memory, A/D, actuators, power control, science instruments (Active Pixel sensor (APS) and both spectrometers) along with any digital or

analog inputs was controlled by the Gate Array. Subblocks of the Gate Array control all fine grain timing need for all instruments as well as the brushless D.C. motor control which included a sine generation table, period control and PWMs drivers for all 10 motors on the rover. The Gate Array also includes a separate section that implements a separate system clock divider that allows for control of power consumption of the digital electronics by controlling the clock rate of the digital electronics. Control of the power is then largely regulated by (3) and is linear with frequency (f), voltage (V) and capacitance (C) can be considered constant.

$$P = CV^2f \quad (3)$$

All sections of the electronics shown in Figure 15 were prototyped and tested cold. The flight processor was implemented on the same gate array as the special functions implemented by our team here at JPL. This allowed for the Gate Array to be tested cold for verification of extreme cold temperature operability. The design of the CPU implemented in the Gate Array was a synchronous MIPS processor. Synchronous design was implemented on the our special function Gate Array. This coupled with the cold temperature analysis described

above, gives high confidence the design of the gate array will operate as specified.

Electronics Physical Implementation

The implementation of the rover electronics is via Chip On Board assemblies that fit inside the nanorover body. Partitioning of the functions worked out across six single sided board assemblies. The functions are partitioned as follows: a computer board, two (half size) memory boards, an analog measurement and A/D board, a motor driver board and the switching regulator board.

Four of these board assemblies are full size (see figure 16) and are joined into two double side board assemblies. The remaining two board are half size and a joined into a third double sided board assembly. Figure 17 shows side on view of the locations of the board assemblies relative to the rover optical bench.

The reason for fabricating single sided board assemblies and joining them together after fabrication is due for component density needs and the tooling needs during manufacturing.

Test COB boards have gone through 100 thermal cycles and show no crack propagation in the die attach and any cases where solder was used. At the inception of the project an initial stress analysis performed for large die (0.8 cm²) on a polyamide board material when the die was subject to a large temperature delta and when the die was subject to a large normal board force. In both cases the sheer needed to case the die to detach from the board was not exceeded. Additional testing will be done on the engineering models.

Below is another bulleted list that summarizes the board partitioning:

- Computer Board:
- 32 bit Synova Mongoose V a rad hard version of LSI's R3000
 - 1.5 Mbytes SRAM
 - 1.0 Mbytes EEPROM
 - ASIC for glue and interface to motors & science instruments.

- Analog signal chain & A/D Board:
- 64 analog channels
 - 10 bit A/D

- Brushless motor driver board:
- 10 – 3 phase brushless D.C. motor drivers
 - hall effect sensor interface

- Switching regulator Power Board:
- startup linear supply
 - fixed 5volt switching regulator
 - 0.3 to 4.4 volt variable voltage switching regulator
 - POR circuitry

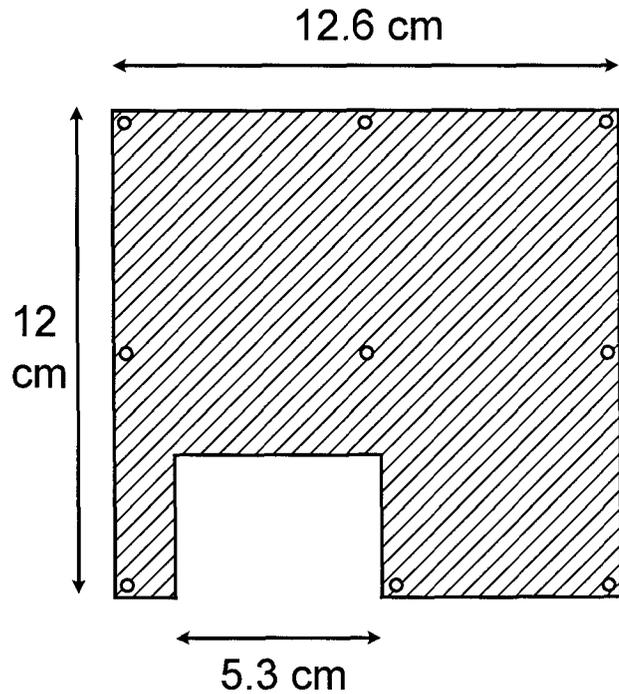


Figure 16. The Muses-CN top and bottom electronics board assembly footprint.

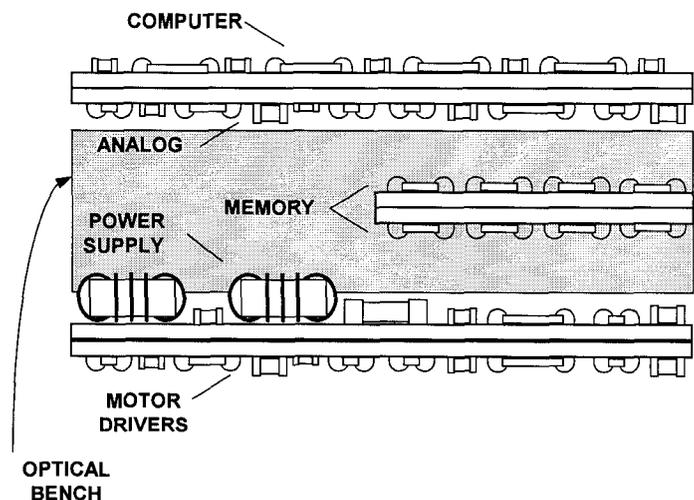


Figure 17. Side view of board stackup

Figures 18 gives a frame of reference of the rover electronics boards shown in Figures 16 and 17 with the

engineering unit optical bench. Figure 19 give a reference of the optical bench with a scale rover model.

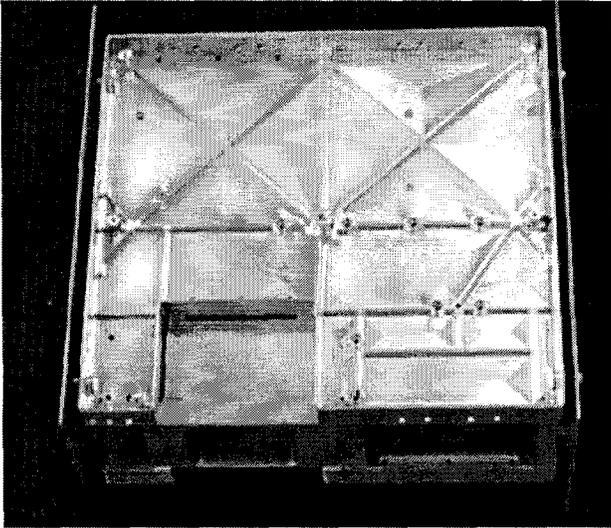


Figure 18. The top of the Muses-CN Optical test bench, which the electronics boards assemblies will mount to both sides of this assembly.

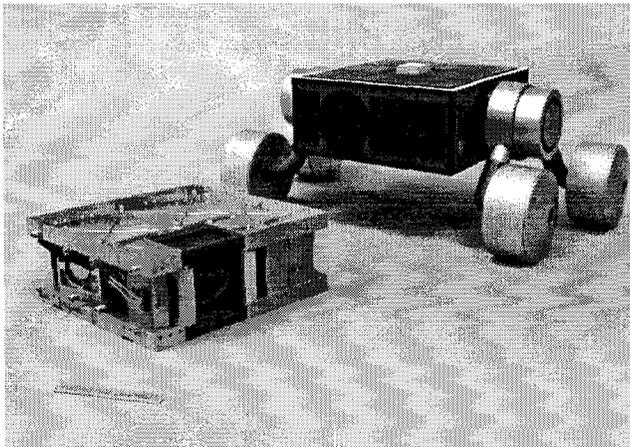


Figure 19. The Muses-CN Optical test bench, with a scale rover for comparison.

6. CONCLUSIONS

Expanded temperature range operation of regular devices

This work covers the implementation of a design approach for using standard and custom components over an extended temperature range and achieving reliable operation.

An theoretical justification for using MOSFETs in an extended temperature range was presented. An approach

to analysis of CMOS digital components was described at a board and integrated circuit level.

A unique approach that allows for compensating of digital CMOS components which have hold time margin problems at cold temperature was described. While the lowering of the voltage will recover propagation delay, it does so at the cost of noise margin.

The approach has been used to enable a flight nanorover design that will operate between -170°C to $+125^{\circ}\text{C}$. Issues related to temperature will have to be addressed in future nano-sciencecraft and we believe that this approach helps to enable future nano-sciencecraft.

There are issues to be looked at regarding hot carrier inject degradation effects in MOSFET based devices to enable longer nano-science craft mission of longer operating duration.

7. ACKNOWLEDGEMENTS

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Reference herein to any commercial product, process, or service by trade name, trademark, manufacturer, or otherwise, does not constitute or imply its endorsement by the United States Government or the Jet Propulsion Laboratory, California Institute of Technology.

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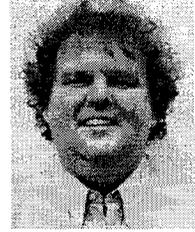
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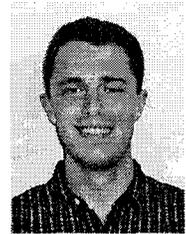
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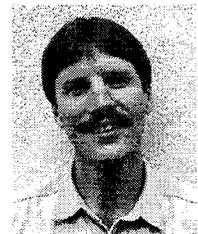
Michael Newell has fifteen years of experience designing and analyzing digital and analog systems for space flight, and is currently a senior member of technical staff at JPL. For the last four years he has been investigating operation of CMOS devices at cryogenic temperatures for both the Nanorover Technology Task and as the Muses-CN Cognizant Engineer. He has a patent for his work on a 32 bit risk processor MCM with reconfigurable hardware. His flight work includes design of integrated circuits design for the Cassini Spacecraft, lead designer of the APEX flight experiment, design team lead of the Mars Environmental Compatibility Assessment, along with design analysis on the Sojourner Rover. Research work includes embedded systems for research robots, special purpose microcontrollers and his current task, leading the Gilgamesh super computer hardware design team at JPL. He has a BSEE from the California State Polytechnic University, Pomona.



Ryan Stern has been an associate member of the technical staff at JPL for nearly 5 years while simultaneously being a full-time student. He has worked on the MECA and MUSES-CN projects doing circuit design and cold-temperature electronics analysis. He received his BA in Physics from Pomona College in 1999, and is currently in the Master's program at UCLA for Electrical Engineering.



David Hykes has fourteen years in spacecraft circuit modeling, analysis and design. He has performed transistor level modeling, parts stress, worst case, and failure mode analysis for various defense systems. As a senior member of technical staff at JPL he has worked in reliability and mission assurance on the Cassini, MISR, and X33 AFE tasks. He has designed a number of analog systems for X33 AFE, Athena and Muses-CN, and is currently performing analog design for the Mars Exploration Rover. He has a BS degree in engineering from California State University, Fullerton.

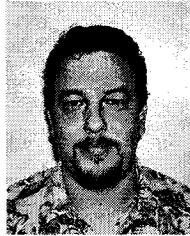


Gary Bolotin has 15 years of design and analysis experience in the area of digital integrated circuit and board design. Gary was the lead designer of the Electronics for the Mar Pathfinder Sojourner Rover. He also designed many gate arrays for the Cassini Spacecraft which is currently on the way to Saturn.



He Early on at JPL he received a patent for his work in the MAX fault tolerant computer architecture and implementation. He is currently the deputy manager of the Avionic Equipment section at JPL. He has a BSEE from Illinois Institute of Technology and a master's degree from University of Illinois.

Timothy Gregoire has been a Senior Electronic Technician at JPL since 1989. In that time he has served primarily as a designer and task leader on the development of automated thermal control systems designed to simulate solar flux and orbital thermal transients in JPL's space simulators.



These systems were successfully employed in the MLS, TOPEX, NSCAT, PMIRR, Mars Pathfinder, Cassini, and MISR Solar Thermal Vacuum Tests (STVT). He has also designed and built optical benches and laser systems for several metrology tasks and provided key technical support to U.S. Army sponsored projects such as ASAS and AMTT. Since May of '97, Timothy has been providing electronic support to the Nanorover development task and the MUSES-CN project.

Thomas McCarthy is a Member of Technical Staff at JPL. He has co-designed a Gate Array on the MUSES-CN Rover. In addition to Gate Array design and test, he has designed and prototyped numerous electronic systems for the MUSES-CN Rover and OMRE including the prototyping of the 32-bit RISC processor and Ethernet boards. He has also been a member of the team which performed two successful interface tests with the Japanese Muses-CN spacecraft interface. Previous work included developing Hardware Tests for the Pathfinder Sojourner Rover. Tom earned a BS in Electrical Engineering from the University of Notre Dame, in 1997.



Christine Buchanan is a senior member of technical staff and is current group supervisor of the ASIC Design group for the Avionic Equipment section at JPL. She has 10 years experience with space flight hardware in the areas of Gate Array design and hardware test & integration. She is a verilog HDL designer and has spent the last three years co-designing the MUSES-CN Gate Array which includes the Nanorover motor controllers and other rover & spacecraft functions. She is an expert in and has consulted numerous flight projects both locally and internationally on their Mil-Std-1553 bus implementation and test strategies. At JPL she has worked on Cassini, Mars Volatiles and Climate Surveyor, Deep Space 1, Low Power Serial Data Bus, Space Technology Research Vehicle, X2000, and Team-X. She has a BS degree in Electrical Engineering from California State University, Northridge.



R. Scott Cozy is currently a Member of Technical Staff at the Jet Propulsion Laboratory in Pasadena, California. Prior to his arrival at JPL in 1997, he worked for four years at the Robotics Research Laboratory at the University of Southern California. During his three years at JPL, he has worked on the Nanorover Technology Task, as well as the MUSES-CN team, where he is currently designing and testing flight electronics. He holds a bachelor's degree in Computer Engineering/Computer Science from the University of Southern California, and a degree in Electronic Engineering from Los Angeles Trade Technical College.

