

Radiation Issues and Applications of Floating Gate Memories

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Abstract—The radiation effects that affect various systems that comprise floating gate memories are presented. The wear-out degradation results of unirradiated flash memories are compared to irradiated flash memories. The procedure analyzes the failure to write and erase caused by wear-out and degradation of internal charge pump circuits. A method is described for characterizing the radiation effects of the floating gate itself. The rate dependence, stopping power dependence, SEU susceptibility and applications of floating gate in radiation environment are presented. The ramifications for dosimetry and cell failure are discussed as well as for the long term use aspects of non-volatile memories.

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1. INTRODUCTION

With a large number of long term space missions being flown with non-volatile memory (NVM) banks as integral avionics systems, such as the upcoming mission to Europa, the need to precisely understand the effects of radiation on the NVM types has grown considerably. This is mostly because the NVM banks on such missions are by far the most susceptible to total ionizing dose (TID) effects, and fairly susceptible to single event effects (SEE) [1, 2]. The variation of radiation effects with variables like dose rate, stopping power, and radiation type has become very important.

Flash memories command the lion's share of commercial NVM applications: digital cameras, wireless communication devices, and computer storage. They are also being considered for many current and future JPL space systems, including solid-state recorders for the X2000 project. Previous missions used DRAMS for solid-state recorder applications. Flash technology has evolved very rapidly during the last five years. Multi-level 128-Mb devices that can store more than one bit per cell, are now available commercially including advanced flash memories with complex internal control circuitry, block erasing and writing to internal buffers, which is all transparent to the user. Flash memories of older

generations used an external erase/write pin that required a separate power supply of 12 volts for erasing and writing data to the cells. Newer, single power supply advanced flash memories rely on internal charge pump circuits to provide the high voltages that are needed for erase and write operations. Scaling issues for newer flash devices are more complex than conventional CMOS devices because of the need for high voltage (10 to 20 volts) for erasing and writing. The tunnel oxides used in flash storage cells are above 9nm and have not been reduced, as devices have been scaled [1, 2]. Multi-level cell storage is one approach for the achievement of higher storage density. Ionizing radiation has always been an issue for flash devices, and newer technologies have increased susceptibilities due to scaling.

Two separate technologies have been developed to build the basic cell structure of advanced flash memories. The NOR structure technology uses channel hot electron injection to program and Fowler-Nordheim (F-N) tunneling to erase. A typical floating gate cell is shown in Fig. 1. When a flash memory is read, 3.3V is applied to the control gate and drain while the source is grounded. In an erased cell, the control gate voltage overcomes the transistor turn-on threshold voltage, V_{th} , and the sense-amplifier circuitry detects the drain-to-source current and translates it to a "1". The voltage due to the control gate of a programmed cell is not sufficient to overcome the V_{th} and the absence of the drain-to-source current translates it to a "0".

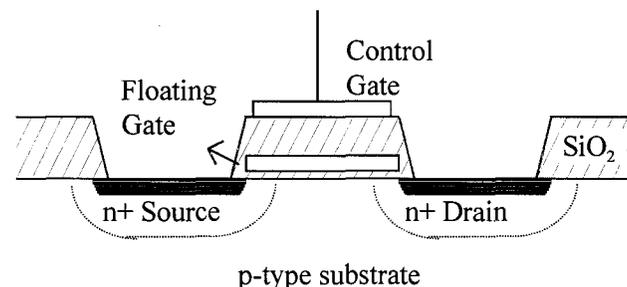
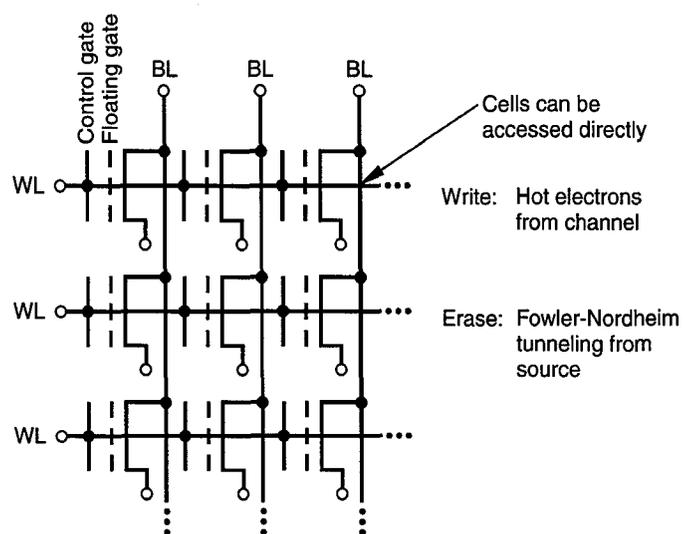


Fig. 1. Standard floating gate device. The drawing is not to scale and the gate oxide thickness varies for each technology.

The NAND structures use F-N tunneling for both writing and erasing. Reading is identical to the NOR structure's method. The NAND structure erases and programs uniformly across the gate oxide, resulting in minimal wear. The NOR structure, on the other hand, concentrates

the programming current to the source side corner of the gate oxide, resulting in a decrease in wear-out endurance compared to the NOR structure. The NOR structure is faster than the NAND structure, due to the lower current achieved through tunneling.

The cell architecture of a NOR flash memory, Fig. 2, provides direct access to an individual cell, allowing random access reading and programming. Because of the need for one bit line contact for each two cell group, the dimensions of a NOR array are about 140 percent larger than those of a NAND technology [3]. A typical NAND array stacks 16 floating gate transistors connected in series along with two control transistors. This arrangement eliminates the bit line contacts between the cells as shown in Fig. 3, which allows more transistors to be placed into the die. Operations of both circuits are explained in [4].



3 wordlines and 3 bit lines shown
Fig. 2. Cell architecture of a NOR flash memory.

When considering flash memories for space missions, any application that uses intensive read/write cycling will be of the most sensitive to radiation. This mode is important in data recorder or other applications where flash memories are being used in designs that were previously restricted to DRAMs or SRAMs. In such applications, like X2000, there is the concern of wear-out, which occurs after a large number of erase/write cycles. Since the intensive read/write mode will be used in future applications, the robustness of this mode in space environment must be well understood. Most of the radiation liability of flash memories arises from the circuit elements that read and write the floating gates, as the studies below show.

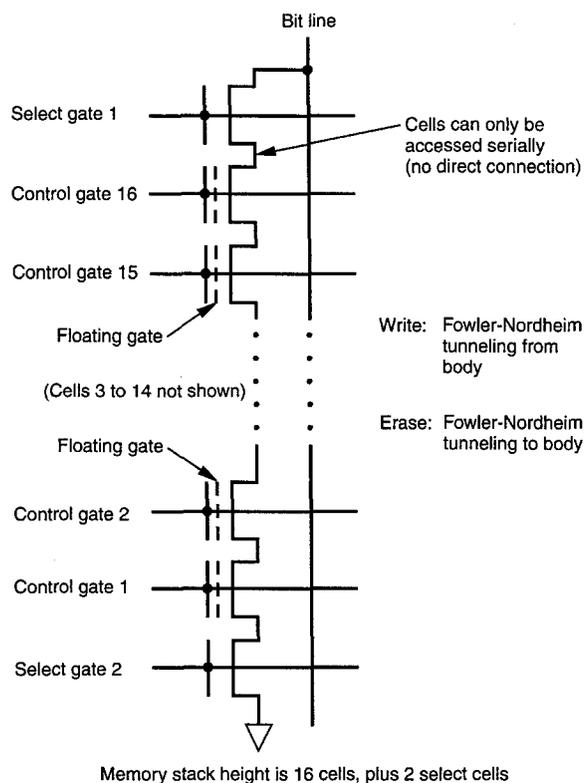


Fig. 3. Cell architecture of a NAND flash memory.

To study the effects of radiation on the floating gate, the UVPROM allows the easiest investigation. This arises from the UVPROM's simple on-board circuitry. The structure of the UVPROM's cell is similar to other NVMs, like the EEPROM or flash memories. UVPROMs are erased only by exposure to radiation [5]. UV radiation is specified by the manufacturer to erase the device. Electron-hole pairs are generated in all areas of the circuit when ionizing radiation interacts with microelectronic circuits [5]. In the FAMOS cell of a UVPROM, some of the holes may interact with the floating gate of the cell to reduce its stored charge [5]. Electrons may also be removed from the gate by direct radiation interaction.

An energetic charged particle generates electron-hole pairs according to its Linear Energy Transfer (LET = stopping power / target density), and the amount of charge removed from the floating gate depends on the LET and the proximity of the trajectory to the gate. One would expect different radiation types to have similar but not identical effects because of different recombination rates and mechanisms [6]. The effect of any exposure to ionizing radiation is the partial removal of charge from the floating gate. This, in turn, reflects the amount of exposure received. By measuring the amount of radiation required to remove all of the charge from the floating gate, the sensitive volume of the oxide which makes up the collection region for erasure surrounding the floating gate of the FAMOS cell can be determined.

2. EXPERIMENTAL PROCEDURES

A. Flash System Analysis

I. Devices Selected for Study

Flash memories from two manufacturers were selected for wear-out. They are listed in Table I. The charge pump effects were studied using the Samsung devices. The wear-out endurance of the Intel parts was studied to support this correlation.

TABLE I
DEVICES SELECTED FOR STUDY

DEVICE	SIZE	MFG	TECHNOLOGY
28F128	128-Mb	Intel	NOR multilevel flash
KM29U128	128-Mb	Samsung	NAND flash
AMD27C64	64-kb	AMD	UVRPOM

Electrical tests after irradiation level were made using an Advantest 3342 test system. The biased circuits follow the DC standby current characteristics of Intel and Samsung specifications. Tests include evaluation of the write operation that requires initial erasure of the flash memory. TID tests were performed at the JPL cobalt-60 room-type irradiator. The devices under test were irradiated under standby power conditions at a dose rate of 25 rad (Si)/s.

II. Charge pump circuit

The typical charge pump circuit is based on the circuit proposed by Dickson in 1976 [7]. The Samsung charge pump circuit uses MOS transistors to accomplish the diode function, as shown in Fig. 4. The circuit operates by charging the coupling capacitors successively each half-clock cycle. The transistors, functioning as forward bias diodes, hold an incrementally larger voltage at each step. The open-circuit voltage can be calculated with the following equation:

$$V_{out} = V_{cc} - |V_{te}| + N (\infty V_{cc} - |V_{te}|) \quad (1)$$

Where V_{te} is the effective V_{th} of the pass transistor, ∞ is close to 1 in practical cases, N is the number of stages.

So, even in standby mode, the charge pump is fully engaged. The generated output voltage is directly proportional to the number of charge pump stages and, therefore, it can be generated even at a very low supply voltage ($< 2V$).

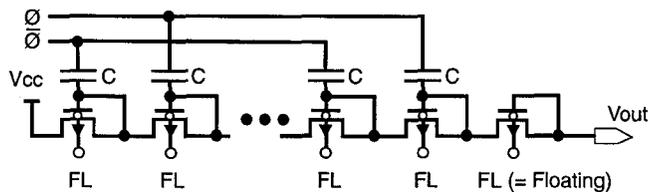


Fig. 4. Samsung flash memory charge pump circuit from Ref. 11.

III. Set-Up for Charge Pump Measurements

The reason for suspecting charge pump degradation in wear-out is obvious. Data from previous papers had shown that the degradation of the internal charge pump affected the write and erase capabilities of flash memories [1, 2, 4]. The TID failure level of the Intel 28F016SV flash memories with two power sources (by passing the internal charge pump circuits) was 100 krad(Si), compared to the 25 krad(Si) with the 5V-only power option [4]. Direct measurements of charge pump voltage were accomplished through a probing contact at the die. The probe was connected to a digital multi-meter to read the charge pump voltage of the flash memory arrays. In this study, a Samsung flash memory device was de-lidded to expose the probing pads.

IV. Wear-out Test Procedure

Current test programs were modified to exercise each selected block repeatedly. The test program erases the contents of the flash memory devices (verification of "1" to ensure that the erase process was successful), writes "0" (inversion of data) and then reads "0" (verification of writing data) in all locations of a selected block. The cycle repeats until the test program loop ends or is cancelled.

Two Intel devices were used to study the effects of TID on wear-out of the erase capability. Intel 28F128 devices that operate after being irradiated at 7krad(Si) were then cycled until they failed to erase. Two Samsung devices were tested for wear-out after 9 krad(Si). The selected Samsung device was cycled until it failed to write.

B. Floating gate studies

The devices used in this study were AMD27C64 series UVRPROMs consisting of 65,536 FAMOS cells in an 8192x8 bit format. UV radiation can erase the device in part due to a quartz lens encased in the ceramic dip directly over the cells. The normal commercial use of this device is as a read only memory. The UVRPROM is exposed to low energy (< 8 eV) ultraviolet radiation, which removes electrons from the floating gate, if erasure is desired.

The floating gate has been shown to be the most robust subsystem of floating gate memories, but as floating gate

memories become scaled, they floating gate may become the foremost radiation liability. The UVPRM were programmed to capacity and interrogated after exposure to radiation. The amount of erasure is measured in terms of equivalent UV radiation. In this manner, the effects of different radiation type, LETs, dose rates etc, can be investigated by only pin interrogation. This is described in detail in [8]. Since the radiation response can be precisely measured and calibrated, floating gate devices can be successfully used as dosimeters. This has been shown on the MPTB satellite and is described in detail in [8].

3. RESULTS

A. Flash Charge Pump Degradation

Fig. 5 shows that the charge pump voltage is constant until the memory device reaches 6 krad(Si) where the voltage drops about 100 mV (from 12.53V to 12.43V). After 7 krad(Si), the measured voltage decreases to 11.8V, but the device still can be erased and written with the new pattern. At the next level of 8 krad(Si), it fails catastrophically during the erasure of 1,024 blocks of memory cells, and the charge pump voltage drops sharply to 6.7V. Direct probing has shown that TID stops the charge pump from providing the expected output voltage for proper erase operation. The dose level at which this device fails is within the distribution of typical radiation failure levels for this device type [1].

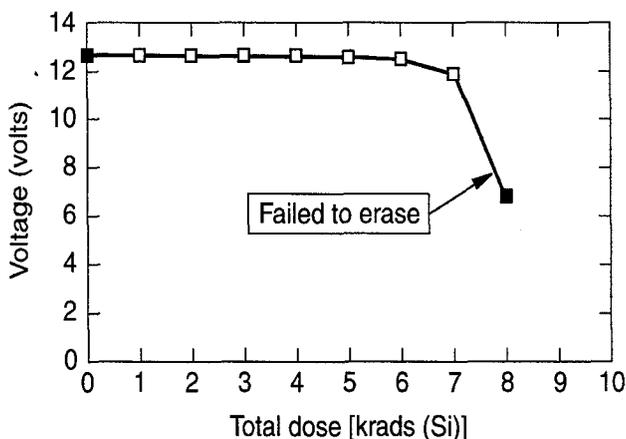


Fig. 5. Charge pump voltage versus total dose.

B. TID Effect on Wear-out

Wear-out is the endurance of flash memory erase/write functions, and it is usually specified by manufacturers as a given number of erase/write cycles. As described earlier, there is some concern about wear-out in solid-state recorder applications that would require many read/write sequences. However, the selected block must be erased before any data can be written into the arrays of a flash memory cell. If the block cannot be erased or is

only partially erased the programmed data will contain errors.

Figs. 6 and 7 show wear-out results. After a dose of 7 krad(Si), both Intel devices failed to erase the selected block at about 20,000 cycles compared to 95,000 cycles for an unirradiated part as shown in Fig. 6. Erase errors are permanent failures to remove electrons from the floating gates and registered as "0"s by the sense amplifier circuitry in the read operation. In this study, both irradiated parts were tested with the maximum allowed erase time as specified by Intel (5 seconds per block erasure). Write errors of "0" data are failures to place correct amount of electrons to the floating gates and registered as "1"s during the read operation. It is also obvious that TID accelerates the erase/write wear-out effects of both Intel and Samsung flash memories. Since erase/write are the only operations that use the 12.5V, the degradation must result from the decay of the charge pump circuitry and previous studies have shown that the read operation is unaffected up to 50 krad(Si) [2]. Fig. 8 shows another effect of the charge pump degradation. Radiation lowers the charge pump voltage thus reduces the tunnel current removing the electrons more slowly.

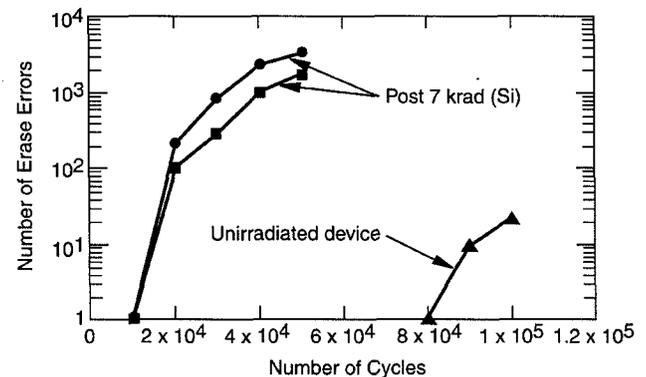


Fig. 6. TID effects on wear-out of Intel devices. Erase errors are failures to remove charge from floating gates.

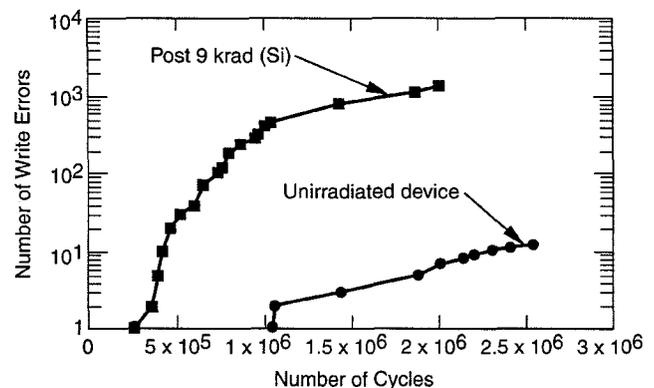


Fig. 7. TID effect on write wear-out of a Samsung device. Write errors of "0" data are failures to place correct amount of electrons to the floating gates.

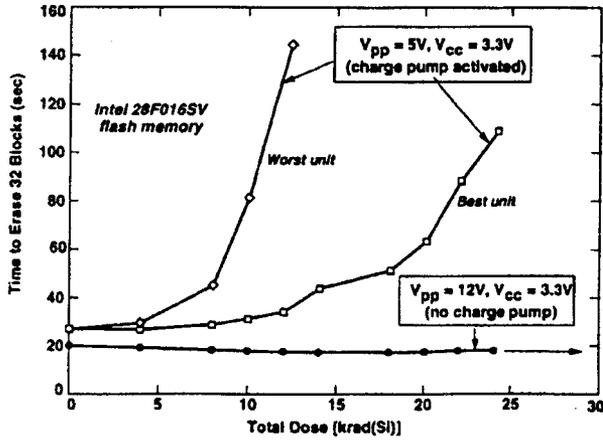


Fig. 8. Effect of dose on timing. The diminished charge pump take longer to induce tunneling in erasure.

C. UVPROM Cell Erasure Results

The plots the fraction of cell erasures as a function of doses for various radiation types are shown in Fig. 9. Fig. 9 shows the result of selected live readout methods. Shown are UV, 50 MeV protons and 1 GeV Argon ions. These erasure curves were directly measured during experiments at accelerators. Fig. 10 shows the fraction of charge on the gate as a function of dose.

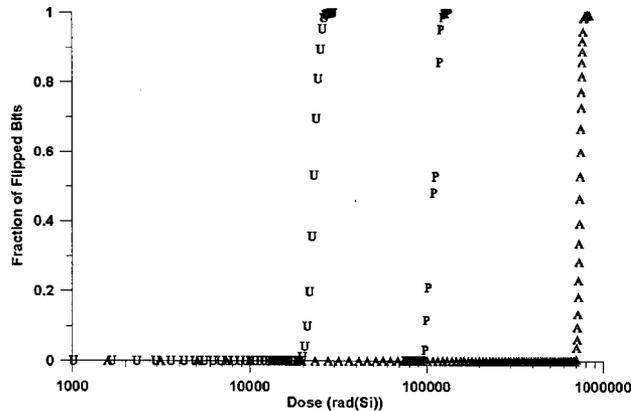


Fig. 9. The live readout erasure response of the device to various radiation types. The U point protector is UV, the P is 50 MeV protons, and A is 1 GeV Argon ions.

From Figs. 9 and 10, the total amount of radiation require to erase a device can be measured. The power law behavior is most likely due to varying sensitivity to dose as a function of dose. The field of the floating gate will decrease with dose, which leads to an exponential

relationship, i.e., $E = E_0 e^{-\frac{Dose}{Dose_0}}$, where E_0 is the initial field and $Dose_0$ is a constant. This may explain why higher LET particles are less effective at erasing the device. So there must be two new erasure mechanisms

that are shown here. The rate of erasure is based on dose and also LET, revealing that the oxide around the floating gate must contribute to the erasure mechanism. It is impossible to differentiate between these effects using only the output from the pins of the device.

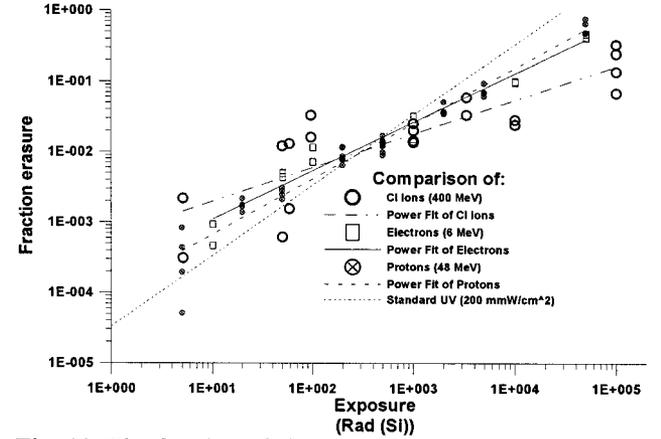


Fig. 10. The fraction of charge left on the floating gate as a function of radiation.

C. UVPROM Sensitive Volume Calculation

By looking at the relationship in Fig. 10, one can start to see how much the oxide affects the erasure process. The relationship is an exponential dependence of erasure efficiency on LET. Not surprisingly, higher LET radiation experiences higher recombination and thus erasure rates are affected. A more obvious statement of this can be seen through the calculation of the effective sensitive volume thickness which is given in detail in [6]:

$$t_{eff} = \frac{1.8 * 10^5 eV}{\rho D_{sat} A_{FG}} \quad (1)$$

The relationship between t_{eff} and LET is shown in Fig. 11. The relationship is again exponential, revealing that the effective thickness of the collecting oxide decreases with increasing LET. The reason for this inverse effect may be due to the charge generation profile of higher LET particles.

D. UVPROM Dosimetry on the MPTB Satellite

One of the important applications of floating gate devices is the measurement of absorbed dose, or dosimetry. Two AMD27C64 UVPROMs were placed in the MPTB experiment as prototype dosimeters. The results are shown in Fig. 12. The first 1200 orbits of the experiment are shown. The other dosimeters, A8, B3, B8, and C4, are shown in solid for comparison. The deviation around orbit 800 is postulated to be saturation in the RADFETs.

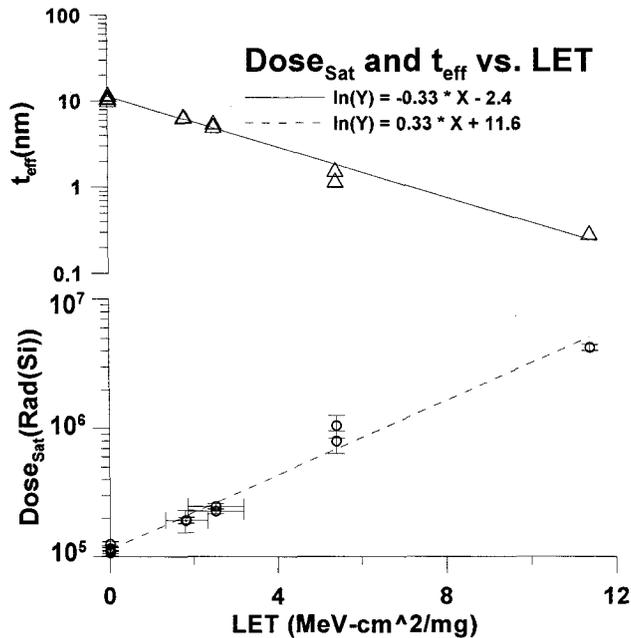


Fig. 11. Total dose required to erase the device versus LET of various radiation.

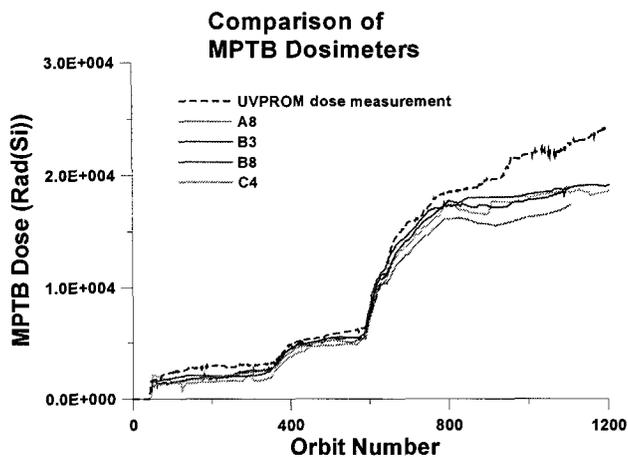


Fig. 12. Dose measured on the MPTB experiment..

IV. DISCUSSION

Several previous studies of radiation effects on EPROM and EEPROM floating gates have reported that data integrity could stand up to 10^5 rad(Si). TID in the range of 10^4 to 10^5 rad(Si) is not expected to upset the data in the memory transistor [1]. SEE studies also concluded that radiation damages the peripheral circuitry before affecting the cell [1, 2]. The total dose failure levels of a 256K EEPROM are limited to values of 10 to 30 krad(Si) due to loss of drive capability of the peripheral circuitry, not charge loss from the memory transistors [1]. The most sensitive control circuitry in flash memory devices is the internal charge pump circuit. Any leakage current within the internal charge pump circuit will lower the output voltage. Serious leakage currents can be conducted by the capacitors coupled in parallel with two non-interleaving

clock signals. The leakage current increases with TID. Any stage-to-stage increases in leakage would also reduce the charge pump output voltage [3]. For NAND devices it should be noted that the highest voltage is needed for erasing (20V), then programming (18V), then reading, this is the order in which failures are seen in the TID tests on the Samsung 128Mb flash memory [2].

Charge injection through the dielectric by tunneling causes hole trapping at the interface. The trapped positive charge induced parasitic leakage current. The floating-well charge pump circuits can also generate substrate current. The resulting currents can clamp the charge pump output voltage to low values, making the flash memory inoperable.

V. CONCLUSIONS

Of the conclusions that can be drawn from this work, the most outstanding is that TID directly affects the output of the internal charge pump. Radiation also reduces the endurance of flash memories due to operations that depend on charge pump output voltages. Thus there is a correlation of charge pump degradation and the number of erase/write cycles. This relationship needs more quantitative investigation. Future studies will quantify the effects of TID on wear-out.

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