IEEE 2001 Aerospace Conference, Big Sky, Montana

HIGH SPEED INTERCONNECT FOR THE SPACE INTERFEROMETRY MISSION W. J. WALKER

JET PROPULSION LABORATORY, CALIFORNIA INSTITUTE OF TECHNOLOGY, PASADENA, CA ABSTRACT

In 2008, NASA's Space Interferometry Mission (SIM) will place in earth-trailing orbit an interferometer that is capable of measuring the positions of astronomical objects with an accuracy of 4 microarcseconds. It is expected that the ability to perform astrometric observations with this unprecedented accuracy will lead to the solution of many significant problems in astronomy. For example, it will facilitate the detection of earth-like planets in orbit around a distant star by measuring perturbations in the star's position due to the gravitational pull of the planet.

This paper focuses on one of the many technical challenges associated with the implementation of an interferometer that can withstand the rigors of launch and several years of unattended operation in space.

The SIM Instrument incorporates four co-aligned Michelson interferometers on a 10m precision support structure. To make useful observations in the presence of disturbances due to vibration and thermal effects, it is necessary to establish real-time control over various optical pathlengths to within a small fraction of the wavelength of light. The strategy for achieving this in SIM relies heavily on active closed-loop control. To achieve the stated accuracy in the expected dynamic environment, several hundred actuators and sensors interconnected by numerous control loops must operate concurrently at sample rates up to 5kHz. Such rates are higher than anything that has been employed in a flight system of this complexity before. It is therefore not surprising to find that the allowable I/O latencies are much smaller than that which can be readily achieved using flight-proven digital interconnect techniques.

A simple approach would be to co-locate all the digital electronics functions so that they all have access to a single high-speed backplane bus such as VME. This is not attractive for the following reasons.

- The performance of a backplane bus declines as its length and the number of connected devices increases.
- It is not possible to prevent faults in a single bus from propagating to the devices connected to it.
- Since many of SIM's sensors and actuators are located several meters apart, some of them would have to be attached to the centralized electronics by long, bulky cable bundles which are often problematic.
- It is difficult to integrate and test a system in which all the electronics is centralized because "nothing works until everything works".

In the approach to be described, the instrument electronics is partitioned into 23 fault containment regions and I/O within each partition is handled by a local VME bus. The partitions are packaged in 17 card cages which can be located several meters apart. The partitions communicate with each other via a low-latency interconnect based on IEEE STD 1596: Standard for Scaleable Coherent Interconnect (SCI).

The architecture of the SIM Instrument will be outlined. Driving requirements in support of the conclusion that none of the available "heritage" interconnects is suitable will be presented. Reasons for choosing SCI as a baseline will be given. Known limitations of SCI will be summarized and an approach to redundancy management will be discussed.