Impact of Print Parameters and CSP Pitch and I/O on Paste Quality and Volume

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ABSTRACT

A JPL-led CSP Consortium of enterprises, composed of representing government agencies and private companies, recently joined together to pool in-kind resources for developing the quality and reliability of chip scale packages (CSPs) for a variety of projects. The experience of Consortium on the build of more than 150 test vehicle assemblies, single- and double-sided multilayer PWBs, and environmental test results now published as a chip scale package guidelines document and is being distributed by Interconnection Technology Research Institute (ITRI).

Assembly of the second test vehicle with 15 packages is currently underway. As part of the assembly, solder paste print quality for mixed CSP and BGA packages was studied in depth at two facilities, Celestica and StorageTek. A series of experiments were performed to establish solder paste deposition with printing process variables. A 3D laser measuring system in conjunction with reference copper traces was used to automatically measure solder paste volume. Quality of print was established by visual inspection. This paper presents the effects of paste printing parameters including stencil thickness, squeegee length and materials, and pressurized head on solder paste volume for packages with pitches from 0.5 mm to 1.27 mm and I/Os from 48 to 784.

INTRODUCTION

In recent years, chip scale packages (CSPs) have emerged as the packaging technology of choice, fulfilling industry's continual need for smaller, faster and lighter performance electronics products. This technology has found many applications in digital camcorder, flash memory cards, mobile phones, and telecommunications.

To investigate the many issues of implementing CSP technology and verifying its reliability, a Consortium led by the Jet Propulsion Laboratory (JPL) was formed to design and build a test vehicle with different types of CSPs [1,2]. Solder joint reliability is affected by many variables including screening process especially for a mixed package technology assembly. Two independent team members assembled a large number of test vehicle #2 (TV-2) and investigated the effects of manufacturing variables on solder paste release. Members assembled test vehicles were:

a) Celestica with extensive experience in ball grid array (BGA) and flip chip attachment process development and goal of integration of CSPs into main stream SMT assembly[3]. Celestica's Customer Oriented Rapid Engineering Lab (CORE Lab, Facility A) completed the assembly of fifty TV-2s in high volume assembly production. Key printing process variables including quality and solder paste volumes for various CSPs and BGAs were established prior to the test vehicle built to understand key process variables and during build to verify previous results and use information for correlation to solder joint reliability.
b) StorageTek (Facility B) with well known implementation of advanced microelectronic packaging for high reliability applications. Thirteen TV-2s were also built at this facility. Solder paste volume also were measured and were compared between the two facilities.

Solder paste deposition quality, i.e., solder paste consistency and volume, is critical to solder joint reliability. It has been shown that $40% of the soldering defects in SMT assembly are associated with the solder paste printing process[4]. This is become even more critical for CSPs with smaller physical features including pitch and solder bump and increase in I/Os.

A series of experiments were performed to establish solder past deposition with printing process variables for package patterns with various pitch and size. Previously, preliminary data on the effects of area aspect ratio of stencil on the amount of solder paste release to understand process variables were presented[5]. This paper will present additional information gathered during assembly of the JPL Consortium test vehicle covering many aspects of print quality and its correlation with manufacturing variables for a mixed package assembly. Reliability aspects were presented in another paper included in this proceeding by other team members of this Consortium[2].

TEST VEHICLE

The printed wiring board (PWB) had an OSP surface finish and a pad size variation from 0.25 mm to 0.66 mm and a pitch variation from 0.5 mm to 1.27 mm. An assembled test vehicle is shown in Figure 1. A section of PWB shown in Figure 2 includes pitches of 0.5, 0.8, 1, and 1.27 mm. Note calibration traces designed close to pads in order to have reference surfaces when pads are covered with paste in order to ease the automatic solder paste volume measurement by a 3D laser system.

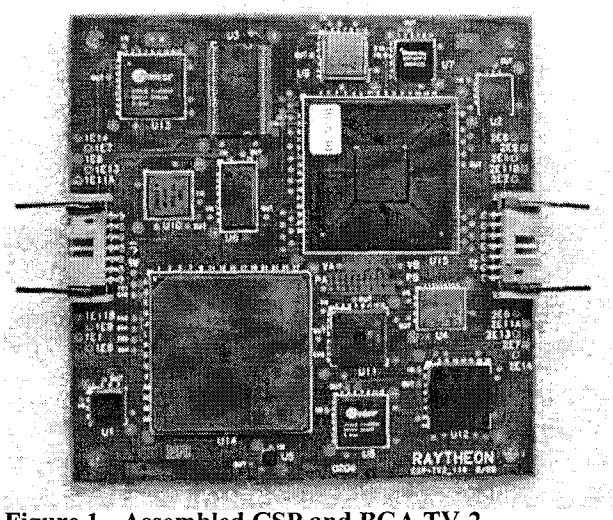

Figure 1 - Assembled CSP and BGA TV-2

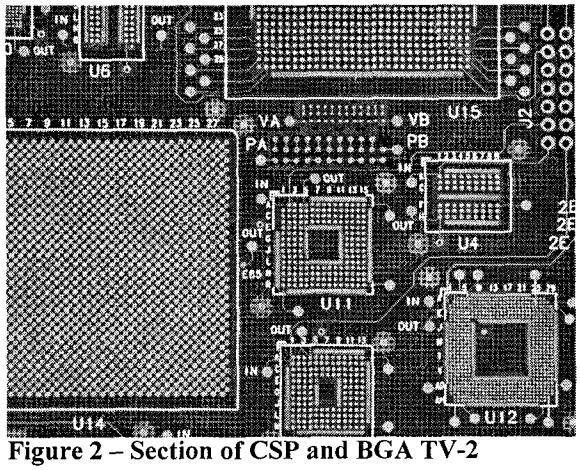

Figure 2 – Section of CSP and BGA TV-2

Experimental Runs and Test Vehicle Build

Experiments were performed prior to the build (herein, Runs) and during test vehicle build (herein, Builds) had some differences. Table 1 lists process parameters for the four experimental Runs and Table 2 lists variables for the four Build assembly.

Run —For the Run investigation, two printers with fine pitch print capability were used and squeegee angles and overhang length were also varied. The variables reflected generic printing processes for a manufacturing line. A pressurized printer head was used to compare against the squeegees. Only six package patterns on PWB out of fifteen were included in the Run experimental analysis.

Build —In the Build study, only one screen printer was used due to availability at the time of test vehicle build. Three different stencils were used during the build were:

- 150 μm (0.006 inch) thick laser-cut and fabricated out of stainless steel. This stencil was also used in the Run experiment
- 125 μm (0.005 inch) thick laser-cut and fabricated out of stainless steel
- 141 μm (0.00565 inch) thick electro-formed out of nickel

Each stencil design incorporated square apertures with rounded corners. The electro-formed stencil incorporated the same aperture design as the 6 mil laser cut stainless-steel stencil. Thirteen out of fifteen PWB package patterns were characterized in the Build experiments.

Table 1: Variables for screening printing of TV-2 for the Run experiment

Experimental Run	Run 1	Run 2	Run 3	Run 4
Equipment	Printer A	Printer A	Printer A	Printer B
Squeegee Angle	45	60	N/A Pressurized Head	60
Squeegee Blade Overhang	5 mm	15 mm	N/A Pressurized Head	22
Print speed	Standard	Standard	Standard	Standard
Pressure	Standard	Standard	Standard	Standard

Table 2 Variables for screening printing of TV-2 for the Build experiment

Assembly Build	Build 1	Build 2	Build 3	Build 4
Equipment	Printer B	Printer B	Printer B	Printer B
Squeegee Angle	60	60	60	60
Squeegee Blade Overhang	22 mm	22 mm	22 mm	22 mm
Print speed	Standard	Standard	Standard	Standard
Pressure	Standard	Standard	Standard	Standard
# of PWBs	12	13	5	5
Stencil used	6 mil Laser cut	5.65 Efab Stencil	5.65 Efab Stencil	5 mil Laser cut

Paste Print And Volume Measurement

The study included a no-clean paste, type III (-325+500) mesh, with a metal content of 90.25% and a viscosity of 900-1000 Kcps at room temperature (22 °C). Each printed wiring board (PWB) was visually inspected after screening for gross defects such as bridging or insufficient paste. Pastes were screened on the acceptable PWBs using normal manufacturing parameter setup. Registration of solder paste was ensured through normal solder paste printing protocols using sample PWBs and optical microscopy. Once the registration of the print met manufacturing standards, the PWBs were printed. After each print the underside of the stencil was wiped out automatically or manually with a lint free cloth.

After screen print completion, solder paste volumes were measured by an automated 3-D vision inspection machine. The precision and confidence level of the data was assured by using multiple measurement cycles. This process was carried out for the four different setups during the Run experiment and Build of test vehicle.

TEST RESULTS PERFORMED AT FACILITY A

The paste volume released by the screening process changes as the pad size decreases from BGA to CSP. Two parameters were considered to establish such changes:

- Release rate (percentage ratio of measured paste volume to a calculated theoretical volume)
- Aspect ratio (ratio of wall area to aperture area)

Relationship between the two for the many Runs and Builds were characterized.

Consistency or variability of the screening process, i.e. variation for different sites of a package pattern in a PWB and different PWBs were also determined using an analysis of variance (ANOVA) statistical approach. The process variation was calculated as a percentage of the theoretical volume for each site in PWB or an average of sites for a PWB based on a six-sigma process. Variation values then were normalized with respect to the theoretical volume for each individual case. Detail test results are discussed below.

Correlation of Paste Volume with Aspect Ratio

Figure 3 shows the relationship between release rate and aspect ratio for the Run experiment. The relationship between the release rate and the aspect ratio was assumed to be linear even though there appears non-linearity at the two extremes. A similar relationship was found for the Build experiment as shown in Figure 4. The data for Builds 2 and 3 were combined since the same stencil was used in both cases. In general, as aspect ratio increases the release rate also increases. The rate of increase depends on the Run or Build condition. For example, the Run 4 release rate was more sensitive to the aspect ratio than the other Runs. The thicker stencil used in the Build 1 showed less sensitivity to aspect ratio compared to other Builds with thinner stencil.

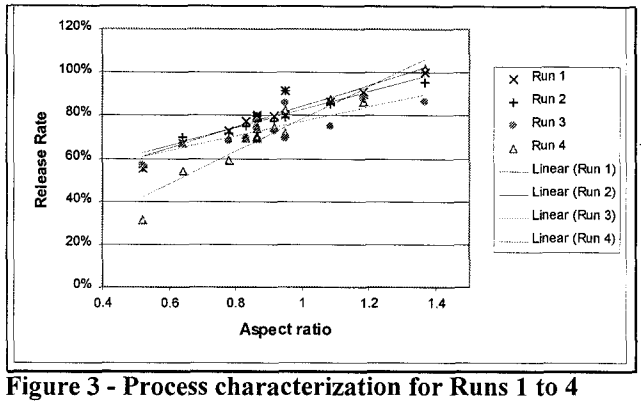

Figure 3 - Process characterization for Runs 1 to 4

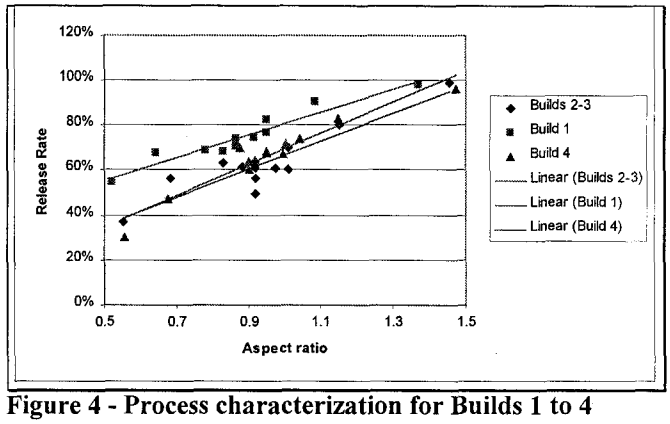

Figure 4 - Process characterization for Builds 1 to 4

Also note that the Run 1 and Build 4 have the same process condition including the same stencil thickness, except for the time of experiment. Figure 5 shows the release rates for the Run 4 and Build 1. Even though both experiments show linear correlation, however, the release rate for the Build was less sensitive to aspect ratio than the Run experiment. In addition, the release rate was about 20% was higher for the Build than the Run at the lowest aspect ration of 0.5.

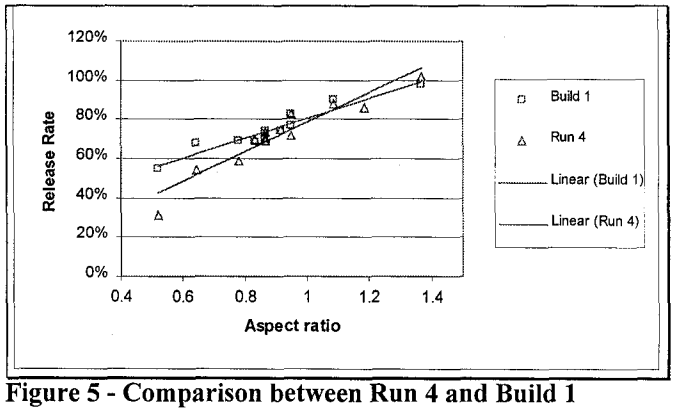

Figure 5 - Comparison between Run 4 and Build 1

Effect of Stencil Type on Release Rate

The stencil manufacturing type has a direct impact on the

release rates. For example, the release rates for the electro-formed stencils were more scattered (Builds 2 and 3) than laser cut version (Build 1 and 4) as shown in Figure 4. This scatter can be attributed to the nature of the electro-formed stencil. The nominal thickness for this stencil was 5.65 mil +/- 0.5mils. The thickness was based on the inside walls of the aperture.

Contrary to stainless steel stencils (+/- 0.4 mils), which are made of sheet metal an electro-formed stencil is grown on a mandrel from a solution. The solution contains nickel ions, which are discharged by an electric current and deposited on the mandrel containing a negative pattern of the stencil design. The density of the apertures of a site on the mandrel determines the growth rate of the nickel. As a result the areas of the stencil with higher density may have a greater deposition rate than other areas and will result in a greater thickness of nickel at that site.

It is noteworthy to mention here that the vendor from whom this stencil was obtained was still in the development stages of the manufacture of electro-formed stencils. The results presented here do not reflect the results that would be obtained for all electro-formed stencils.

The variation in the thickness of an electro-formed stencil greatly affects the actual aspect ratio of the stencil compared with the original stencil design. As a result the true aspect ratio of the stencil should be determined by direct measurements of the stencil thickness and aperture dimensions. This implies that the relationship between the release rate and aspect ratio should be more carefully investigated to determine the true trend for the electro-formed stencil. The aspect ratio used in Figure 4 was the theoretical value based on stencil design. A different aspect ratio would probably obtained for different apertures compared to the original stencil design. As a result the relationship between release rate and aspect ratio may have resulted in a true trend than what was observed initially.

The theoretical aspect ratio was also used for the laser cut stencils instead of the true or measured aspect ratio. But in this case, since the thickness of sheet metal is a more carefully controlled process, the aspect ratio of these stencil designs was taken as a good approximation to the true value. As a precaution though measuring the actual stencil aperture dimensions of the laser cut stencils would be an important exercise.

Consistency of the Screening Process for the Runs and Builds

The variation in processes were compared for different PWBs and sites on a PWB using two factor ANOVA analysis with replicates. For example, the size of package pad and therefore stencil opening will affect solder paste release. Clogging of aperture opening was observed more often for CSPs with 0.5 mm pitch that larger pitches. Figure 6 includes release rate as well process variation with aspect ratio for the Run 1. As expected, the process inconsistency decreases as aspect ration increases, from 20% for 0.5 ratio to 5% for 1.2 ratio. A similar trend was observed for experimental Runs of 2 and 3. However, the variation for the Run 4 was different and showed a parabolic relationship as shown in Figure 7. Variations are minimum (about 10 %) at about 0.9 aspect ratio with the extreme values of about 40% and 30% at 0.5 and 1.35 ratios, respectively.

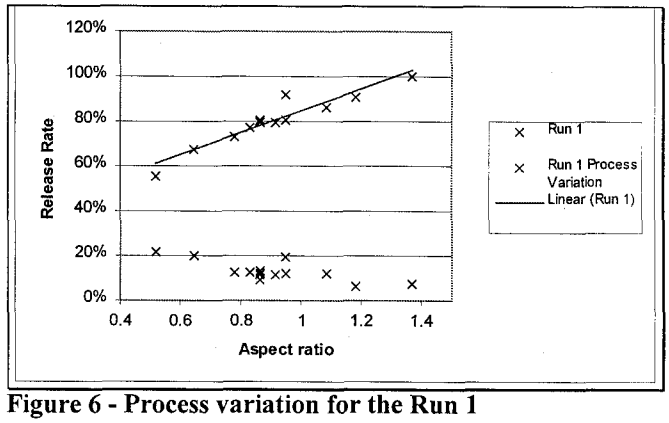

Figure 6 - Process variation for the Run 1

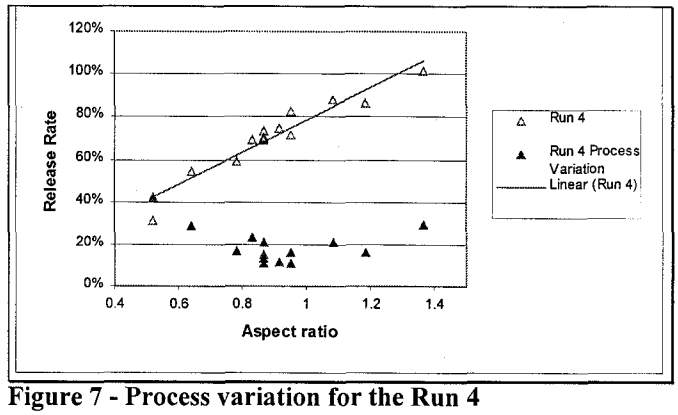

Figure 7 - Process variation for the Run 4

Verification of these results was an important step in determining the cause of this discrepancy. The process variation for the Build 1 is shown in Figure 8. A similar trend was also observed for the Run 4 as shown in Figure 9. The process variation value at 0.5 aspect ratio is high and is about 40%, it reduces to 15% at 0.85, and then increases to 33% at higher ratio of 0.9.

The cause for this no-linearity trend in process variation value with aspect ratio is not well understood and is the focus of a future study. In addition the Builds had higher process variation than the Runs in the range of 0.6 to 1 aspect ratio. The cause for this difference was also not determined at the present time. Possible causes include the use of different screening machine, paste from different lots, difference in operator skill.

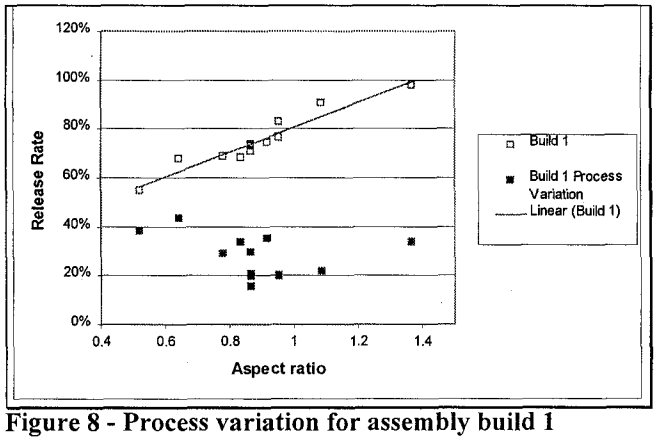

Figure 8 - Process variation for assembly build 1

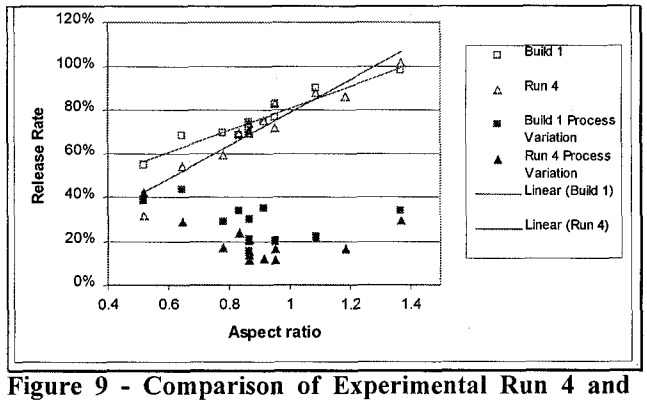

Figure 9 - Comparison of Experimental Run 4 and Build 1

Consistency of Screening Process for Different PWBs and Pads

One of the useful advantages of an ANOVA is that the contribution of the general process variation can be narrowed to a more specific parameter. The PWB to PWB variation of the process with aspect ratio is shown in Figure 10 for the Run 4 and the Build 1. The pad to pad variation for a site with aspect ration is shown in Figure 11 for Run 4 and Build 1.

Comparison of the two figures shows that the contribution of pad to pad variation is more significant that PWB to PWB variation. In addition the PWB to PWB variation for Run 4 shows a similar decreasing trend to the variation observed in the Run 1. This implies that although the process was consistent from PWB to PWB in Run 4 and Build 1, there was more variation from pad to pad of a site in a PWB. This also implies that there were discrepancies associated with or inherent to the process. The contributing factors could have been inconsistencies in the stencil apertures, position of the apertures of a site with respect to the PWB, direction of the roll of the paste during printing as well as other variables attributed to the equipment setup and operation.

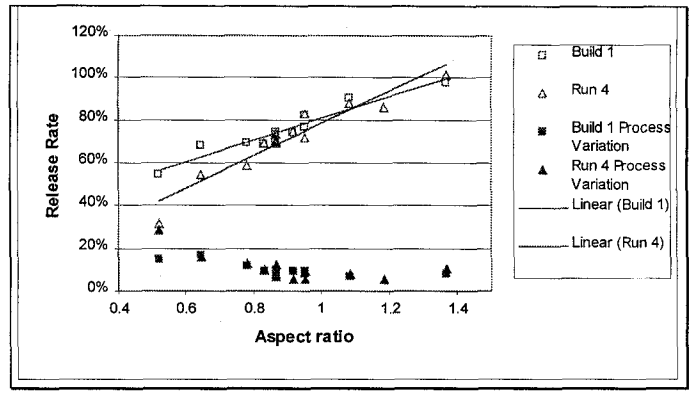

Figure 10 - Comparison of Run 4 and Build 1 for PWB to PWB variation

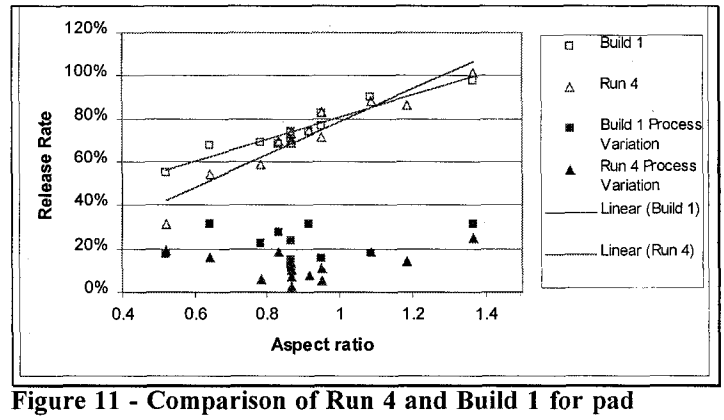

Figure 11 - Comparison of Run 4 and Build 1 for pad to pad variation

TEST RESULTS PERFORMED AT FACILITY B

Solder paste volume was also measured at Facility B during assembly of twelve test vehicles. Table 3 summarizes the measure paste volume versus theoretical values. The shaded rows with package identifications (U8, U9, U11, U14, U15) are suspect data and therefore were not considered in the plots of Figure 11. For the theoretical volume calculation, the stencil opens were all measured and actual measurement instead of design data was used.

Discussion: Paste and Solder Joint Reliability for CSP Technology

The integration of CSPs into current manufacturing process using standard SMT practices may require process similarity with higher pitch packages that also maximizes CSP reliability. The effect of solder paste volume on the reliability of CSPs is yet to be determined, but it is assumed to be dependent on the amount of paste deposition during manufacturing processes. An increase in solder paste to a certain level, should improve solder joint reliability, even though such relationship is not yet established. To achieve higher manufacturing yield as well as improved reliability, key printing process parameters and control of paste deposition consistency are needed to be understood. In-depth characterization

provided here were aimed towards understanding the key parameters that are needed to be controlled for solder paste process optimization as well defining relationship between solder paste volume and reliability.

Table 3 Percent Release Rate and Aspect Ration for Various Packages (Facility B)

Location	Average Measured Volume	Theoretical Volume	Percent Release	Aspect Ratio
U1	1204	1574	76	0.95
U10	232	373	62	0.77
U11	1232	1402	88	0.92
U12	333	460	72	0.62
U13	1218	1436	85	0.91
U14	3103	3269	95	0.91
U15	1965	1900	103	0.83
U2	1374	1692	81	0.87
U3	4741	5267	90	0.61
U4	1460	1812	81	0.76
U6	1299	1617	80	0.83
U7	1693	1881	90	0.85
U8	1550	1511	103	0.90
U9	1479	1822	81	0.82

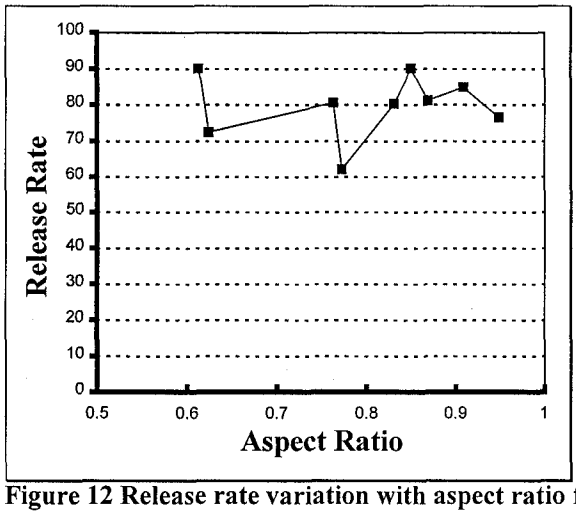

Figure 12 Release rate variation with aspect ratio from data generated at Facility B

CONCLUSIONS

Facility A

The in-depth investigation carried out at Facility A indicates that:

- Solder paste deposition quality (volume and consistency) is related to the aspect ratio of the stencil and the equipment and screen print parameters
- For CSP's to be integrated into the regular assembly process, printing results should approach that of BGA's with highest release rate and process consistency.
- Printing process and paste deposition is required to optimized and controlled for a mixed technology assembly with CSPs to assure reliability of assembly.

Facility B

- Limited data gathered at Facility did not show a strong correlation trend between release rate and aspect ratio determined at Facility A. Further investigation with much larger sample sizes are required to better understand the reasons for such difference

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REFERENCES

1. Ghaffarian, R. "Chip Scale Packaging Guidelines", Distributed by Interconnection Technology Research Institute, http://www.ITRI.org
2. Ghaffarian, R., et al "Thermal Cycling Test Results of CSP and RF Package Assemblies", SMT International Proceedings, Sept., 2000
3. Chen, L.A., Sterian, I., Smith, B., Kirkpatrick, D. (1999), "CSP Compatibility in the SMT Assembly Process", Soldering & Surface Mount Technology, Volume 11 No. 2, pp. 25-19.
4. Clouthier, R.S., "SMT Printing Process For Fine And Ultra Fine Pitch", pp. 674-686, Surface Mount International, San Jose, CA., September 7-11, 1997.
5. Ghaffrian, R., Achong C., Mehrotra, M., "Assembly and Cleaning of CSP's for Hih, Low, Ultra-Low Volume Appications", APEX Electronic Assembly Process conference proceedings, Long Beach, CA, March 12-16, 2000, Session P-AP8/3
6. Chen, L.A., Sterian, I., Smith, B., Kirkpatrick, D. (1999), "CSP Compatibility in the SMT Assembly Process", Soldering & Surface Mount Technology, Volume 11 No. 2, pp. 25-19.