Military & Aerospace / Avionics
COTS Conference
August 22-25, 2000

Commercial Off-The-Shelf (COTS) Program
Methodology and Results of Upscreening Electronic Parts - An Update

Mike Sandor, Shri Agarwal
4800 Oak Grove Drive
Pasadena, CA 91109
Phone: (818) 354-0681 FAX: (818) 393-4559

AGENDA:

ADVOCACY FOR COTS
DRAWBACKS WHEN IMPLEMENTING COTS
JPL COTS++ CRITICAL SCREENING FLOW
JPL COTS++ CRITICAL QUALIFICATION
COST & SCHEDULE TRADEOFFS
COTS++ Upscreening Results
C-SAM Update and Ongoing Work
COTS DPA Failures
SUMMARY
Advocacy for Using COTS (plastic packages):

1. State-of-the-art parts are mostly available as COTS
2. COTS plastic parts performance capabilities continue to increase (e.g., processing power & high density memories)
3. COTS plastic parts enable reduction of hardware weight and volume
4. COTS plastic parts initial acquisition cost is less than ceramic
5. COTS plastic parts have been reported to demonstrate good to excellent reliability in commercial and aerospace applications
6. Often they are the only option when Grade 1 is not offered or available

Drawback to COTS Implementation (plastic packages):

1. Upscreening cost is coupled to the following influences and therefore cannot be tightly controlled (no standard exists)
   - Finding suitable test expertise
   - Minimum quantities often dictate cost
   - Manufacturers unwillingness to upscreen
   - Costs of ownership depends on risk accepted
2. Upscreening schedules can jeopardize project schedules unless
   - Flows and processes are in writing & approved
   - Engineering/QA help is available daily
   - Vendor commits to screening schedule
   - Material in-process status is monitored weekly
3. Risk is not totally eliminated with upscreening
Competitive bidding demonstrates cost & schedule selection tradeoffs

Likelihood of Part Failure Vs Cost for Space Flight Applications

- Cost Legend:
  - Variables are
    - 1. OEM
    - 2. Cost
    - 3. Leadtime
    - 4. Subassemblies
    - 5. Volume
  - Risk Mitigation
    - 1. Application
    - 2. Requirements
    - 3. Reliability
    - 4. Design
  - Replacement Detail Launch
    - 1. Baumeister
    - 2. System
    - 3. Subassembly
    - 4. Board
    - 5. Compliance
More Risk Management is Needed:

JPL/NASA Project Drivers:
- Must infuse the latest technology
- Must significantly reduce development costs
- Must significantly reduce development time
- Per NASA, Better, Faster, Cheaper is here to stay

Average Development Costs  Average Development Time  Average Flight Rate

$500M  $75M  16 Launches/Yr
FY90  FY04  FY90  FY04  FY90  FY04
8  <3  2

COTS PEM Risk Mitigation Addresses the Following Concerns:
- Narrow Temperature Range for Commercial Grade
- Plastic Assembly Quality
- Lot Non-Uniformity & Traceability (including radiation)
- Adequacy of Vendors Testing
- Infant Mortality
- Die Construction and Quality
Radiation Issues of Using COTS for Space Applications:

Rad Hard Assurance Varies from the same processing lot

Radiation Assurance has little statistical confidence

TID response depends on process-
"Positive" process changes can reduce radiation tolerance

SEE depends on circuit design and dimensions-
Commercial vendor can change these without notice

No good way of predicting radiation response without extensive testing-
Exception is a controlled Rad Hard process line

Radiation risk mitigation techniques are often required- $$\$$

---

Methods to Insure Low Risk COTS in Critical Space Applications

**Target Guidelines**

- **15 yr mission:**
  - JPL Upscreen/Qual
  - Derate/WLA/RLAT/DPA/OML

- **10 yr mission:**
  - JPL Upscreen/Qual
  - Derate/WLA/RLAT/DPA/OML

- **5 yr mission:**
  - JPL Upscreen/Qual
  - Derate/RLAT/DPA/OML

- **≤1 yr mission:**
  - JPL Upscreen
  - DPA/Generic Data
COTS++ PEM Upscreen Impact on Risk Mitigation

<table>
<thead>
<tr>
<th></th>
<th>Amplifier</th>
<th>ADC</th>
<th>DC-DC Conv.</th>
<th>Reg.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Narrow Temp.Range for Commercial Grade</td>
<td>1</td>
<td>1</td>
<td>3</td>
<td>9</td>
</tr>
<tr>
<td>Plastic Assembly Quality</td>
<td>3</td>
<td>9</td>
<td>9</td>
<td>1</td>
</tr>
<tr>
<td>Lot Non- Uniformity &amp; Traceability</td>
<td>1</td>
<td>9</td>
<td>3</td>
<td>3</td>
</tr>
<tr>
<td>Adequacy of Vendors Testing</td>
<td>1</td>
<td>9</td>
<td>3</td>
<td>9</td>
</tr>
<tr>
<td>Infant Mortality</td>
<td>1</td>
<td>9</td>
<td>1</td>
<td>9</td>
</tr>
<tr>
<td>Die Construction and Quality</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

Total Score: 8, 38, 20, 31
COTS++ impact on lowering risk: Low, High, High, High
Fallout: 4%, 85%, 26%, 25%

Risk mitigation weighting factors used: Minimum = 1, Moderate = 3, Significant = 9

---

COTS++ Upscreening Rejects by Part Type & Vendor

<table>
<thead>
<tr>
<th></th>
<th>Amplifier- A</th>
<th>ADC- B</th>
<th>ADC2- B</th>
<th>DC-DC Conv.-C</th>
<th>Voltage C/A</th>
<th>S. Regulation-B</th>
</tr>
</thead>
<tbody>
<tr>
<td>DPA:</td>
<td>0/4</td>
<td>1/8</td>
<td>TBD</td>
<td>0/4</td>
<td>0/4</td>
<td>0/4</td>
</tr>
<tr>
<td>Incoming:</td>
<td>0/78</td>
<td>n/a</td>
<td>0/78</td>
<td>1/78</td>
<td>0/80</td>
<td>8/80</td>
</tr>
<tr>
<td>C-SAM:</td>
<td>3/78</td>
<td>38/78</td>
<td>5/75</td>
<td>5/77</td>
<td>5/80</td>
<td>5/80</td>
</tr>
<tr>
<td>Temp Cycle:</td>
<td>0/78</td>
<td>10/78</td>
<td>0/75</td>
<td>3/77</td>
<td>0/80</td>
<td>3/72</td>
</tr>
<tr>
<td>Burn-In:</td>
<td>0/78</td>
<td>3/68</td>
<td>0/75</td>
<td>0/74</td>
<td>0/80</td>
<td>9/69</td>
</tr>
<tr>
<td>QCI:</td>
<td>0/10</td>
<td>0/10</td>
<td>TBD</td>
<td>0/10</td>
<td>0/10</td>
<td>0/10</td>
</tr>
<tr>
<td>Total:</td>
<td>3/78</td>
<td>51/78</td>
<td>TBD</td>
<td>20/78</td>
<td>5/80</td>
<td>20/80</td>
</tr>
</tbody>
</table>

JPL 8-24-00
Failure Mechanisms from PEM Delamination:

- Stress-induced passivation damage over the die surface
- Wire bond degradation due to shear displacement
- Accelerated metal corrosion
- Die attach adhesion
- Intermittent electricals at high temperature
- Popcorn cracking
- Die cracking

<table>
<thead>
<tr>
<th>Part Type</th>
<th>Manufacturer</th>
<th>Yield</th>
</tr>
</thead>
<tbody>
<tr>
<td>NPN Transistor 1</td>
<td>A</td>
<td>83%</td>
</tr>
<tr>
<td>Switching Diode</td>
<td>A</td>
<td>0%</td>
</tr>
<tr>
<td>NPN Transistor 2</td>
<td>A</td>
<td>100%</td>
</tr>
<tr>
<td>Zener Diode</td>
<td>A</td>
<td>50%</td>
</tr>
<tr>
<td>NPN Transistor 3</td>
<td>A</td>
<td>100%</td>
</tr>
<tr>
<td>Op-Amp 1</td>
<td>B</td>
<td>87%</td>
</tr>
<tr>
<td>Op-Amp 2</td>
<td>C</td>
<td>0%</td>
</tr>
<tr>
<td>Op-Amp 3</td>
<td>C</td>
<td>7%</td>
</tr>
<tr>
<td>Phase Detector</td>
<td>D</td>
<td>100%</td>
</tr>
<tr>
<td>Mini Circuit</td>
<td>E</td>
<td>40%</td>
</tr>
</tbody>
</table>

Results are package/vendor assembly dependent.
Lot sizes range from 15-30 parts each.
## A New Failure Characterization Study

is Underway Utilizing Plastic Part C-SAM Rejects

**Objectives:**

- Identify C-SAM reject parts by criteria(s)
- Measure Material Properties including sonic test, IR, X-ray
- Apply extreme temperature cycle stresses
- Repeat Material Properties Measurements including C-SAM at different intervals
- Identify all failure mechanisms and risk rate C-SAM rejects

### J-STD-035
(Acoustic Microscopy for Non-Hermetic Encapsulated Electronic Components)

Source: Sonoscan Inc.
A Failed Chip Scale Board Assembly is under investigation utilizing C-SAM inspection on components/board

Objectives:
- Identify component delaminations
- Identify board layer delaminations
- Make correlation to CSP package thermal cycle failures
  - CTE Mismatch
  - Package Proximity and Location on Board
  - Ball Bond Size and Location

Updated Examples of COTS Parts/Die Failing DPA

Op Amp

PROM

Metallization anomalies are the predominant failures
Summary/Conclusions:

- The concerns/risks anticipated with using COTS PEMS can be reduced to acceptable medium risk levels using JPL upscreening.

- A part qualification plan has been added to JPL's existing screening flows to further insure the reliability of parts used by Projects when application requirements are different.

- Further investigations/studies are being conducted on individual components and board assemblies using C-SAM analysis. This information will provide more understanding of the correlation between delamination and component/board failure mechanisms.