Evaluation of the Sensitivity of Newly Emerging FD-SOI Technologies to Low Temperature and Radiation Environment in Space

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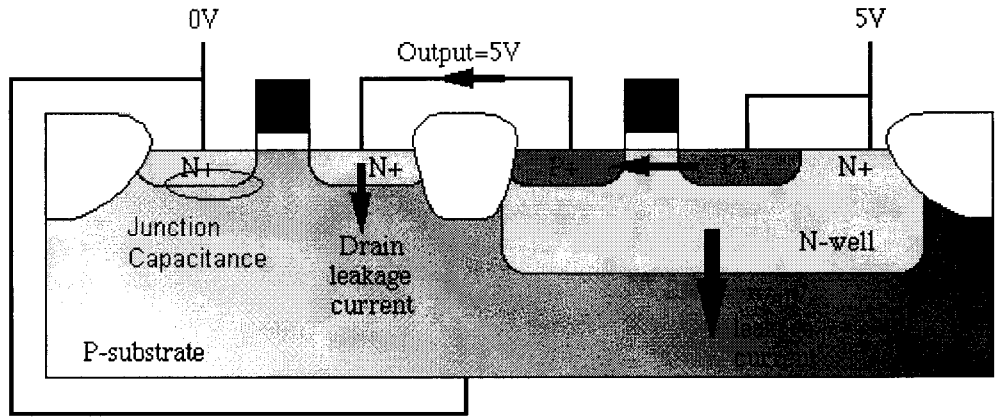
Overview

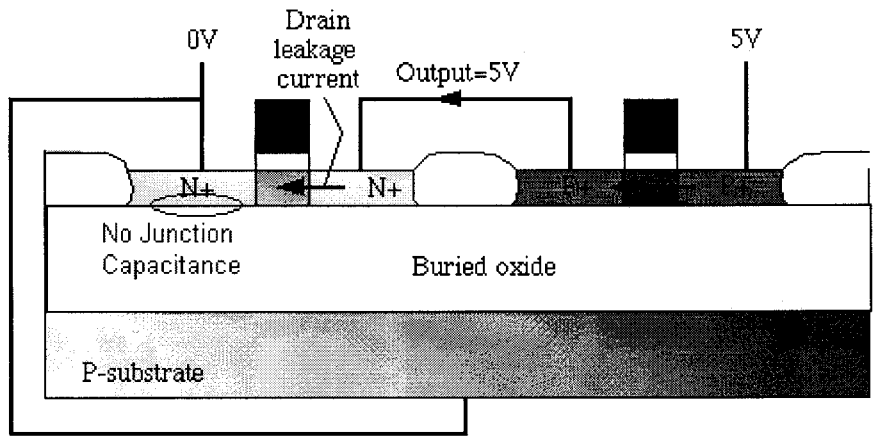
- Performance advantages of Silicon-On-Insulator (SOI) technology over conventional bulk technology
- Cold temperature operation and relevance to space applications
- Performance after proton irradiation
- Summary

SOI Technology Advantages

- Radiation Tolerance
  - *Latchup immune*
  - *SEU: potentially significant improvement*
- Low Power, <1.5V
  - *Lower leakage current*
  - *Lower parasitic capacitance*
- High Density
  - *1 Gbit DRAM, Hyundai*
  - *0.025um devices possible*
- Digital, Analog, Mixed, RF, and Optical Applications all on one chip

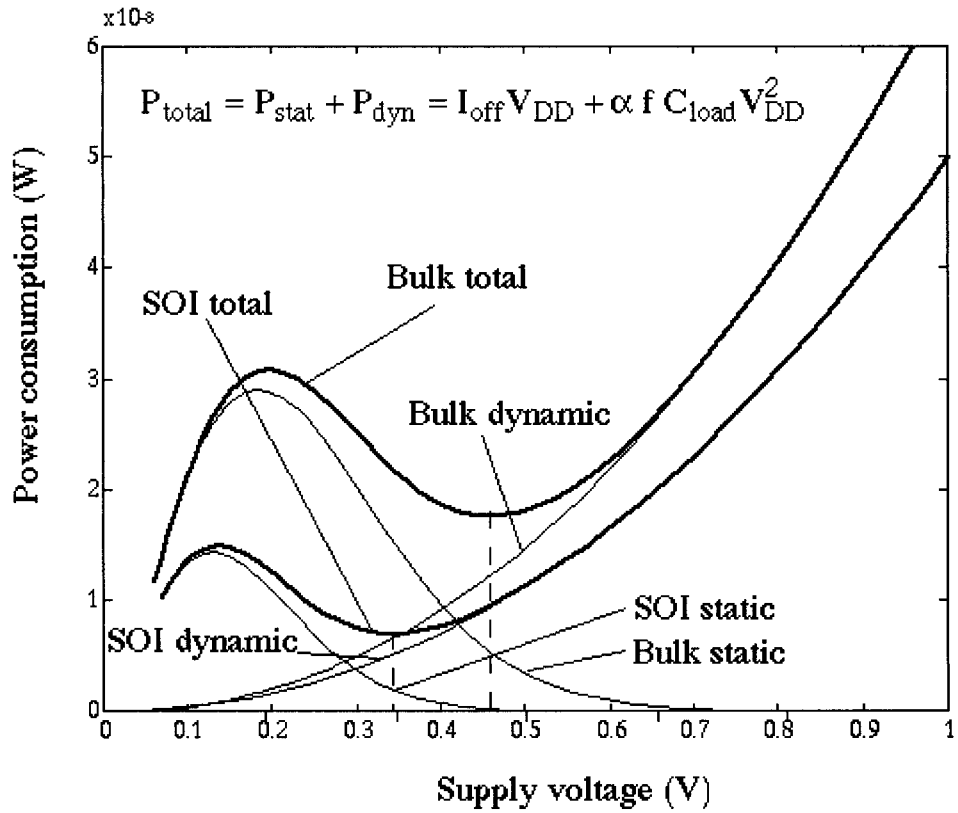
Bulk vs. SOI



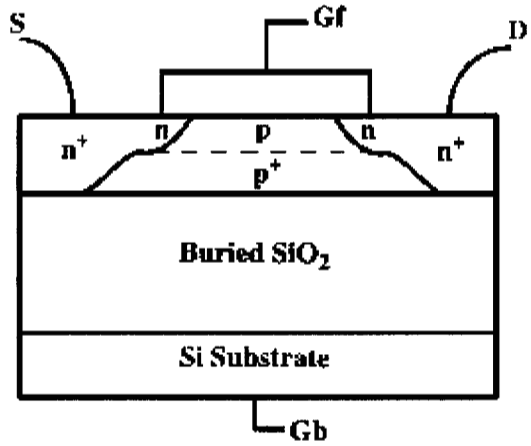


Performance Comparisons between SOI and Bulk

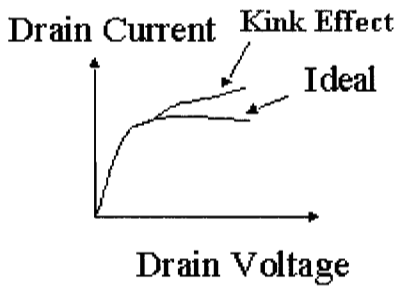
Power Consumption Comparison for SOI and Bulk Technologies



Partially-Depleted SOI (PDSOI)



Failure Mechanism 1: Kink Effect



Failure Mechanism 2: Hot Carrier Degradation

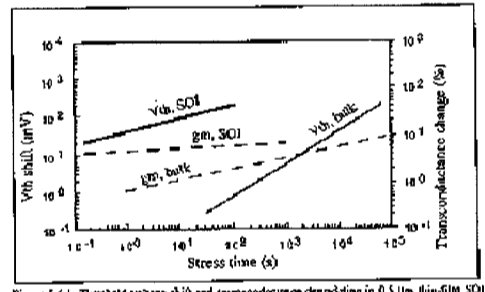
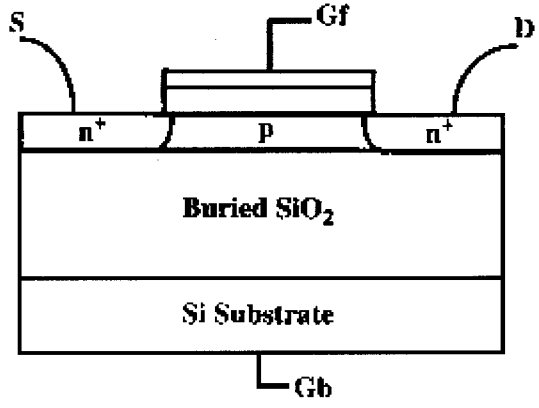


Figure 5.64: Threshold voltage shift and transconductance degradation in 0.5 μm thin-film SOI and bulk n-channel transistors as a function of stress time. V_{GS}=0 V, V_{DS}=6 V.[38]

Fully-Depleted SOI (FDSOI)



Failure Mechanism 1: Floating Body Effect

Causes transient effects and hysteresis. Threshold voltage tends to shift.

Must make backgate contact to avoid the problem.

FD-SOI is harder to fabricate. However, it is preferable due to potential performance improvements

Failure Mechanism 2: Hot Carrier Degradation

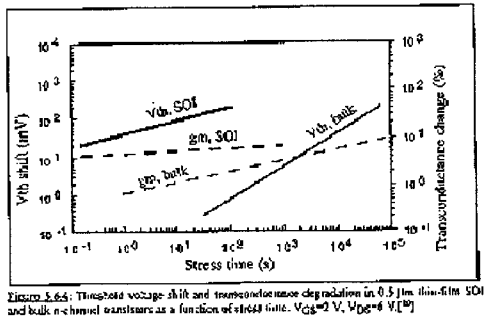
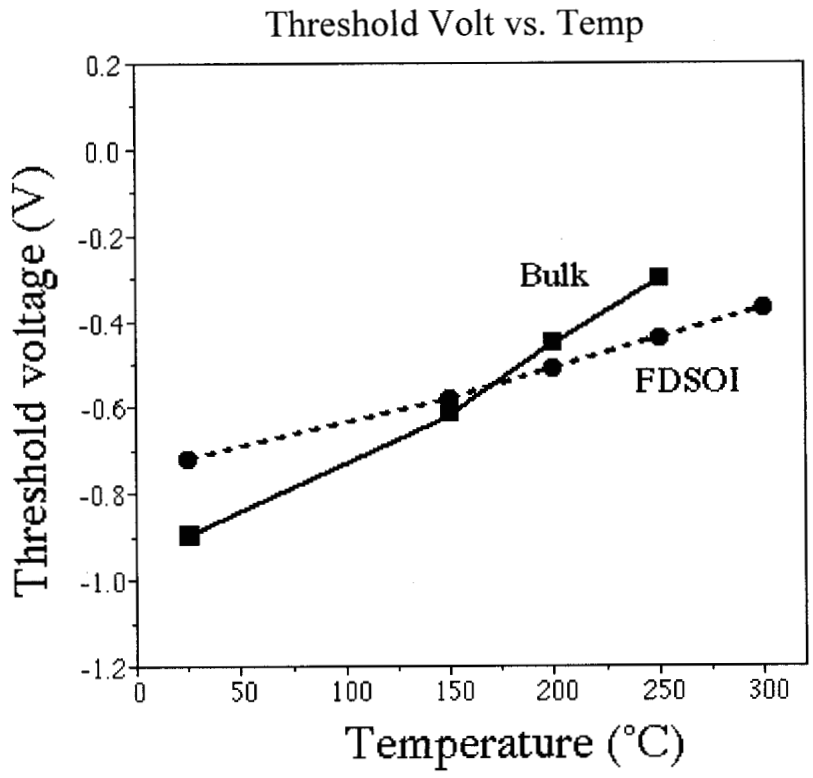


Figure 5.64: Threshold voltage shift and transconductance degradation in 0.5 μm thin-film SOI and bulk n-channel transistors as a function of stress time. V_{GS}=2 V, V_{DS}=4 V.[19]

Special Considerations for Space Applications

In addition to the mentioned performance advantages, SOI technology is particularly well suited for space applications. Devices that can operate reliably in harsh environments, without temperature regulation, can provide valuable energy savings.

The threshold voltage variation with temperature is more than two times smaller in SOI than bulk devices.



Low Temperature Experiments

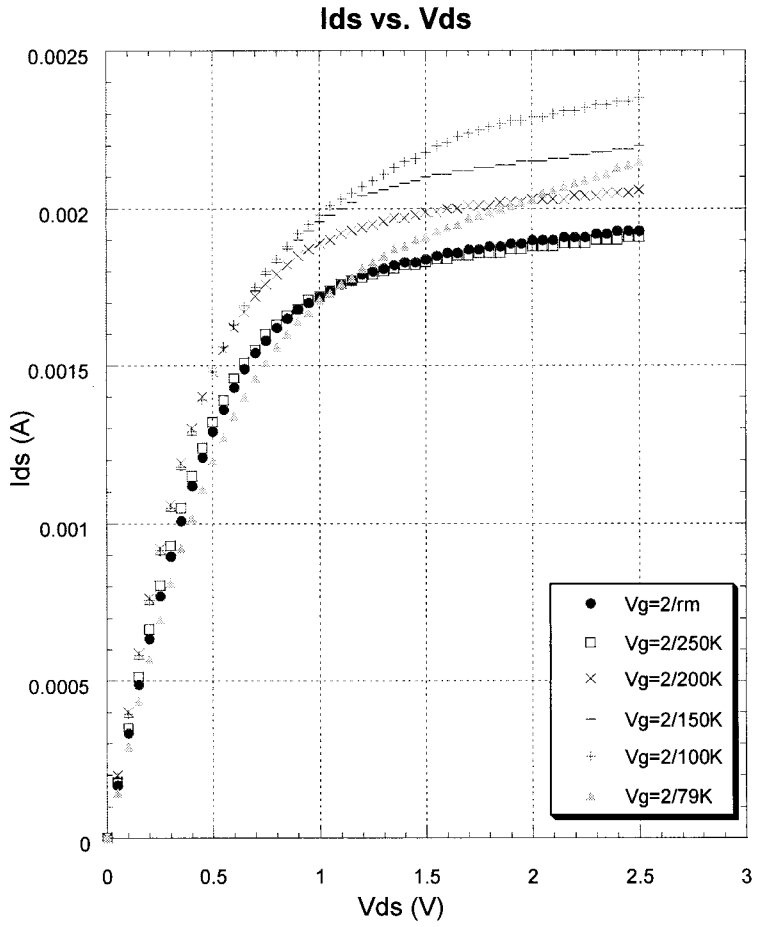
Parameters of Interest:

- Drain Current
- Threshold Voltage
- Effective Mobility
- Subthreshold Slope

Sample Size:
3 NMOS, 3 PMOS, all from one chip

Devices	Channel length	Si film (t_{Si})	Film doping	T_{ox}	BOX	Width
MIT-LL FD-SOI Transistors	.25, 0.30, 0.35um	50nm	3.5×10^{17}/cc	7.5nm	190nm	8um

Drain Current



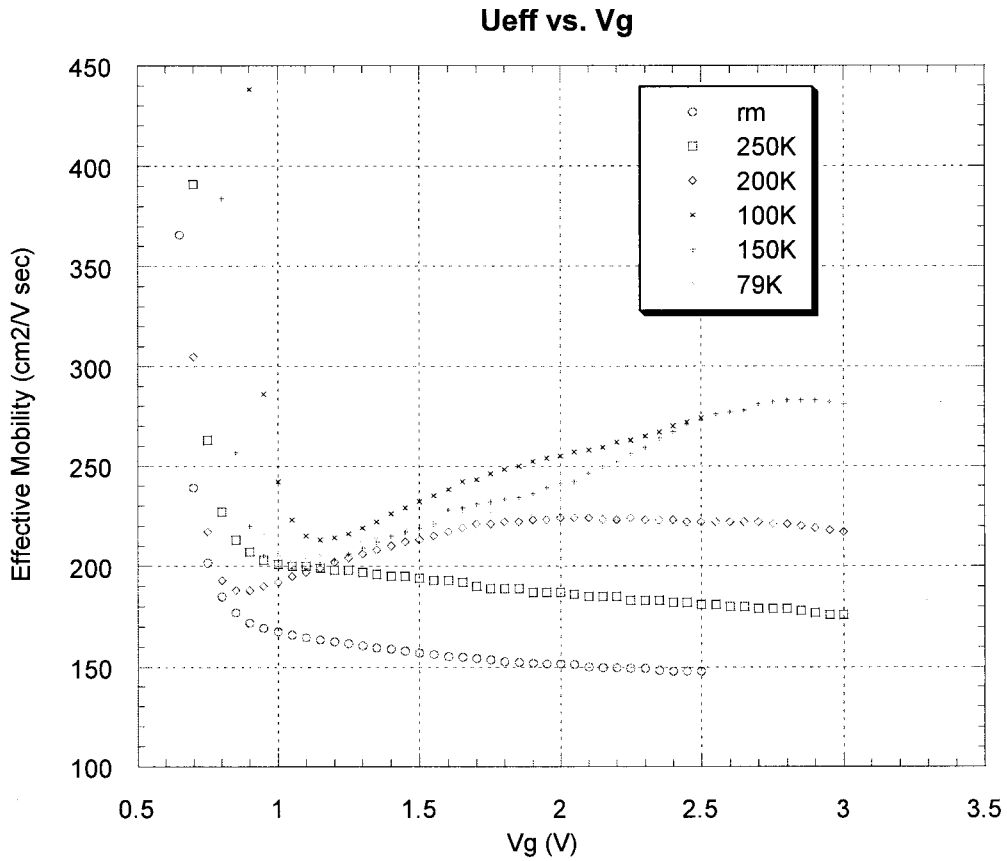
With 2V applied at the gate, the drain current increased as temperature decreased down to 100K. Below 100K, the current started to decrease.

Gradual degradation of the slope in the saturation region was observed as temperature decreased.

One explanation for the observed result is competition between the carrier mobility evolution and the shift of the threshold voltage.

Effective Mobility

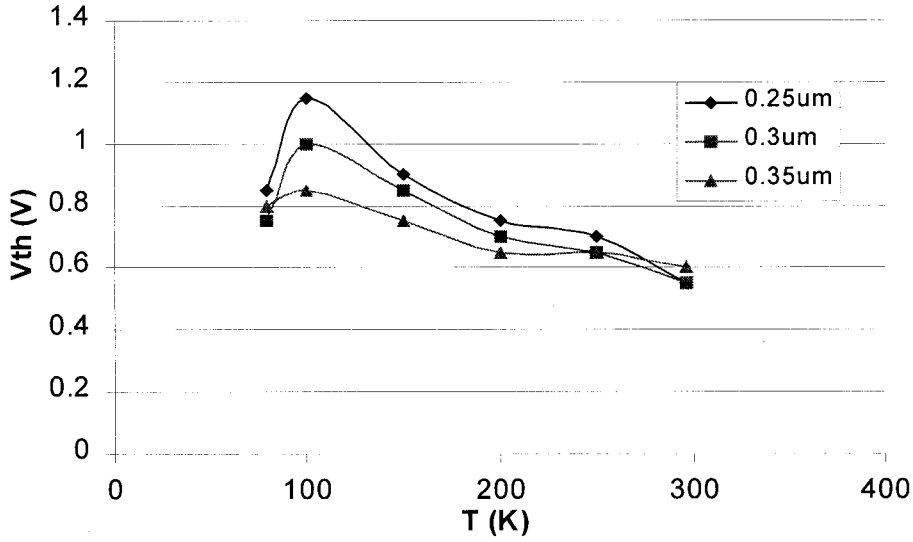
Electronic Parts Engineering



For this 0.35um NMOS, as temperature decreased, the mobility increased down to 100K, and decreased below 100K. This was directly correlated to the drain current behavior.

Threshold Voltage

Vth vs. Temp

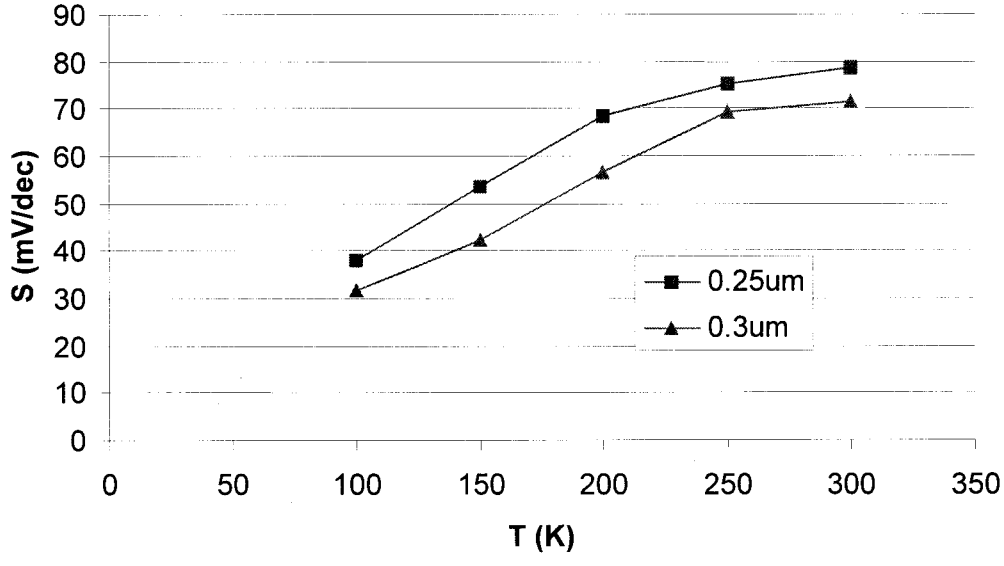


The threshold voltage increased with decreasing temperature in the range from 300K to 100K, and decreased below 100K.

Therefore in the temperature range from 300K to 100K, the drain current increased due to the predominant increase of mobility over threshold voltage. Below 100K, the decrease in mobility overcame the decrease in threshold voltage, leading to a decrease in drain current.

Subthreshold Slope (S)

S vs. Temp for 0.25 and 0.3um NMOS



The Subthreshold slope improves with decreasing temperature, which indicates the transistor is turning on faster.

Radiation Evaluation

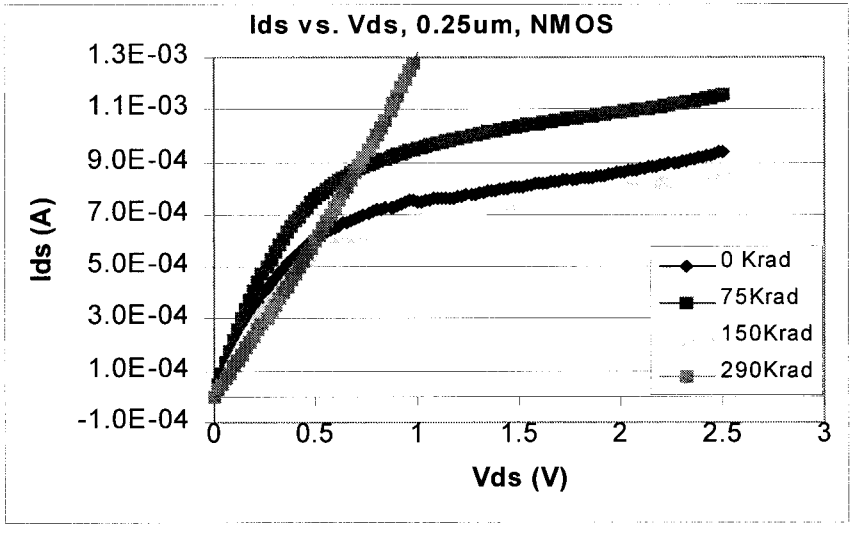
Sample size: 2 NMOSFETs, 3 PMOSFETs, all from one chip

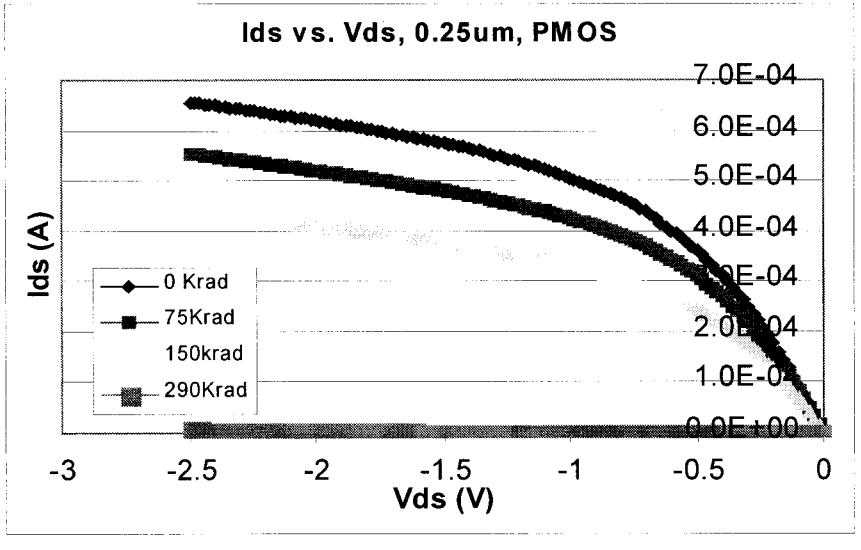
Bias: All pins were grounded

Radiation Source: 200MeV proton source,
Bloomington, Indiana

Drain Current

Electronic Parts Engineering



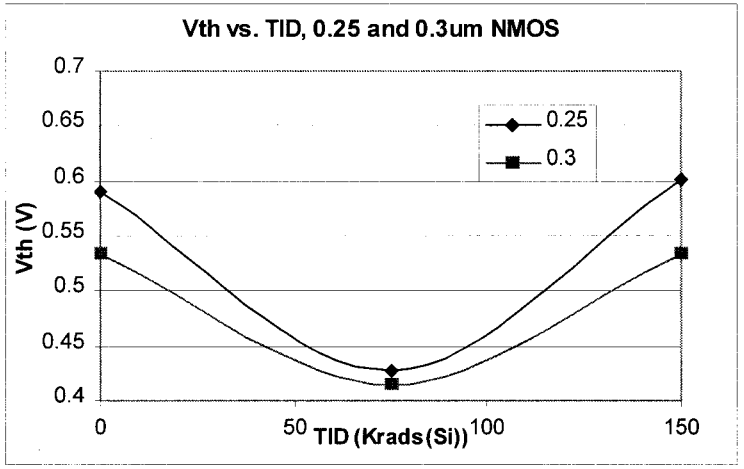


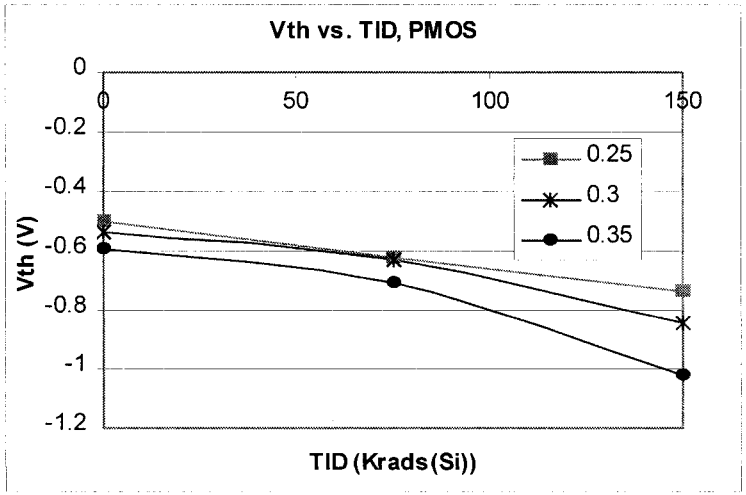
The transistors survived up to 150Krads(Si). Previous experiments have shown that transistors irradiated with X-rays are less susceptible. To verify that proton sources consistently cause more damage than X-rays, more data must be collected on a larger sample space.

We also noticed that the drain current reached a peak at 75Krads(Si) for NMOS, and steadily decreased for PMOS.

Threshold Voltage

Electronic Parts Engineering





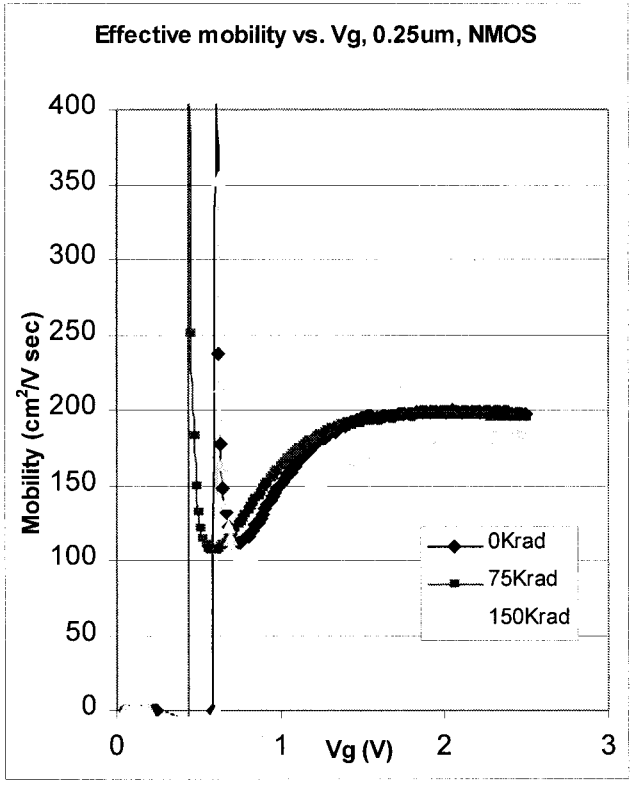
The threshold voltage for NMOS decreased from 0 to 75Krads due to gate oxide charge trapping. Above 75Krads, oxide charge trapping saturated and the effect of interface traps took over, causing a rebound behavior.

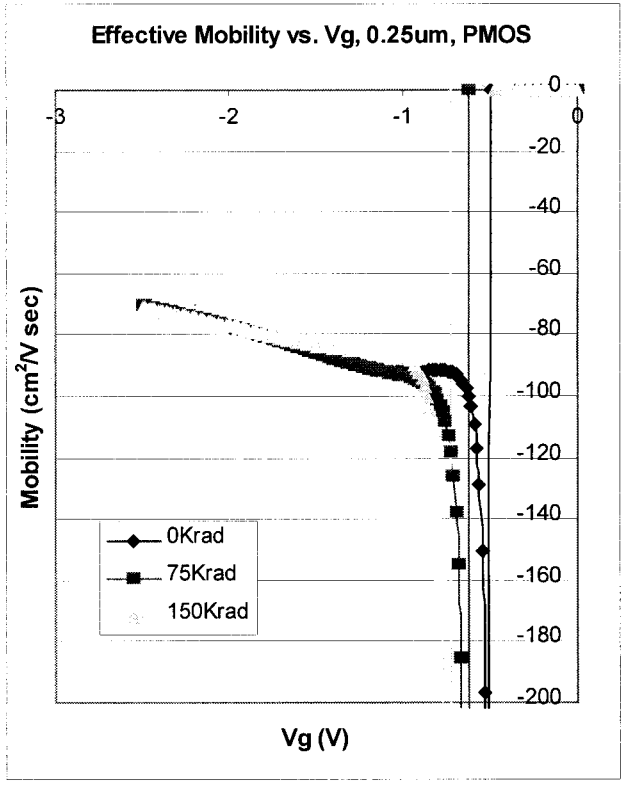
For PMOS, interface traps were positive, which had the same effect as oxide trapping. This was why the threshold voltage continued to decrease until transistor breakdown.

The drain current reflected these trends.

Effective Mobility

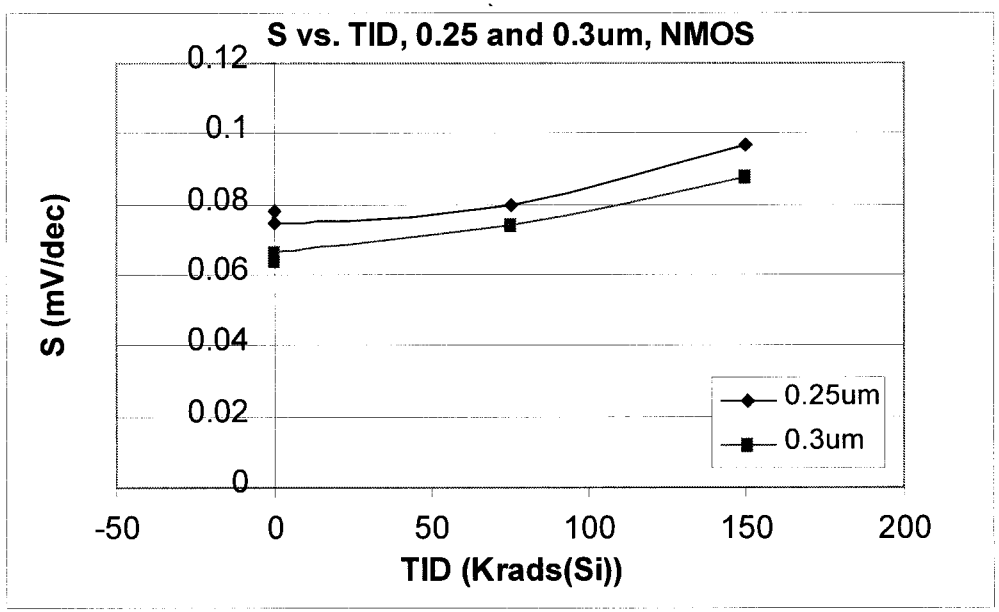
Electronic Parts Engineering





For NMOS, mobility was the lowest at 150Krads(Si), which was favorable for the drain current recovery. PMOS mobility was not observed to change.

Subthreshold Slope



The data showed the subthreshold slope slowly degrading with total dose.

In Summary

- SOI is an enabling technology for space applications due to its better performance in harsh environments, power savings, and its ability to integrate digital, analog, RF, and optical circuits all in one chip.
- FD-SOI has demonstrated good performance at low temperatures.
- FD-SOI transistors may be more sensitive to proton than X-ray irradiation.
- Further reliability studies and a larger sample size are needed to verify the radiation results. Combined effects of low temperature and radiation must be examined.

Acknowledgments

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