CSP Assembly Reliability and Effects of Underfill and Double-Sided Population

Reza Ghaffarian, Ph.D.
Jet Propulsion Laboratory, California Institute of Technology
Reza. Ghaffarian@JPL.NASA.Gov
Namsoo P. Kim, Ph.D.
Boeing Phantom Works

ABSTRACT

The JPL-led MicrotypeBGA Consortium of enterprises representing government agencies and private companies have jointed together to pool in-kind resources for developing the quality and reliability of chip scale packages (CSPs) for a variety of projects[1]. In the process of building the Consortium CSP test vehicles, many challenges were identified regarding various aspects of technology implementation. Last year, ball shear test results before and after isothermal aging were presented and compared to ball grid array packages[1].

These package were assembled on single- and double sided printed circuit board (PWB) without and with underfill. These test vehicles were subjected to various environmental tests including four thermal cycling conditions. These cycles represent the extreme harsh accelerated testing in the range of -55 to 125°C to a commercial requirement in the range of 0 to 100°C. This paper presents the thermal cycling test results to 2,000 cycles performed under different environmental conditions for single- and double-sided assemblies with and without underfill.

CSP IMPLEMENTATION CHALLENGES

Emerging CSPs are competing with bare die assemblies and are becoming the package of choice for size reduction applications. These packages provide the benefits of small size and performance of the bare die or flip chip, with the advantage of standard die packages.

Although the expression "CSP" is widely used in microelectronics industry by both suppliers and users, its definition evolved as the technology matured. At the start of the package's introduction into the market, a very precise definition was adopted by a group of industry experts as a package that is up to 1.2 or 1.5 times larger than the perimeter or the area of the die.

Soon, it became apparent that suppliers were using the term CSP to promote a miniature version of a previous package. A rapid transition to a much smaller size was difficult for both package suppliers and end users. Suppliers had difficulty building the packages whereas users had difficulties accommodating the need for the new microvia printed circuit board (PWB), mainly because of routing requirements and its increased cost. Other issues for accepting the "interim definition" by industry included lack of maturity in assembly and infrastructure. For example, the use of pitches other than 0.5 mm, including 0.75 and 0.65, was aimed at using a standard PWB design to avoid the increased cost of microvias.

The "expert definition" undermines a key purpose of chip scale packages, allowing for die shrinkage. If die shrinkage is acceptable for the package to retain the footprint, then a decrease in die size for the same CSP results in not conforming to the definition of a CSP. Therefore, in reality, CSPs are miniature new packages that industry is starting to implement, and there are many unresolved technical issues associated with their implementation.

Technical issues themselves also change as packages mature. For example, in early 1997, packages with a 1-mm pitch and lower were the dominant CSPs, whereas in early 1998 packages with 0.8-mm and lower became the norm for CSPs. New issues must be addressed including the use of flip-chip rather than wire-bond die in CSPs. Flip-chip solder joint failures within CSPs is a potential new failure mechanism that needs to be considered.

CSP RELIABILITY

CSPs have their own unique form factor not seen in SMT and many of them may not be able to meet the traditional reliability test requirements. There is a paradigm shift on reliability for CSP, and new specific tests such as bend and drop tests are being adopted to especially meet consumer requirements for portable electronic products. The shift is further motivated by several factors, including the following:

- Reduction in life expectancy for consumer electronics;
- Rapid changes in electronic technology

For surface mount, solder joints have both electrical and mechanical functions, and they have traditionally been the weakest link in assembly reliability. The most common damage to solder joints are those induced by thermal cycling. Creep and stress relaxation are the main causes of cycling damage

Reducing the CTE mismatch between the component and the PWB reduces cycling damage. For leaded SM package, the CTE mismatch between the solder joints

and the PWB was relieved by using compliant leads. Even though grid CSPs are robust in manufacturing, their rigidity is one of the main reliability concerns.

For the thermal cycling environment, several features of CSPs have helped its reliability. These include reduction in package size and therefore die size and package thicknesses. Both these will improve reliability, thereby partially reducing the inherent concern with CSPs. For high reliability applications, especially packages with high I/Os, such improvement might not be sufficient and other innovative technology developments will be required to decrease the local and global CTE mismatch.

Innovative approaches had been developed aimed at absorbing the CTE mismatch between the die and board within the package or externally through strain absorbing mechanisms, and therefore reducing stresses on the solder interconnects. These innovative approaches could introduce their own unique damage mechanisms since the weakest link may now have been transferred from solder to some other area of the attachment system.

One innovative approach uses compliant TAB leads and elastomeric materials between the die and substrate to reduce the package CTE mismatch. Since the TABs absorb the majority of the stresses, they become the weakest link and possible failure site. This approach has been widely shown to be effective for low I/O CSPs, but yet to be proven for higher I/O CSPs. The other innovative approach, which is called "Floating Pad Design", has potential for absorbing the global CTE mismatch, and therefore it could theoretically handle a large I/O package. Test results by the manufacturer are promising, but they are yet to be verified by others. It is not know if such solder ball floating would weaken the mechanical strength.

Factors that affect assembly reliability of CSPs were reviewed in a previous paper [3]. This paper presents cycle-to-failure data for CSP under four different thermal cycling conditions, with and without underfill, and single- vs double sided assemblies.

CSP TEST MATRIX

The Consortium agreed to concentrate on the following aspects of CSP technology and environmental testing after numerous workshops, meetings, and weekly teleconferences.

Package I/O /PWB (printed wiring board) — Eleven packages from 28 to 275 I/Os as listed in Table 1 were used. Figure 1 shows a schematic drawing of the PWB used (TV-1). The TSOP was used as control. The PWBs were fabricated from FR-4 and BT (bismaleimide triazine) materials which were available in the resin copper coated form and a high temperature FR-4. The boards were double sided, standard and microvia. Four types of surface finishes were considered:

- organic solder preservative (OSP);
- hot air solder level (HASL);
- immersion Au/Ni;
- Silver.

The majority were OSP finish.

Solder Paste/Volume — Three types of solder pastes were included:

- no-clean;
- water soluble (WS);
- rosin mildly activated (RMA).

Three stencil thicknesses were included:

- high (7 mil),
- standard (6 mil);
- low (4 mil).

Different stencil aperture design were used depending on the pad size. The standard stencil thickness used for the majority of test vehicles was 6 mil.

Package/Test Vehicle Feature — All packages were daisy-chained, and they had up to two internal chain patterns. Packages had different pitches, solder ball volumes and compositions, and daisy-chain patterns. In most cases, these patterns were irregular and much time and effort was required for the PWB design. This was especially cumbersome for packages with higher I/Os and many daisy-chain mazes were developed.

Packages with underfill requirements were included both with and without underfill to better understand the reliability consequence of not using underfill. The test vehicle (TV-1) was 4.5• by 4.5• and divided into four independent regions. For single-sided assembly, most packages can be cut for failure analysis without affecting the daisy chains of other packages.

Single-/Double-Sided Assembly — The PWBs (TV-1) were double-sided (microvia and standard); several boards with packages on both sides were assembled. This allowed a direct reliability comparison between the standard and microvia technologies, single- and double-sided processing issues, and single- versus double-sided solder joint reliability. In designing daisy-chains, it became apparent that the standard PWB technology could not be used for routing the majority of the packages.

Underfill — Several assemblies had underfilled packages even though it was known that the packages may not require underfilling. This was done in order to better understand the impact of underfill on solder joint reliability for different CSP styles. Package O required

underfill, and of these packages, the majority were underfilled. Several were not underfilled in order to better understand the reliability consequence of not using underfill for this package.

Table 1 CSP Package Configurations Matrix

Package ID	Package Style	Package Size (mm)	Pad Size (mm)	Pitch (mm)	I/O Count	Package. Thickness (mm)	Ball Dia (mm)
B	Leadless-1	7 x 13.6	0.35 x 0.7	0.8	28	0.8	-
C	TAB CSP-2	7.43 x 5.80	0.4	0.75	40	0.885	0.3
D	TSOP44	18.61 x 10.36	0.27 x 0.5	0.8	44	1.13	n/a
E	Leadless-2	7 x 12.3	0.30 x 0.75	0.5	46	0.8	n/a
F	TAB CSP-1	7.87 x 5.76	0.4	0.75	46	0.91	0.3
G	Chip on Flex-1 (COF-1)	0.3" x 0.3"	.010 in.	.020 in.	99	1.75	0.3
J	Wire Bond on Flex-1	12.1 x 12.1	0.375	0.8	144	1.4	0.5
K	Wire Bond on Flex-2	12 x 12	0.25	0.5	176	0.5	0.3
M	Chip on Flex-2 (COF-2)	0.5 x 0.5	.010 in.	.020 in.	206	1.75	0.3
N	Ceramic CSP	15 x 15	0.4	0.8	265	0.8	0.5
O	Wafer Level	0.413 x 0.413	.010 in.	.020 in.	275	-	0.3

* All measurements are in mm unless otherwise specified

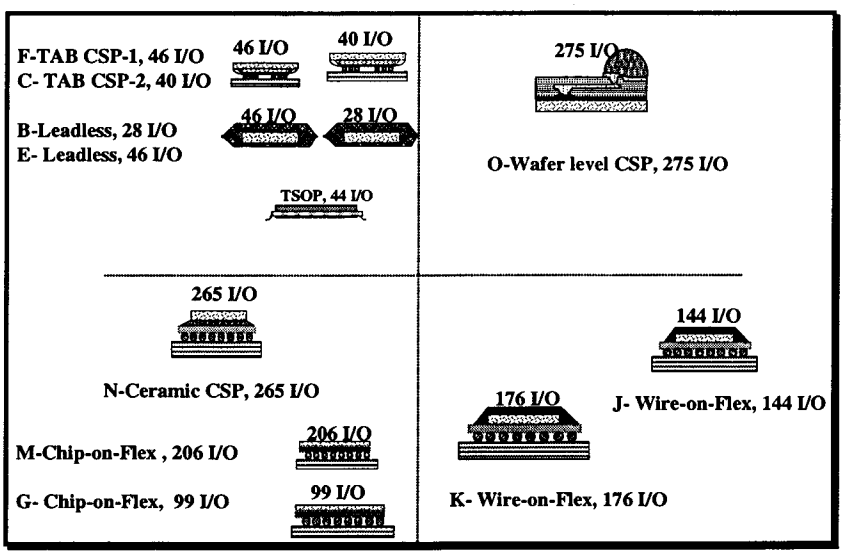

Figure 1 Schematic drawing of chip scale packages for the TV-1 test vehicle

Table 2 Thermal cycle conditions.

Cycle Type	Temperature Range (°C)	Heat up/Cool Down Rate (°C/min)	Dwell Time (minutes)	Duration Minutes (cycles per hour)
A	-30 to 100	2 to 5	10-20	82 (0.73)
B	-55 to 125	>10	10 to 20	68 (0.88)
C	-55 to 100	2 to 5	10 to 20	90 (0.66)
D	0 to 100	2 to 5	10 to 20	73 (0.82)
E	-55 to 125	2 to 5	10 to 20	159 (0.38

Accelerated Thermal Cycling- To provide a link to the JPL-led ball grid array Consortium testing[4,5], two conditions of –30° to 100°C (cycle A) and –55° to 125°C (Cycle B) were included. Two additional cycles were also investigated. Thermal cycling in the range of 0° to 100°C was performed to meet the needs of commercial team members. Hence, four different thermal-cycle profiles were used which are listed in Table 2.

Monitoring — The test vehicles were monitored continuously during the thermal cycles for electrical interruptions and opens. The criteria for an open solder joint specified in IPC-SM-785, Sect. 6.0, were used as guidelines to interpret electrical interruptions. Generally, once the first interruption was observed, there were many additional interruptions within 10% of the cycle life.

ENVIRONMENTAL TEST RESULTS

A large number of assemblies have already failed, and their cycles to failure have been documented. Out of these, cycles to failure data for three packages under four thermal cycling conditions are reviewed. Results for two chip-on-flex assemblies and leadless assemblies on single- and double-sided test vehicles are also presented. Results for other failed and survived assemblies are being gathered and analyzed and will be presented in the future.

Cycles to Failures Under Four Conditions

Figure 2 compares cycles to failure test results for the M package with 206 I/Os under four thermal cycling conditions. The trends are as expected, i.e., as the thermal cycling temperature ranges increase, the cycles to failure decrease. Note that assemblies failed between 3 to 34 cycles under a near thermal shock in the range of –55° to 125°C (B condition). Cycles to failure was 152 cycles under a typical commercial thermal cycling conditions in the ranges of 0° to 100°C. Results for –55° to 100°C and –30° to 100°C were between the two extreme cycling conditions as expected.

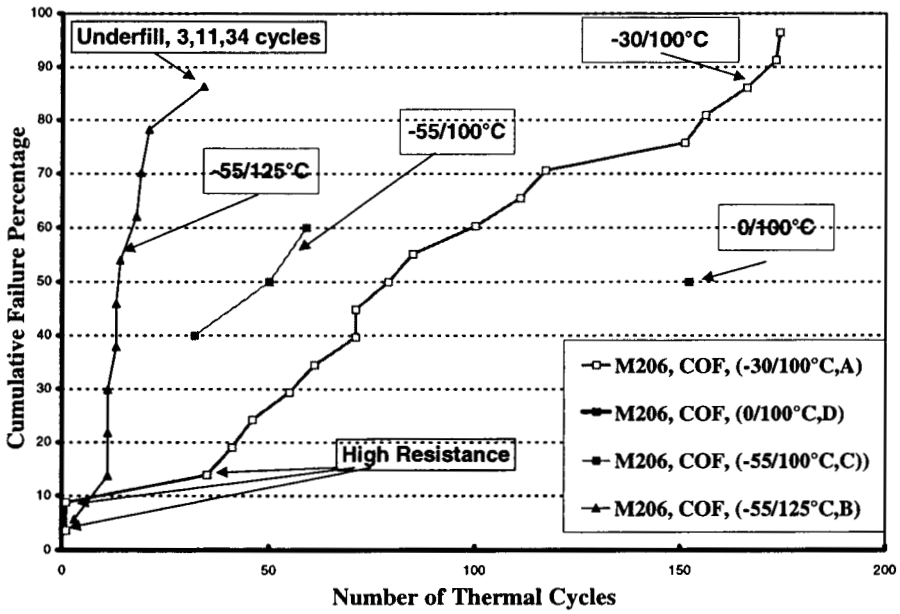

Figure 2 Cumulative Failure Distribution for Flex on Chip Assemblies with 206 I/Os Under Four Thermal Cycle Conditions

Cycles to Failure for Assemblies with Underfill

Cycles-to-failure test results for assemblies with underfill were analyzed and compared to standard assemblies without underfill. Three categories based on their impact on reliability were identified: (1) improvement by underfilling, (2) minimal effect, and (3) degradation due to underfilling. Cycles-to-failure data for representative packages are given below.

Improvement by underfilling

Cycles-to-failure data for package B, leadless, 28 I/O with no underfill under A (-30° to 100°C) and B (-55 to 125°C) thermal conditions are shown in Figure 3. As expected, cycles to failure increased as temperature cycling range decreased. Cycles to failure for B condition ranged from 372 to 546 with an $N_{50\%}$ of 441 (cycles to 50% of failure population). For A condition, it ranged from 641 to 1007 cycles with an $N_{50\%}$ of 763 cycles.

Results for 3 test vehicles with underfills are also shown in Figure 4. Underfilled assemblies showed only one failure at 1374 cycles under B condition to 1,500 cycles and no failure under A condition to 2,000 cycles. These limited test results clearly indicate significant improvement that can be achieved by underfilling for this category of peripheral leadless package.

Minimal impact by underfilling

Cycles to failure for package G, chip-on-flex, with 99 and package M with 206 I/Os with and without underfill under B condition are shown in Figure 4. Cycles to failure were higher for packages with lower I/O, but both assemblies showed extremely low cycles to failure (<100). Three datum points for assemblies with underfill are also plotted. These limited data indicate that improvement due to underfilling for this package with two I/Os is almost insignificant.

Degradation by underfilling

Cycles-to-failure data for package F, TAB CSP-1, with 46 I/Os under A and B thermal cycle conditions are summarized in Table 3. Under both conditions, assemblies with underfill showed much lower cycles to failure than those with no underfill. Assemblies showed no failure to 2,000 under A condition, whereas the three underfill version failed at 996, 1385, and 1727 cycles. Note that this package decouples the die CTE mismatch by use of a stress dampening elastomeric materials layer and flexible TAB lead interconnects.

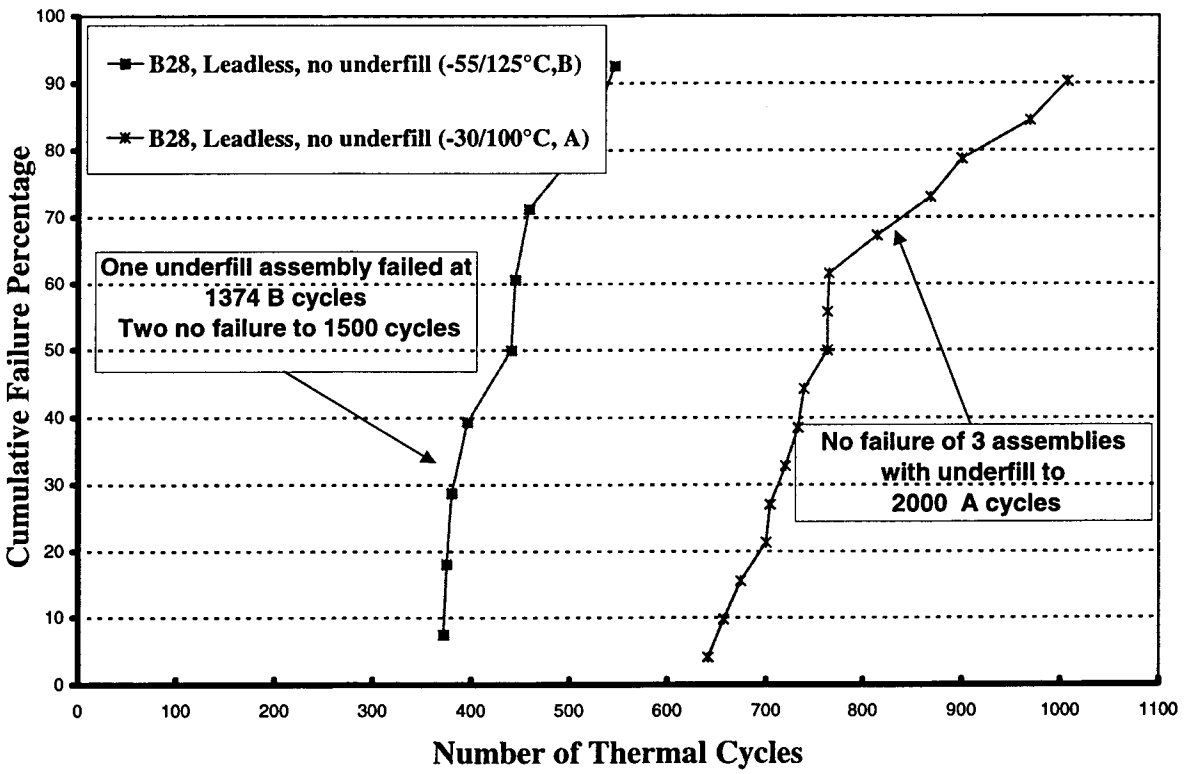

Figure 3 Cycles-to-failure for a 28 I/O leadless package without and with underfill

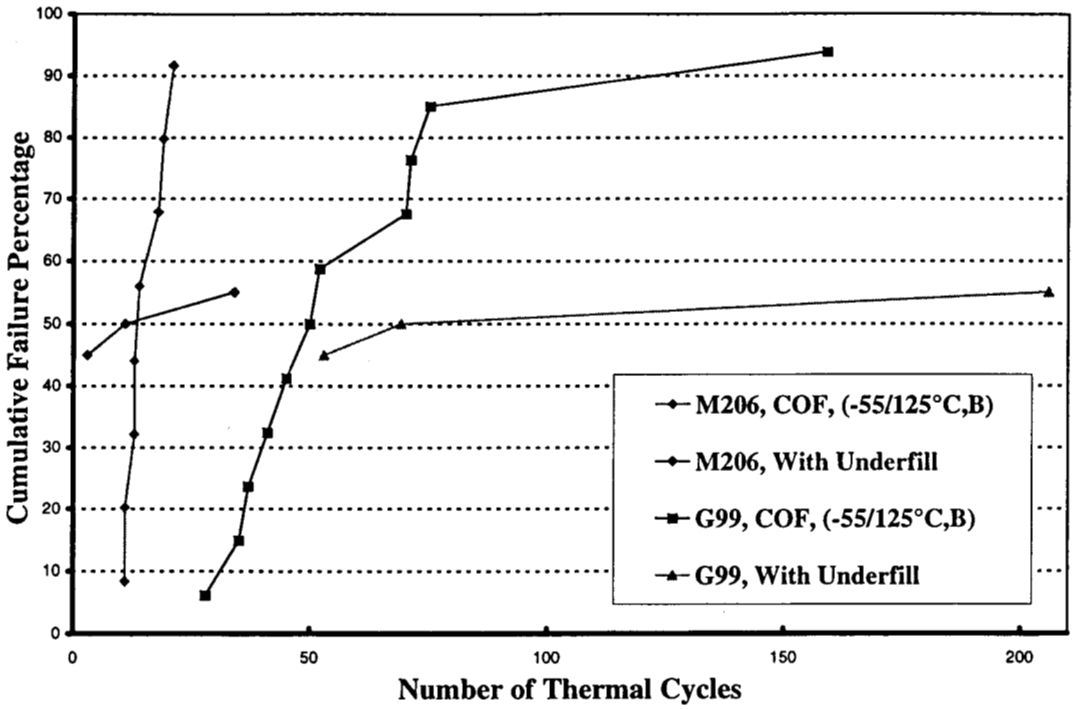

Figure 4 Cycles-to-failure for chip-on-flex assemblies with and without underfill

Table 3 Assemblies with and without underfill comparison

Package & thermal cycle condition	No Underfill Number and cycles to failure	With Underfill Number and cycles to failure
Package F, TAB CSP, -55°C to 125°C, B, 1,500 Cycles	3 out of 10 failure at 709, 896, and 1,380 cycles	3 out of 3 failures at 32 (?), 142, 710 cycles
Package F, TAB CSP-1, -30°C to 100°C, A, 2,000 cycles	No failure (15 assemblies)	3 out of 3 failure at 996, 1385, and 1727 cycles

Single vs. mirror-imaged double-sided assembly

Single-sided assemblies were observed to fail at much higher cycles-to-failure (i.e. more fatigue resistance) than double-sided assemblies. The N50 (cycles to 50% failure of the population) were 437 for double- and 763 for single-sided assemblies under test condition A (-30/100 °C). Double-sided assemblies also failed at a much faster rate for a more sever thermal cycle condition in the range –55 to 125°C.

Discussions

Double-sided assemblies are attractive from the view point of density and electrical improvement. However, there are processing and reliability concerns when double-sided boards are assembled. Significant reliability decreases for double-sided assemblies are of great concern, especially since most CSPs lack the needed reliability when compared to leaded packages. Another minor concern is potential part fall from the assembled side during second reflow. The CSP's small ball size plus low solder paste volume might not generate enough molten surface tension force to hold the package weight during reflow. This problem can be easily resolved, for example, by the use of an adhesive to strengthen the package attachment, even though it adds materials cost, additional process steps, and possible contamination

In looking for determine the cause of the early failures of double-sided B28 leadless assemblies, it was noticed that this package exactly overlapped another leadless package on the second side with a 90° rotation. During visual examination, it was noted that the first failure location was at two cross-over corners as shown in Figure 7. These test results, showing early joint failures for double-sided assemblies, are qualitatively in agreement with a few assembly reliability test results reported in literature [6].

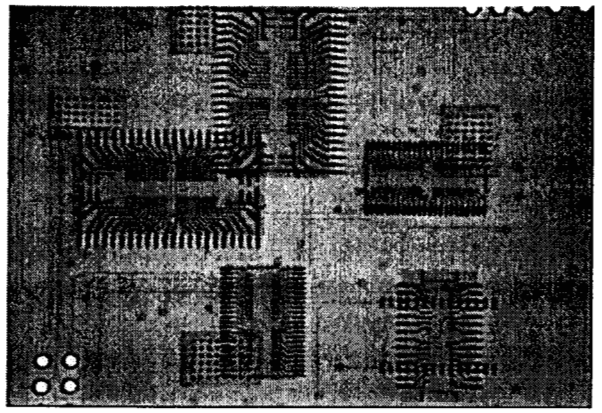

Figure 7 X-ray photos of double-sided test vehicle with package overlap

To better define the causes of early failure in double-sided assemblies, their differences with single-sided assemblies need to be examined further. Three main differences are:

- Localized stiffness change due to the second package
- Increase in solder joint height due to package weight during second reflow
- Thermal disturbance- Stress induced disturbance from one package to the other and metallurgy of paste and solder.

It is postulated that when solder joints are directly disturbed, they are affected by double sided assembly. Since there were no direct disturbances for the QFP/CSP cases, improvement was observed. A possible reason for an increase in cycles to failure might be due to solder joint elongation because of CSP weight during second reflow. As solder joint height increases, the shear strain due to CTE mismatch decreases, hence improvement in joint reliability.

Combination of solder joint disturbance and increase in stiffness are the main reasons for a decrease in solder joint reliability for double-sided-assembly. An increase in local stiffness, especially for thinner PWB, might have a more pronounced effect on its curvature during second reflow and hence cause a disturbance on solder joint. Thermal disturbance might also occur due to metallurgical differences between melting and solidification of solder paste and solder with different compositional phases. A more detailed study is needed to identify significance of each parameter.

Underfill Effects on Reliability

Underfill has been widely used to improve by at least an order of magnitude solder joint reliability of area array flip chip die attachments both for use in internal packages and on the PWB. Underfill absorbs the CTE mismatch and therefore reduces stress significantly by distributing stress uniformly through the solder joints. Underfilling, however, is undesirable because of the additional process requirements of cost increase and the reduction in manufacturing throughputs. Another drawback of underfill is the inability to rework defective parts. Progress has been made to reduce the negative impact of underfilling by shortening the process time by the use of snap cure polymers and enabling reworkability by the development of reworkable underfills.

For CSPs, it was shown that the effect of underfilling on reliability depends on package structure. The package structure for three categories were:

- Underfill improved leadless CSP reliability
- Underfill had a minimal impact on flex-on-chip reliability
- Underfill degraded a CTE absorbed TAB CSP

The leadless package has a resin body containing die with protruded peripheral groves for solder joint attachment. Underfill will bond the molded body to PWB without coverage of periphery solder joints. A good bonding between underfill and the package resin is expected, thus reducing CTE mismatch stress on solder joint and improvement in cycles-to-failure.

The chip-on-flex, an area array package, uses a polyimide flex bonded to dice as I/O redistribution. Bonding between flex and underfill will reduce stress on solder joints, however, it may increase CTE mismatch between die and flex and underfill composite. Failure mode change from solder joint failure to flex bond separation may possible reason for a lack of improvement on cycles-to-failure for the assembly with underfill.

The TAB CSP, uses a flexible polyimide substrate and leaded TAB leads for I/O redistribution. The flexible interposer with addition of underfill will significantly relieve CTE mismatch on solder joint. However, addition of underfill with CTE close to elastomeric interposer may increase stress on package internal TAB leads and therefore lower cycles-to-failure.

Failure analyses are being performed to determine failure modes of assemblies with underfill in order to confirm the failure mechanisms discussed for different CSPs.

CONCLUSIONS

- Cycles to failure for the same assembly under four different environments were different, but the trends were as expected, i.e., as temperature cycling ranges increased, cycles to failure decreased.
- The solder joints, disturbed by a second reflow due to back-to-back double sided assembly, showed early failure. The reduction to failure percent for the leadless package.
- Underfill effects on cycles to failure may be positive, neutral, or negative depending on package types. It

improved the reliability of leadless package, was neutral for chip-on-flex, and had negative effects on the TAB CSP reliability.

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ACKNOWLEDGMENTS

The majority of research described in this publication is being carried out by the Jet Propulsion Laboratory, California Institute of Technology, under a contract with the National Aeronautics and Space Administration.

I would like to acknowledge the in-kind contributions and cooperative efforts of the JPL CSP consortia. Special thanks to J.K. Bonner, S. Barr, J. Okuno, A. Arreola, JPL; E. Siméus, S. Stegura, R. Smedley, Raytheon; M. Chisa; Boeing; A. Chen, I. Sterian; Celestica; K. Selk, B. Bjorndahl, TRW; R. Chanchani, Sandia; and other team members who have made contributions to the progress of this program.