Overview of Non-Volatile Testing and Screening Methods

Farokh Irom

Jet Propulsion Laboratory
California Institute of technology
Pasadena, CA 91109

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Abstract

Testing methods for memories, and non-volatile memories are have become increasingly sophisticated as they become denser and more complex. High frequency and faster re-write times as well as smaller feature sizes have led to many testing challenges. This paper outlines several testing issues posed by novel memories and approaches to testing for radiation and reliability effects. We discuss methods for measurements of Total Ionizing Dose (TID).

I. INTRODUCTION

Complementary metal-oxide-semiconductor (CMOS) memories can be divided into two main categories: random access memories (RAM's), which are volatile, i.e., they lose stored information once the power supply is switched off, and read-only memories (ROM's), which are non-volatile, i.e., they keep stored information when the power supply is switched off. Flash memories combine those two features. There are different ways to design flash memory cells, and they have different characteristics, depending on the cell design. In flash memories a single cell can be electrically programmed and a large number of cells called block are electrically erasable at the same time. Flash memories provide a high-density storage technology for applications that do not require frequent write/erase operations. The basic structure of a flash-memory cell uses a dual sandwiched gate structure, interposing a floating gate between the body of the device and the control gate. Its structure is similar to EEPROM, but uses a much thinner oxide between the floating gate and channel region. The thin oxide allows charges to be transferred to and from the floating gate by either Fowler-Nordheim (F-N) tunneling from the source or body, or hot-electron injection from the channel region for erasing and writing. Most manufacturers use F-N tunneling for erasure, but different write mechanisms [1].

Two basic approaches have been used to develop high-density flash memories. The NAND structure is shown in Figure 1. The NAND cell is more compact because it does not provide contacts to individual source and drain regions. However, the read and write time is inherently slower in this technology because cells cannot be accessed individually; the read path goes through other cells in the stack. In order to deal with this, the device architecture divides the memory into pages. A page buffer is used to improve read time.
The NAND structure uses Fowler-Nordheim tunneling for erasing and writing. The oxide between the floating gate and body is about 250 A. This requires higher voltages – typically 20 Volts for erasing and writing.

The NOR structure is shown in Figure 2. In this technology, random access of individual cells is allowed. This approach minimizes access time compared to the NAND structure. The erase function is done at the block level by applying a high voltage (Vpp) to the source, grounding the control gate and allowing the drain to float. Charge in the floating gate is transferred to the source by Fowler-Nordheim tunneling. Programming is done by grounding the source, and applying (V_{pp}) to the control gate [2,3]. The oxide between the floating gate and channel is around 100 A, to enhance the tunneling effect. Cells in the NOR structure require about 12 Volts for erasing and writing which is lower than the 20 Volts of the NAND structure. Some flash memories produced by Intel can operate at

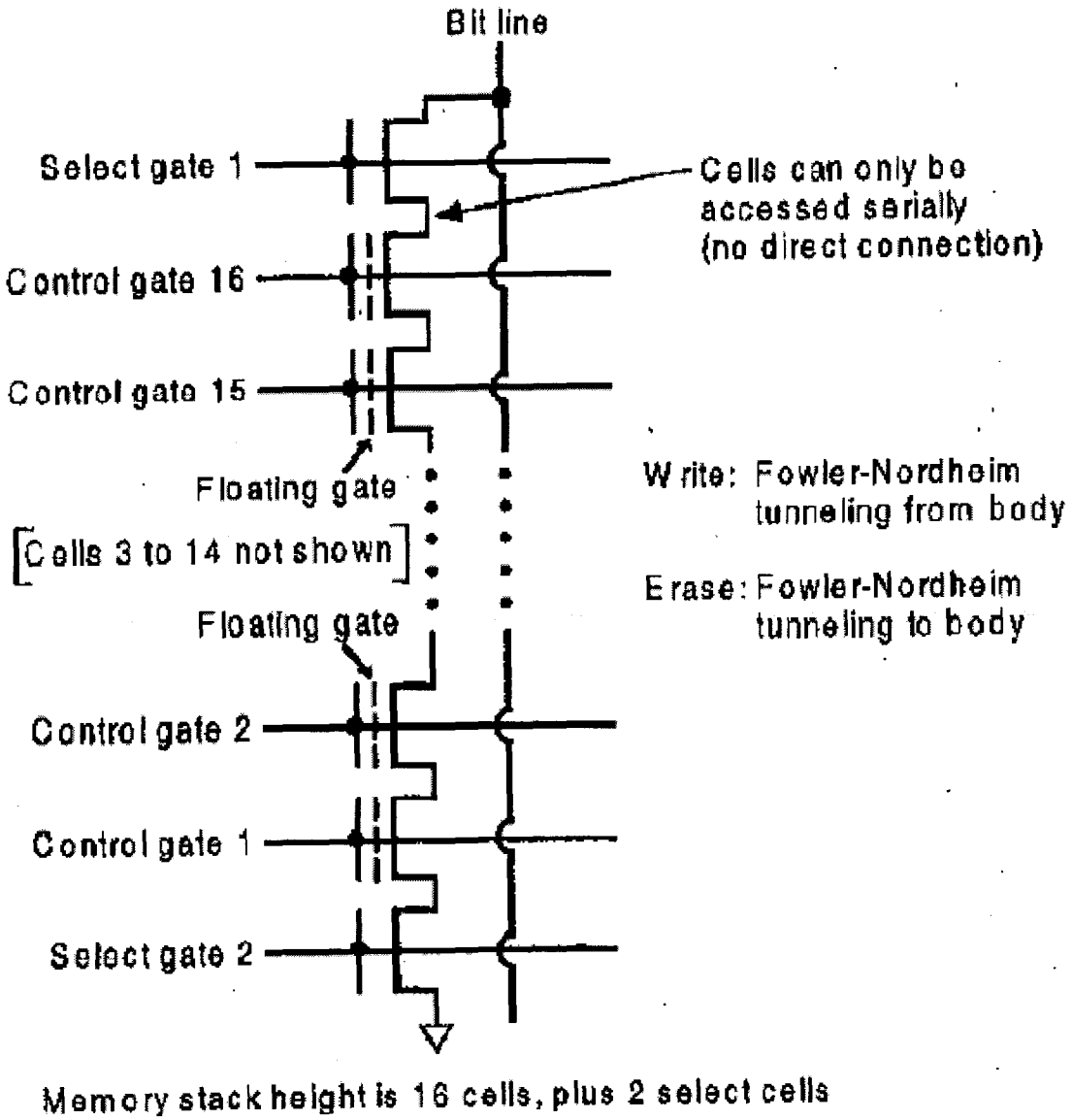

Fig. 1. Cell architecture of a NAND flash memory organized in 16-bit stacks

either 3.3 or 5 Volts. A boosted word-line voltage is required with the lower power supply voltage; internal circuitry detects the voltage and automatically applies the boost voltage [4].

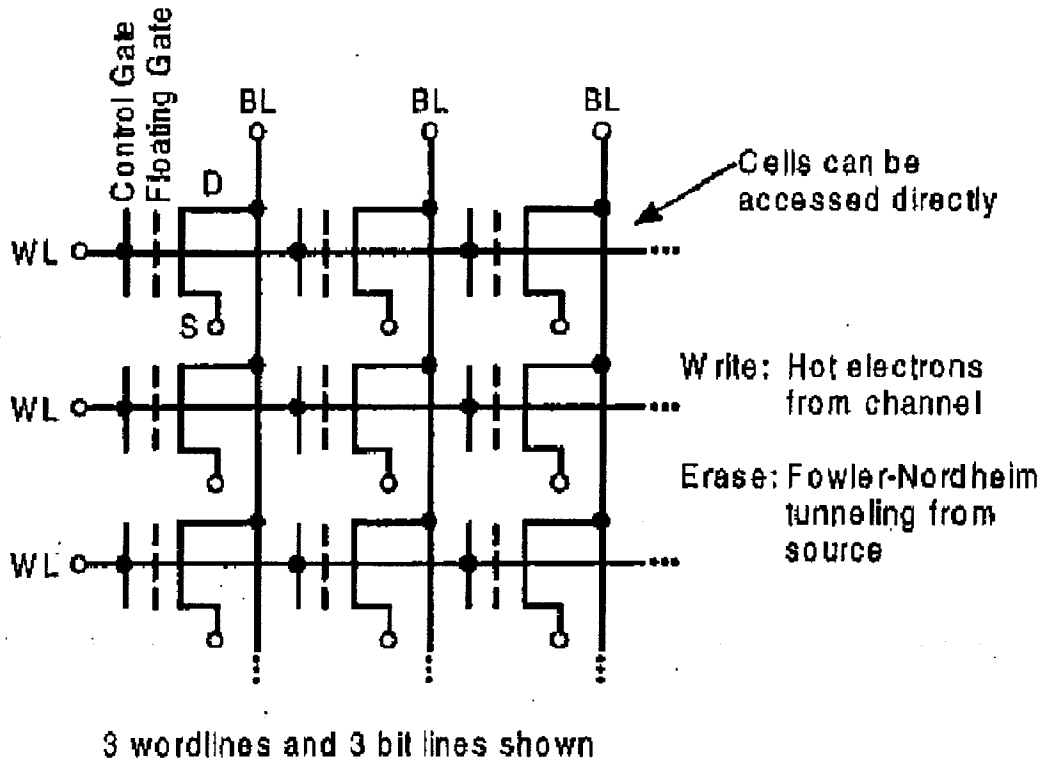

Fig. 2 Cell architecture of a NOR flash memory

The overall architecture of either type of flash memory is very complex. Reading can be done relatively rapidly for either cell architecture using conventional circuitry for access and readout. However, erasing and writing are very slow operations (on the order of milliseconds) compared to conventional memories. To overcome this limitation, flash memories are subdivided into blocks, allowing erasing and writing to be done at the block level. Internal registers and buffers provide temporary storage for pages of data, allowing more transparent interface. A write state machine and a command state machine are used to control the complex sequences of operations that are needed. A charge-pump circuit is also required in order to provide the high internal voltages that are needed for erase and write operations. Because of this complexity, flash memories cannot be treated as simple memories. It is quite challenging to determine how they respond in radiation environments.

II. TOTAL DOSE TESTING

Flash memories can be used in five basic ways [2]: (1) unpowered mode, which only applies power during the relatively short duration that the memory contents are used; (2) a continually powered standby mode, in which the device is ready to begin reading, but the address lines are static; (3) a read-only mode, which applies continuous power to the device, along with address, clock and control sequences for reading, but never applies power to the write circuitry; (4) a read-mostly mode, or powered static mode, which is similar to the previous mode, but applies voltage to the charge pump and may also include brief periods for active writing; and (5) a mixed read and write mode, which involves many write cycles so that write duty cycle is a significant fraction of the total use period. These modes are briefly summarized in Table 1 below.

Description	Bias Condition	Sensitive to charge Pump	Sensitive to Wear Out
Read Only	OFF	NO	NO
Read Only	ON	NO	NO
Read Mostly	OFF	SLIGHT	SLIGHT
Read Mostly	ON	YES	SLIGHT
Intensive Read/Write	ON	YES	HIGH

Table 1. Possible Operating Modes for Flash Memories

In evaluating flash memories for use in space, it is important to recognize how they will be used. Read mostly applications such as code storage are natural fits because of the very slow write and erase time. In these applications they might not be powered except for brief periods when it is necessary to read their contents. Mode 5 is may be used in some applications (such as data storage during planetary flybys), but usually involve relatively short time durations. We consider two bias conditions that are likely to be encountered during the majority of the time that flash memories are used in space: (1) unbiased (Mode 1); and (2) static biased, where the device is powered, but no address cycling or data access operations are used (Mode 2).

Total dose studies of earlier devices implicated the charge pump circuitry as responsible for device failures in both technologies [5]. This was clearly demonstrated for the 16 Mb Intel NOR device where the erase/programming voltage could be externally supplied; much higher dose levels were achieved when the internal charge pump was not used. Less direct methods were used to show that the charge pump is also the weakest link for the 16Mb Samsung NAND device, based on higher required voltages for erasing and programming after irradiation.

D. Nguyen et al.[3] performed total dose measurements using JPL cobalt-60 test facility at either of two dose rate: 25 rad(Si)/s and 0.012 rad(Si)/s using a series of stepped

irradiations.They used a non-repeating pattern generated by a linear congruential pseudo-random generator with a slight modification: discarding every 31st number. The algorithm produces a reproducible random sequence of states, starting with a "seed" number. Two seeds were used, 31 and 59, which are both prime numbers. When the second seed is used, the pattern developed by the algorithm produces the opposite state in ½ the bits used with the first seed. This tests the ability to program the opposite state in ½ of the bit locations after each irradiation. These complex patterns are the basis of a more comprehensive functionality check which is capable of detecting address or detecting errors, unlike simple patterns. Before the first irradiation, the devices were written with a random pattern (seed-31). The pattern was verified by reading the contents of flash devices before and after each irradiation level for all parts that were evaluated in the "read" mode. For full functional mode; the devices were erased and a new random pattern (seed-59) was written to the memory after the first level. After the second level the original pattern (seed 31) was used, interchanging each pattern after each irradiation step in order to verify that a different pattern could be written into each storage location.

In their studies, some post-irradiation measurements were limited to the "read" mode, making no attempt to verify operation of either erase or write function of the memory. This condition was selected because many applications require very infrequent writing. Other devices were tested more completely after each irradiation level, subjecting each device to a complete erase-write-read cycle (Mode 5). This tests the full functional capability of the memory, and requires that the charge pump and verification circuitry function correctly.

Figure 3 shows test results or their studies for the 32-Mb Intel multi-level flash memory for statically biased and unbiased conditions. With bias applied, the device would no longer function after the second irradiation level [12 krad(Si)]. When tested without bias, the device continued to operate close to 16 krad(Si). Thus, the first versions of the multi-level flash technology failed at lower level than the earlier generation devices (16 Mb at about 25 krad(Si) in erase-write-read mode).

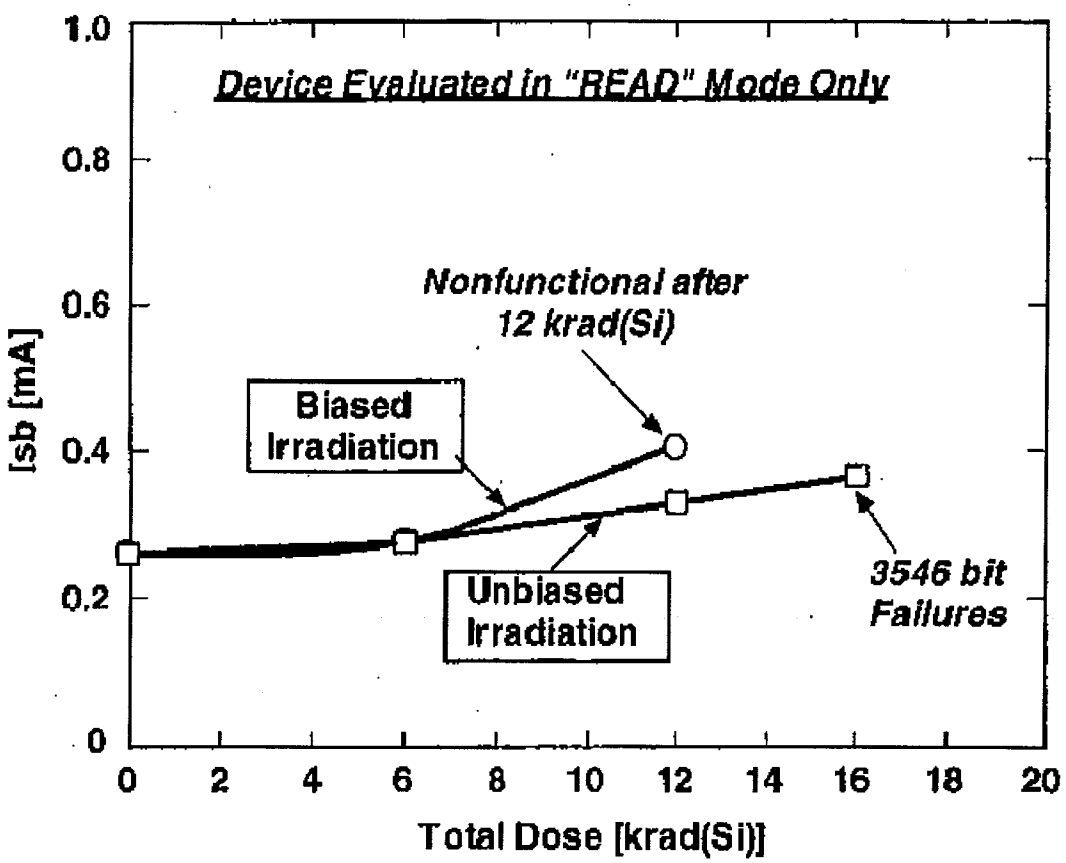

Figure 3. Total dose results for the Intel 32Mb flash memory evaluated in read mode

The 64-Mb multi-level flash memory behaves somewhat differently. The standby current increased much more rapidly with increasing radiation levels when bias was applied compared to results for the 32 Mb devices in Figure 4. The 64 Mb devices typically operated to levels well above 20 krad(Si). These results are shown in Figure 5. When tested without bias, the 64Mb devices passed read functionality up to 50 krad(Si) and showed only slight increases in standby current. However, at 75 krad(Si) a large number of addressing errors occurred. These were severe enough to make the device unusable at that level.

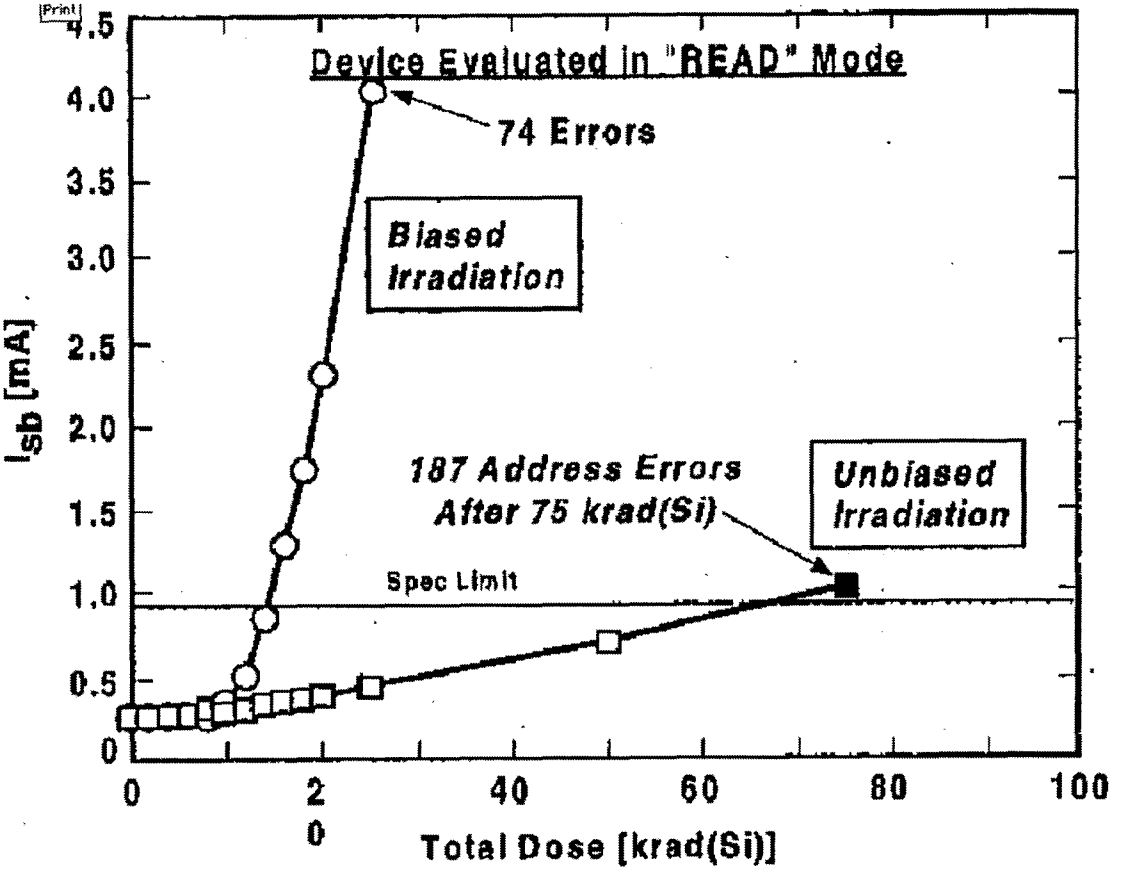

Figure 4. Total dose results for the Intel 64Mb flash devices evaluated in read mode

Results for the 64Mb Intel device in the fully operational mode (Mode 5) are shown in Figure 5. When irradiations were carried out under bias, the device became fully nonfunctional at 11 krad(Si), in contrast to the tests in "read" Mode3 where the device continued to operate with only a few errors to levels almost twice as great. Without bias, the device also failed at much lower levels when fully operational tests were done between irradiations.

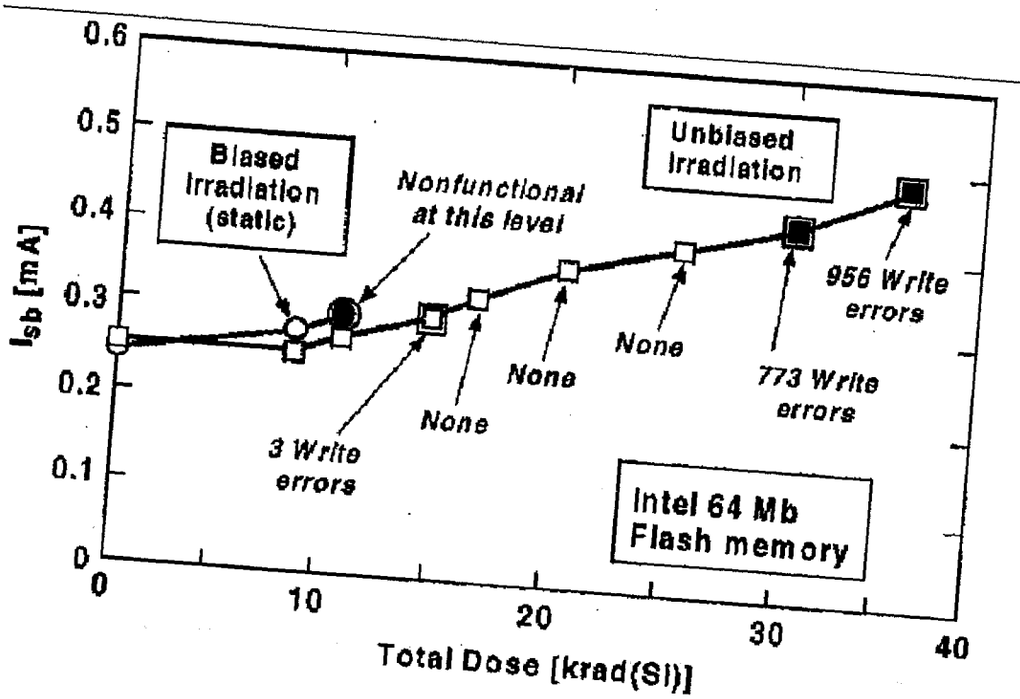

Figure 5. Total dose test results for the Intel 64Mb flash memory evaluated in full functional mode

Test results for 128 Mb Samsung devices in the "read" mode are shown in Figure 6. Without biased irradiation, the standby current increased by several order of magnitude at about 20 krad(Si). When tested without bias the device functioned to levels above 100 krad(Si) with only a small number of "read" errors.

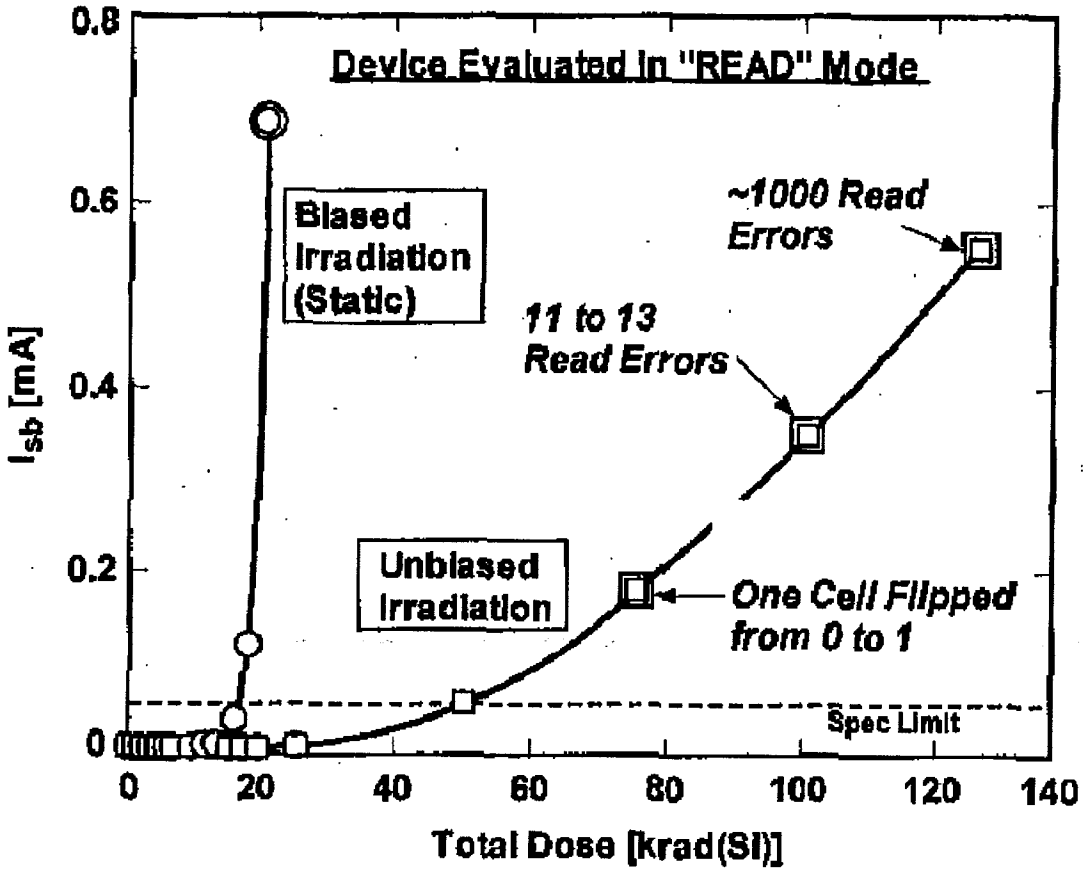

Figure 6. Total dose results for the 128Mb Samsung flash device, tested in read mode

In studies with full functionality tests erase-mode (Mode 5) failures were observed at around 8 krad(Si) under bias irradiation as shown in Figure 7. When fully functional tests were done on devices that were unbiased during irradiation, erase failures occurred at 45 krad(Si).

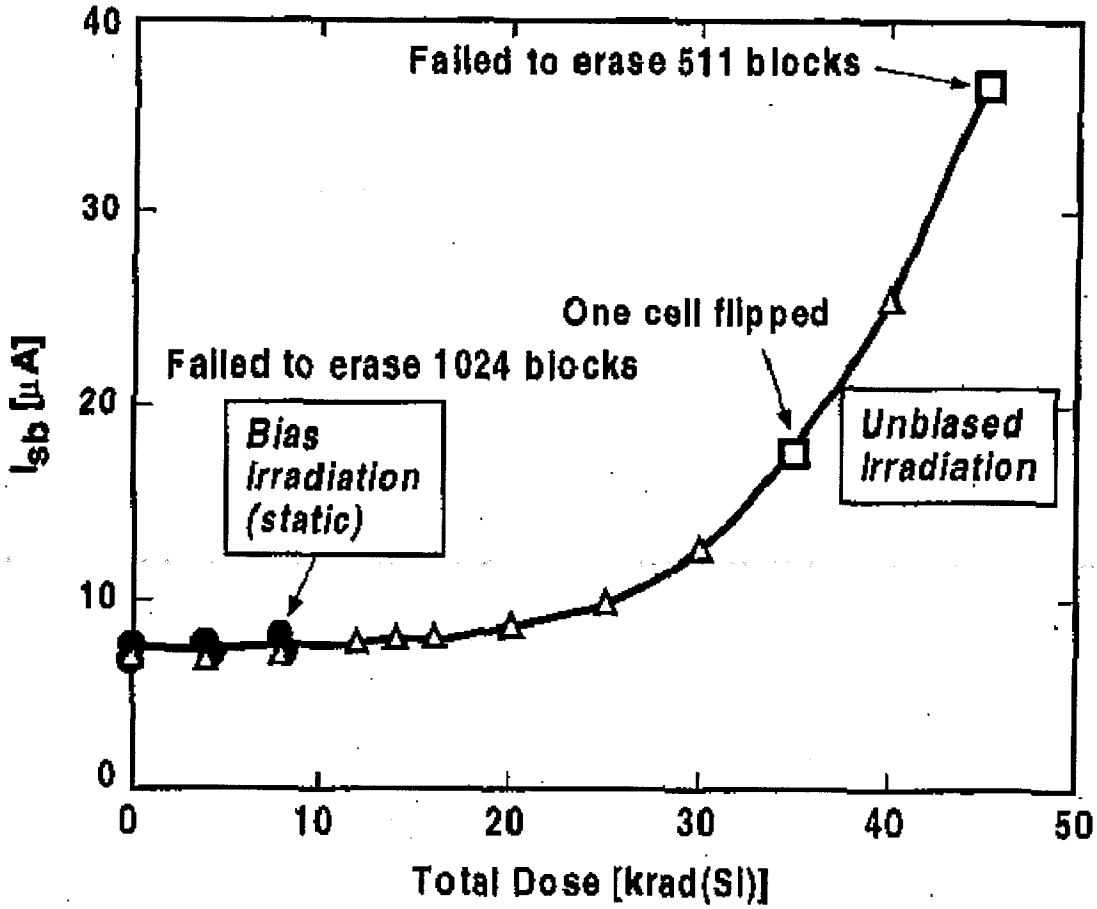

Figure 7. Total dose test results for the 128 Mb Samsung flash memory evaluated in Erase/Write/Read mode (Mode 5).

III. CONCLUSION

Designing systems to effectively use flash memory while avoiding radiation problems, including destructive effects, is becoming more difficult as the devices are scaled to smaller feature sizes and larger overall arrays size. Charge pump degradation continues to be the most significant degradation mode, even for more advanced flash memories. Microdose effects, although they affecting only a small number of bits, may be on the verge of becoming a serious problem as transistor sizes scale and manufactures push toward the next step in multi-level flash memory designs.

REFERENCES

[1] P. Pavan, R. Bez, P. Olivo, and E. Zanoni, "Flash Memory Cells—An Overview," Proceeding of the IEEE, vol. 85, p. 1248, (1997).

[2] H. R. Schwartz, D. K. Nichols and A. H. Johnston, "Single-Event Upset in Flash Memotries," IEEE Trans. Nucl. Sci., vol. 44, p. 2315 (1977).

[3] D. N. Nguyen, S. M. Guertin, G. M. Swift and A. H. Johnston, "Radiation Effects on Advanced Flash Memories," IEEE Trans. Nucl. Sci., vol.46, p. 1744 (1999).

[4] A. Baker, R. Alexis, S. Bell, V. Dalvi, R. Durante, E. Bauer, M. Fandrich, O. Jungroth, J. Kreifels, M. Lansgraf, K. Lee, H. Pon, M. Rashid, R. Rozman, J. Tsang, K. underwood and C. Yarigadda," A 3.3 V 16 Mb Flash Memory with Advanced Write Operation," Digest of Papers from the 1994 international Solid-state ircuits Conference, pp. 146-147.

[5] D. N. Nguyen, C. I. Lee and A. H. Johnston,"Total Ionizing Dose Effects on Flash Memories," 1998 IEEE Radiation Effects Data Workshop Record, P. 100.