spoke w/ author not novel or new method

Fabrication of Novel Si_3N_4 Micromesh Spider Web Bolometer Using Deep Trench Etching on SOI Wafer.

Minhee Yun, Anthony D. Turner, James J. Bock, and Judith A. Podosek
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I. Introduction

Bolometers are used for sensitive detection of radiation throughout the electromagnetic spectrum, from X-ray to millimeter-wave. Sub-millimeter wave bolometers have achieved a steady increase in sensitivity over the past decade. Traditional bolometers such as thermistors use semiconducting beads with an electrical resistance that decreases with temperature [2]. These bolometers are made from oxides of nickel, manganese, and cobalt and are used extensively to measure microwave radiation. Other bolometers, pyroelectric bolometers [3], are capacitors made by coating two surfaces with a thin film of ferroelectric material. The polarization of the ferroelectric material varies with temperature, changing the capacitance and causing a small voltage or current flow in the capacitor. The micromesh spider web bolometer is very attractive for sub-millimeter because of its size, weight, sensitivity and stability advantages, and has been re-searched widely by our group [1,13,14] . This spide web architecture as shown Fig. 1. provides (i) a low base thermal conductivity and thus a low NEP (noise equivalent power), (ii) a low intrinsic heat capacity, (iii) low cosmic ray cross section area, and (v) high sensitivity. The sensitivity of a bolometer can also be improved by reducing its base temperature, and reducing its thermal conductivity. However, it is very difficult to obtain a low thermal conductivity and heat capacity using traditional semiconductor fabrication processes. In recent years, bolometer technology has progressed rapidly with advances in microfabrication enabling large format arrays of bolometers.

In this study, we have fabricated and developed extremely sensitive Si_3N_4 a bulk micromachined-micromesh spider web bolometer for sub-millimeter astrophysics using microelectromechanical system (MEMS) techniques. The use of MEMS techniques in this research has improved the sensitivity and format of bolometer arrays.

A brief summary of etching technologies is helpful in understanding the advantages of fabrication of the spider web architecture using MEMS. Etching technologies in thin film processes play an important role in the semiconductor industry. Etching technologies for fabrication of ultra large scale integrated (ULSI) devices should have strong anisotropy, uniform etching, and high selectivity. In MEMS devices, a bulk or surface anisotropic etching of silicon is highly required to fabricate micro-transducer structures. These goals can be successfully achieved by applying suitable etching techniques in wet or dry etching.

Wet etching techniques are used extensively in semiconductor processing because of their low cost, high throughput, and excellent selectivity. Important progress in the fabrication of micro-electrical structures with integrated circuits using wet etching has been achieved by many researchers. Anisotropic etchants etch different crystal planes in silicon at different rates. The most common ansiotropic etchant is potassium hydroxide (KOH) because it is safer to use compared to EDP (ethylenediamine, pyrocatechol, and water) solution which is anothor anisotropic etchant for silicon [4]. Fabrication of UMOS transistors on Si (111) wafers for high power and high current density applications has been achieved by applying KOH anisotropic wet-etching [5]. Other applications of KOH wet-etching include the fabrication of VMOSFETs, radio frequency amplifiers, power supplies, microcomputers [6], and field emission devices [7]. From previous research [8], the analysis of statistically designed experiments of KOH etching has been demonstrated both analytically and graphically, that in order of significance, the factors affecting etching are reaction temperature, KOH concentration, and interaction between them. HND (HF-HNO_3-DI water) etching technology [9] is also a very common wet process widely used for removing the damaged layer materials and cleaning surface of the materials. In addition to that, silicon wafers are typically wet etched in mixtures of nitiric acid and hydrofluoric acid.

In dry etching, glow discharge in gases is used to etch metals, dielectrics, and semiconductors, whereas in wet etching liquids are used to etch these materials. Dry etching is a key part of integrated circuit manufacturing. The importance of the dry etching technologies lies in the ability for fine line definition, highly directional etching, and good selectivity [10]. These etching technologies can be classified as physical or chemical etching. Physical etching uses the impact of incoming ions created in a plasma to sputter material off the surface to be etched. It is a highly directional etching technique. Chemical etching is a non-directional and highly selective etching technique [11]. The most common dry etching technique is reactive ion etching (RIE). With RIE, ions are accelerated toward the material to be etched and the etching reaction occurs in the direction of ion travel. Deep trench RIE is an unique technique and extensively used in semiconductor field. Deep trench etching has many advantages compare to wet etching such as etch uniformity and etch profile. The difficulties in performing a successful deep trench etch process have been compounded by the range of the requirements for various MEMS applications : etch depth from 20μm to over 300μm; aspect ration of greater than 30; with silicon exposed area of below 5% to over 80% [12].

In this research, we used deep trench RIE to fabricate the micromesh spider web bolometer and focused our work on increasing the yield of web production. And our results indicate that use of deep trench RIE increased the yield of micromesh web architectures on the wafer. A novel method of manufacturing bulk micromachined components in SOI material with deep trench RIE is also presented. We observed that the deep trench etching may result in less surface roughness and higher conductivity in the silicon nitride supports. We also present the design and performance of a small bolometer array intended to demonstrate technology readiness for future space-borne such as Herschel and Planck [13], and balloon-borne applications such as BOOMERanG [14] and MAXIMA [15]. These spider web bolometer arrays allow astronomers to develop infrared images of astronomical objects. This technology will provide significantly sharper images than were available in the past. These arrays also have potential applications in instruments for industrial process control and spectroscopy instruments.

II. Bolometer Fabrication

The process sequence of the fabrication of SOI micromesh spider web bolometer is shown in Fig. 2. These processes, including cleaning, dry etching, LPCVD (low pressure chemical vapor deposition), lithography, and metallization, are standard semiconductor fabrication techniques. The processes for the fabrication of the spider web bolometer device have been developed at the MDL (Microdevice Laboratory) at Jet Propulsion Laboratory. The wafers used in this research were thermally bonded SOI wafers with (100) orientation. The thicknesses of the top Si, buried SiO_2, and bottom Si layer were 2 μm, 1 μm, and 350 μm, respectively, with ±10% variation. One of advantages of using SOI material is that reduces the total chip size compared to standard bulk micromachining because of buried oxide. It also adds functionality to the components, such as inherent overload protection and squeezed air-film damping.

First, the SOI wafers were prepared with standard RCA cleaning. Then, 1 μm layer of Si_3N_4 [Fig. 2(a)], which acts as support legs, was deposited on the wafer using low-pressure chemical vapor deposition (LPCVD). Several Au depositions using photolithography processes form the absorber for optimal infrared absorption, the electrical leads which define the thermal conductance, and the wiring layer for electrical readout. Ti-Au metal films are deposited using lift-off technique to form the absorber layer [fig. 2(b)]. The thickness of the Au layer deposited on the absorber is chosen to give optimal infrared absorption. For the array, we used 2 nm Ti + 10 nm Au for the absorbing metal film. The thickness of electrical leads of the array was formed from a 5 nm Ti + 200 nm Au film [Fig 2(b)]. The thickness of the Au layer forming the electrical leads on the supports may be varied to tailor the thermal conductance. Due to the large size of the arrays (up to 3in diameter), e-beam lithography is employed to form the contact layer (electrical leads) to each element to minimize lithographic errors. The wafer is then patterned to define the mask for the membrane [Fig. 2(c)], and etched first with an Ar reactive ion etch to remove the absorber Ti-Au layer followed by a CF_4 and O_2 reactive ion etch to remove the silicon nitride. The backside is similarly patterned, aligning to the frontside with an infrared camera, and reactive ion etched to remove the backside silicon nitride to define the silicon frame [Fig. 2(d)]. A 15 μm x 40 μm Ni-In bump [Fig. 2(e)] is deposited on each of the two contact pads located at the center of the device using liftoff lithography to deposit 40 nm Ni + 3 μm In. The nickel layer is used as an intermediate layer to prevent reaction of the indium with the gold during processing. The arrays are diced into a hexagonal shape from the original wafer. Before attaching the thermistors, the backside is patterned with photoresist and hard baked at 130 °C for 5 minutes.

The thermistors are manufactured from a polished slab of NTD Ge material by p doping with a 4.53×10^{16} /cc concentration of Ga and a 1.29×10^{16} /cc compensation of As[19]. Two contacts are defined on a single face of the chip by photolithography. The contacts are B-implanted and deposited with 2 nm Ti + 20 nm Au. Two 15 μm x 15 μm In bump bonds are then patterned on each contact of the thermistor with the same Ni-In process used on the wafer. The chips are diced with a diamond saw and etched in a mixture of HF and HNO_3 to remove saw damage. The resulting chips are ~300 μm long, ~50 μm wide, and 25 μm thick with two contacts 100 μm wide and 50 μm long, separated by 200 μm. The NTD Ge thermistor was located [Fig. 2(e)] over the contacts at the center of the absorber and attached by the In bumps with 1 - 2 N of force by a micrometer. Finally the silicon was removed using a deep trench reactive ion etch to the insulating layer [Fig. 2(f)], followed by liquid etches to remove the thin oxide and silicon layers [Fig. 2(g)]. We have used ICP (inductive coupling plasma) system for deep trench etching because ICP appears to be the most suitable source for this application. This system allows high etch rates, anisotropic etching with selectivity to conventional photoresist masks [16]. Deep reactive ion etcher (DRIE) is manufactured at Surface Technology Systems (STS) and is a single wafer, load locked system that employs inductively coupled plasma etching with the Advanced Silicon Etch (ASE) process. Fig. 3 shows a schematic diagram of the process chamber. The plasma was generated by inductive coupled coil by 13.56 MHz with a maximum power output of 1000W. Another

13.56 MHz generator is used to apply the electrode which allows independent control of the bias potential of the wafer with a power up to 300W. The wafer temperature is maintained less than 80°C via temperature controller which is connected to LN_2 supplier. The system and reaction pressure is controlled by APC (automatic pressure controller). Typical base pressures are 1 x 10^{-7} Torr and operating pressures are from 1 mTorr to above 10 mTorr. During processing, the wafer electrode is lifted using a large bellows from loading height to a processing height within 10 mm of the bottom coil. This reduces ion density loss by diffusion. The electrostatic chuck and platen assembly are cooled by a de-ionized water chiller system. Wafer cooling is provided by mass flow controlled helium on the backside of the wafer. Ion densities of the order of 10^{12} cm^{-3} are obtained at the center of the chamber. We have used SF_6 and C_4F_8 as the etch and passivation gases respectively. SF_6 is used during etch step to etch Si isotropically, this is followed by a short passivation step using C_4F_8. The SF_6 gas provides fluorine radicals which are the isotropic silicon etchants. The C_4F_8 plasma deposits a polymeric passivating layer on surface as well as side wall [16]. The directional ion energy supplied by the capacitive coupled electrode during the etch reaction preferentially removes the paasivation layer from the base of the features hence etching silicon spontaneously. The balance between etch and passivation determines the final process results and this balance can be controlled through a wide variety of process parameter such as etch time, RF power, gas flow, and etch pressure. The etch reaction starts with introducing standby step which consists of high purity N_2 purge followed by a system pumping out. Then etching gases of 130 sccm of CF_4 and 85 sccm of C_4F_8 are introduced using mass flow controller. The etch rate in this system was 2.2 μm/minute. It varies a little depending upon exposed surface area and feature size. In general, to etch through bottom silicon layer, a 350 micron, takes about 160 minutes. The selectivity to etching relative to silicon is 150 : 1 for the oxide and 75 : 1 for the photo resist. The etch process stopped when silicon has cleared. After the final etch, the standby step is repeated and the load lock handler removes the wafer from the reaction chamber.

Fig. 2(h) shows the final single spider web array after releasing and cleaning. The array is made up of 151 2fλ spaced bolometers filling in a 75mm diameter field of view as shown Fig 4. Each bolometer Si_3N_4 support legs are 5 μm wide and 1 μm thick. The web legs are 4 μm wide and 1μm thick leading to a filling factor of approximately 1.5% in each element of the array. This small filling factor over such a large area allows highly energized particle to pass undetected while still capturing the wavelength of radiation being observed. The absorber has a relatively small mass and is suspended by support legs of silicon nitride which provides robust mechanical support and very low thermal conductivity. Therefore the fabricated bolocam device is mechanically insensitive to the relatively low frequency vibration encountered during launch and operation.

III. Bolometer Characterization

The various fabrications and tests of the bolometer arrays for sub-millimeter wavelength are ongoing at JPL/Caltech. The fabricated bolometer array device in this research will be utilized at Caltech Submillimeter Observatory (CSO) located atop Mauna Kea in Hawaii. The bolometer arrays will scan and map the infrared spectrum to gain insight into the origin of the universe.

Fig. 5 shows current-volts curves for optical efficiency calculation. Fig. 5(a) and (b) are filled beam with 300 K blackbody and 77 K blackbody. These current and voltage plots of arrays show the difference in power absorbed between exposure to the 300K and 77K loads and resistance is about mega ohm which is typical bolometer range.

The bolometer array has an 8 arc-minute field of view and band passes at one of λ = 1.1, 1.4, and 2.1 mm per observing run. The fabricated bolometer array will also have one arc-minute, 30 arc-second and 40 arc-second angular resolution at 2.1, 1.1 and 1.4 mm wavelength respectively. The will be cooled to a base temperature of 300 mK provided by an absorption based liquid helium dewar.

IV. Conclusion

We have fabricated and developed arrays of bolometers based on an absorber made from a finely patterned mesh of silicon nitride using deep trench reaction ion etcher. The process offers a method of deep anisotropic silicon etching suited to meeting the needs of spider web bolometer fabrication. This represents a new technology in sub-millimeter wave detector array fabrication. High plasma densities of $SF_6$and C_4F_8 enable deep trench etch applications with critical anisotropy and profile control. In summary of the etching reaction, SF_6 was etchant gas and C_4F_8 was passivation gas for the etching of silicon in this research. Fluorocarbon polymer deposited on the silicon surface during passivation step is removed by reactive ion etching. Increase ion energy in the vertical direction results in a much higher etch rate of removal of fluorocarbon polymer from horizontal surface than from vertical surface. Once polymer was removed, the horizontal silicon surface is exposed to fluorine ions which are the etchants of silcon. The deep silicon etch is occurred during this period while the vertical surface remain protected by the fluorocarbon polymer.

Using deep trench reactive ion etching, silicon nitride spider web bolometer arrays have more easily been fabricated than standard composite bolometers. The freestanding silicon nitride structure consists of a mesh metalized for optimal absorption. The absorber is suspended by silicon nitride legs which provide rigid mechanical support and very low thermal conductivity. The open structure of the absorber, with a geometric factor as low as 1.5%, maintains infrared absorption and minimizes the cosmic ray cross section. We have noted that obtaining low thermal conductivity and heat capacity is important for building fast, high sensitivity bolometers. Silicon nitride supports enable low thermal conductivity and by tailoring the heat capacity of the device we can achieve a highly sensitive bolometer array. Preliminary current-voltage test shown that the fabricated bolometer arrays are in typical range of current bolometers that are in use on ongoing sub-orbital missions and should achieve good performance during use.

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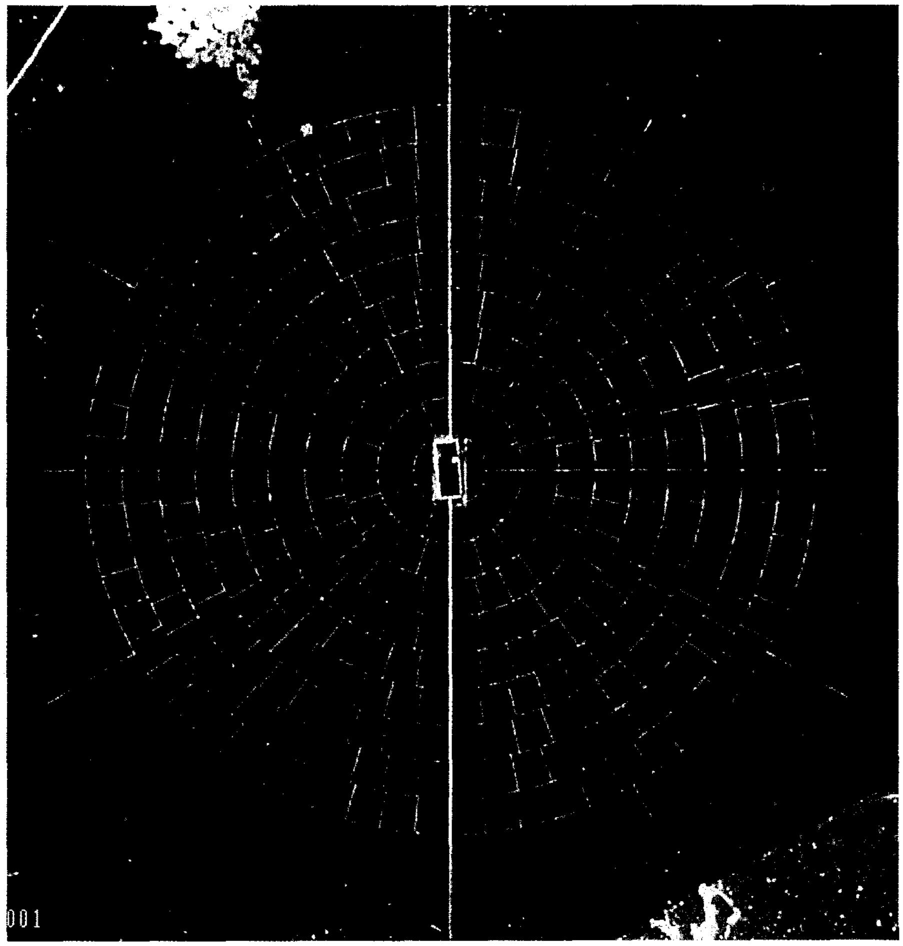


Figure 1. Spider web architecture with NTD Ge thermometer. (put scale)

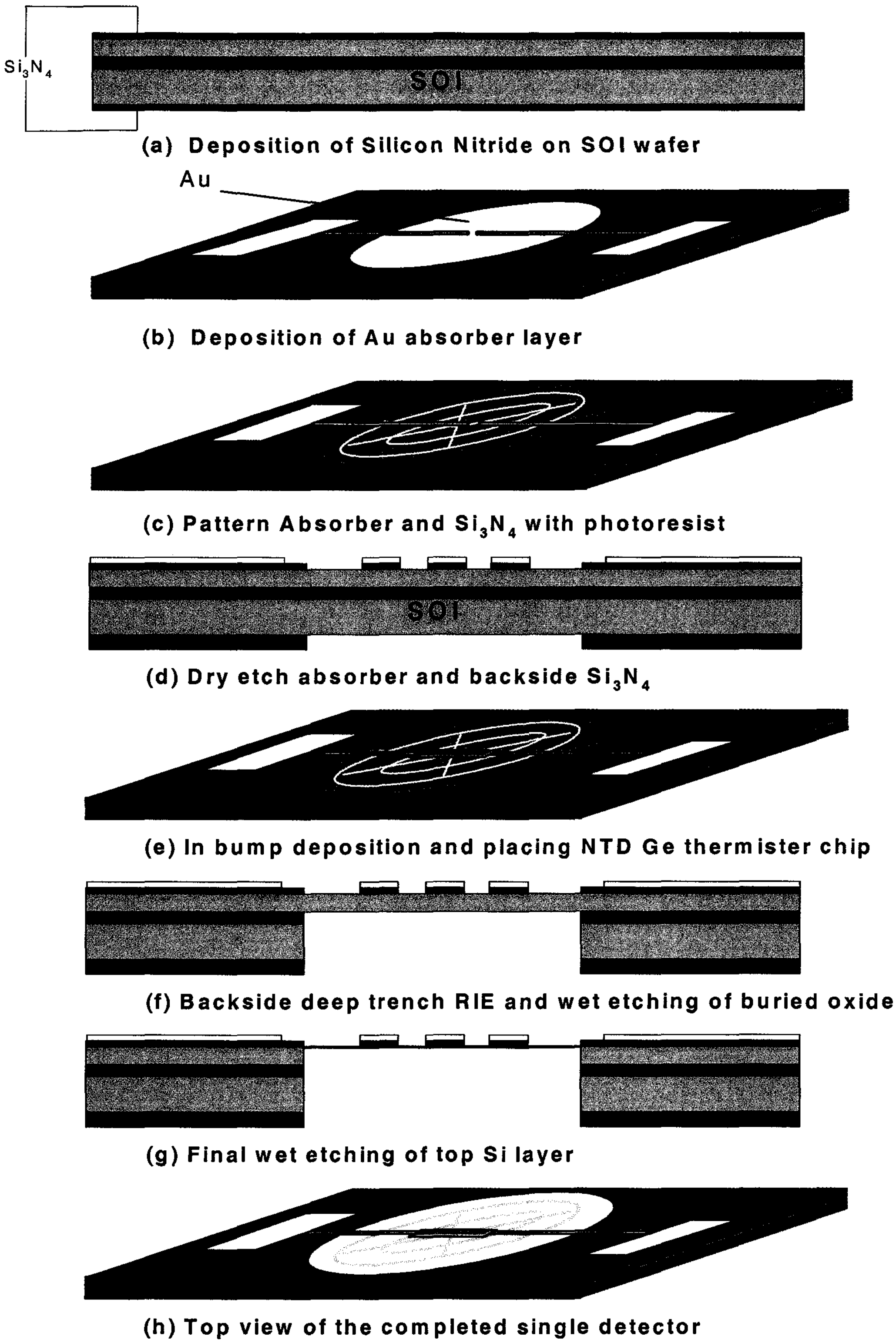


Figure 2. Process Flow diagram

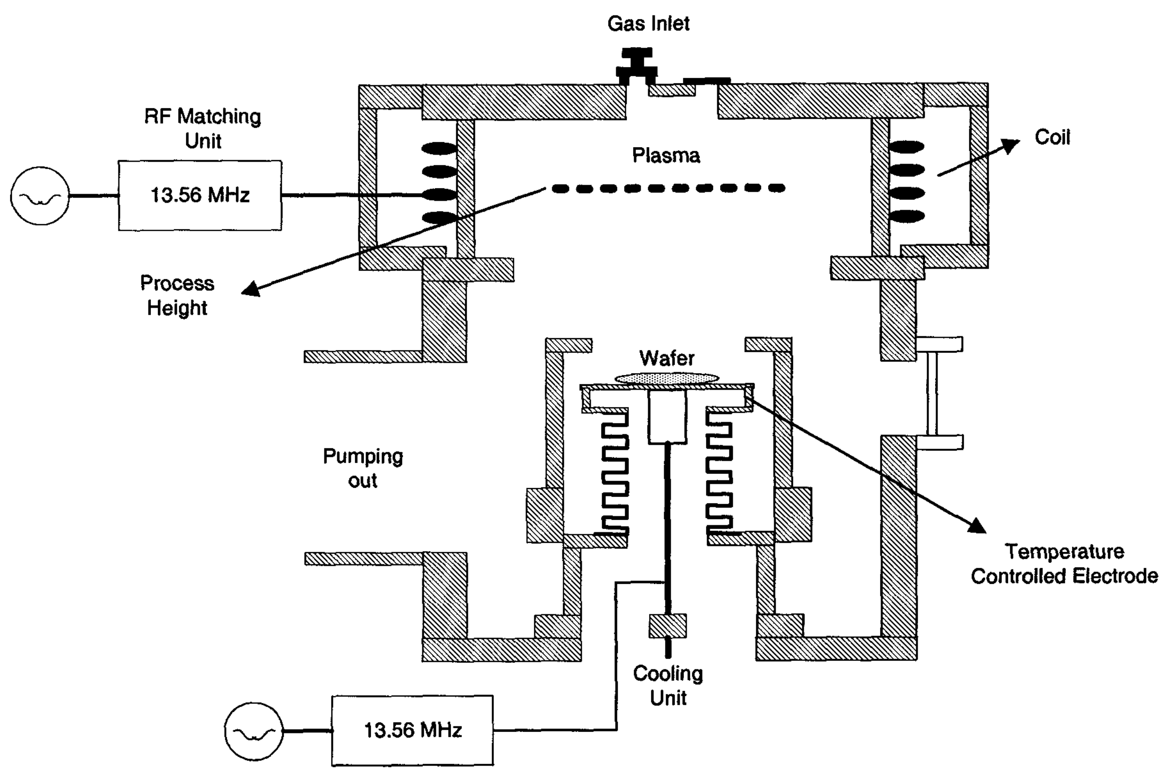


Figure 3. Deep Trench RIE sytem

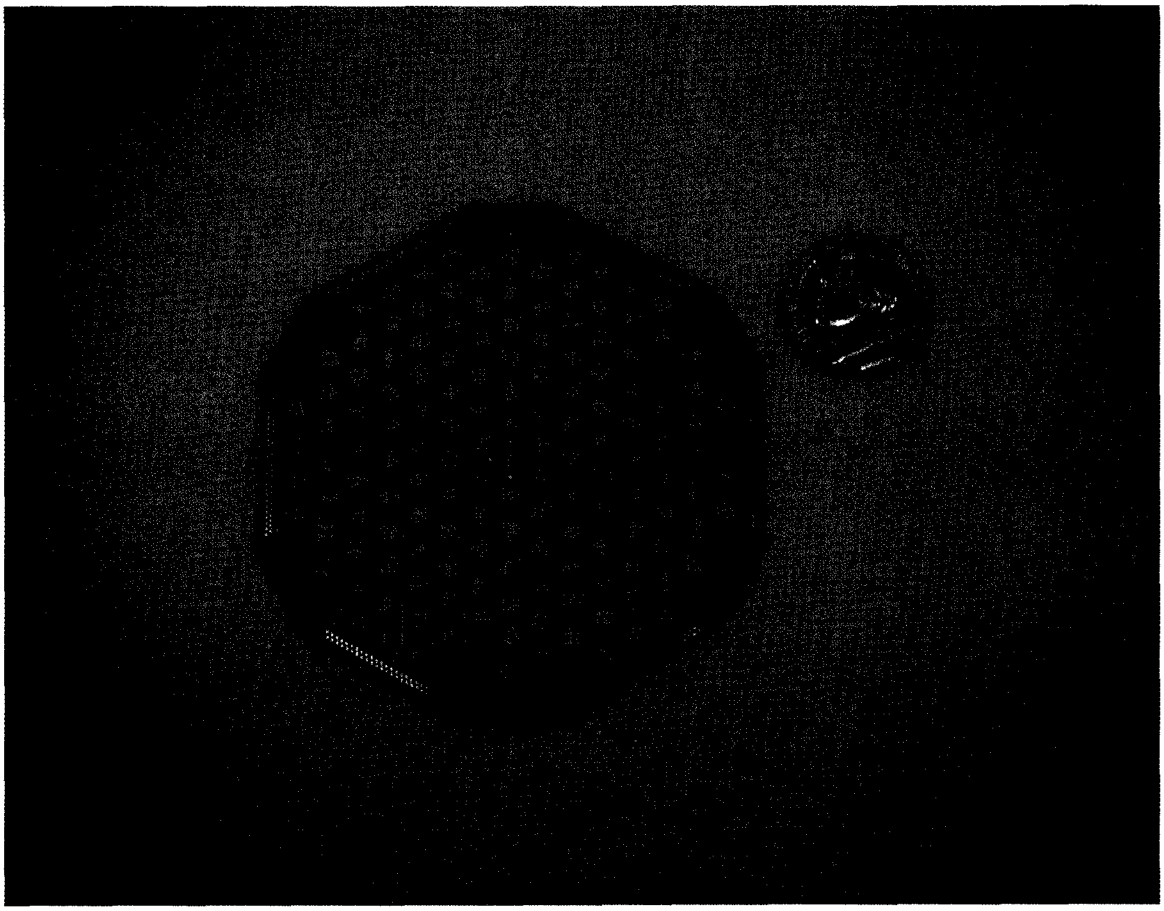
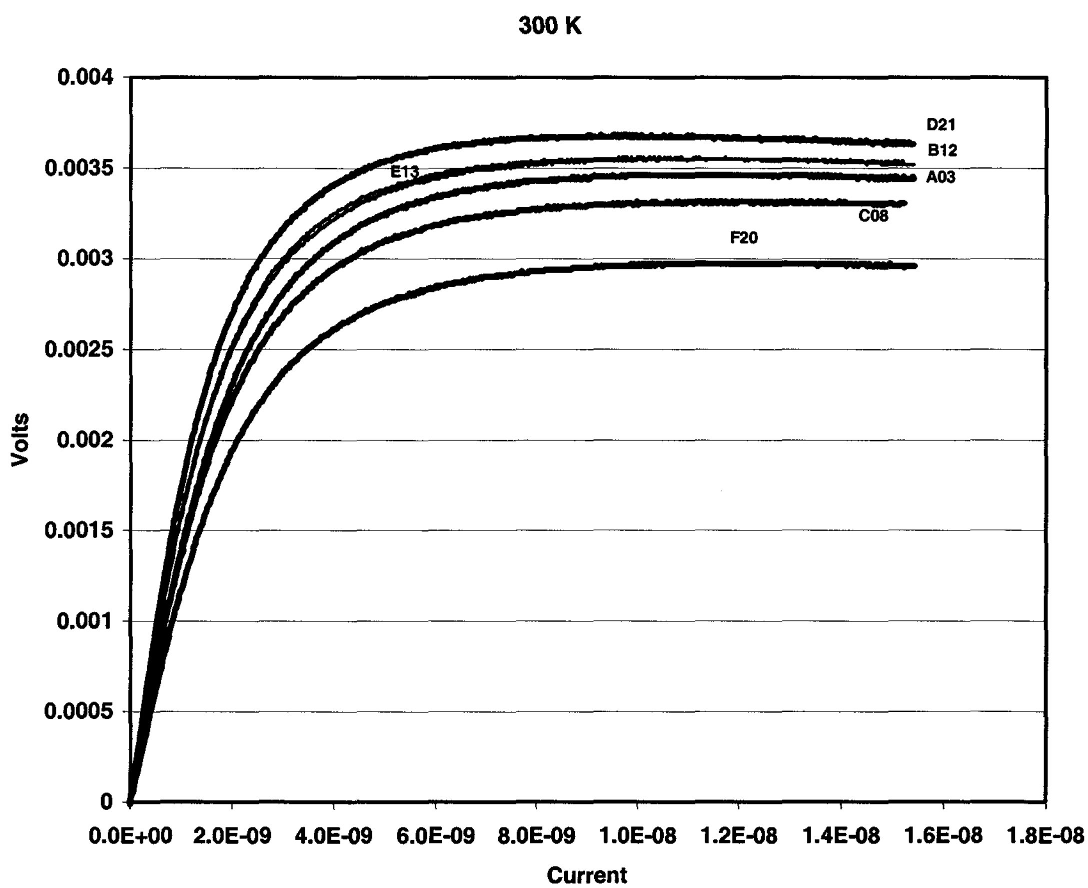


Figure 4. 151 bolometer arrays for earth based bolometer camera


300 K
0.004
0.0035
0.003
0.0025
0.002
0.0015
0.001
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0
Volts
D21
B12
A03
E13
C08
F20
0.0E+00
2.0E-09
4.0E-09
6.0E-09
8.0E-09
1.0E-08
1.2E-08
1.4E-08
1.6E-08
1.8E-08
Current

Figure 5 (a)

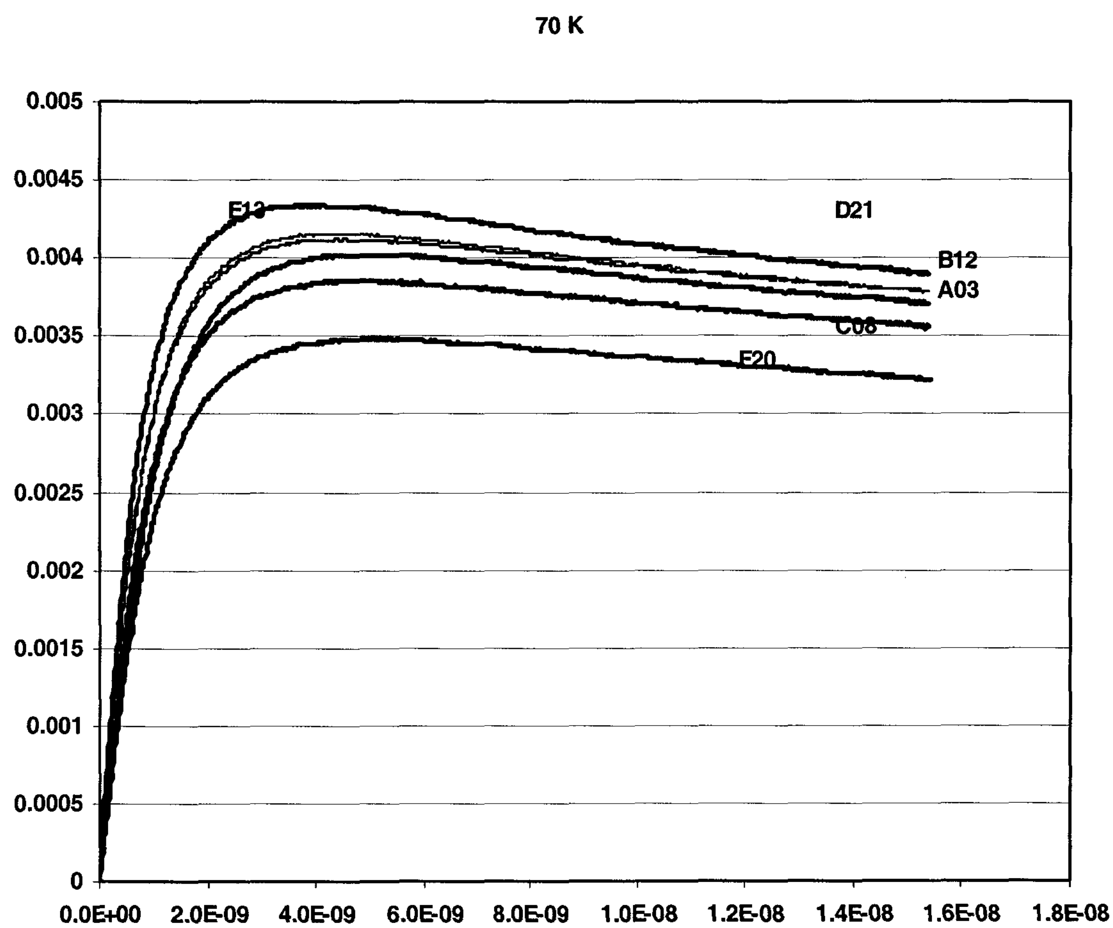

Figure 5 (b). V-I curve of bolometer array at 300K(a) and 70 K(b) test temperature.

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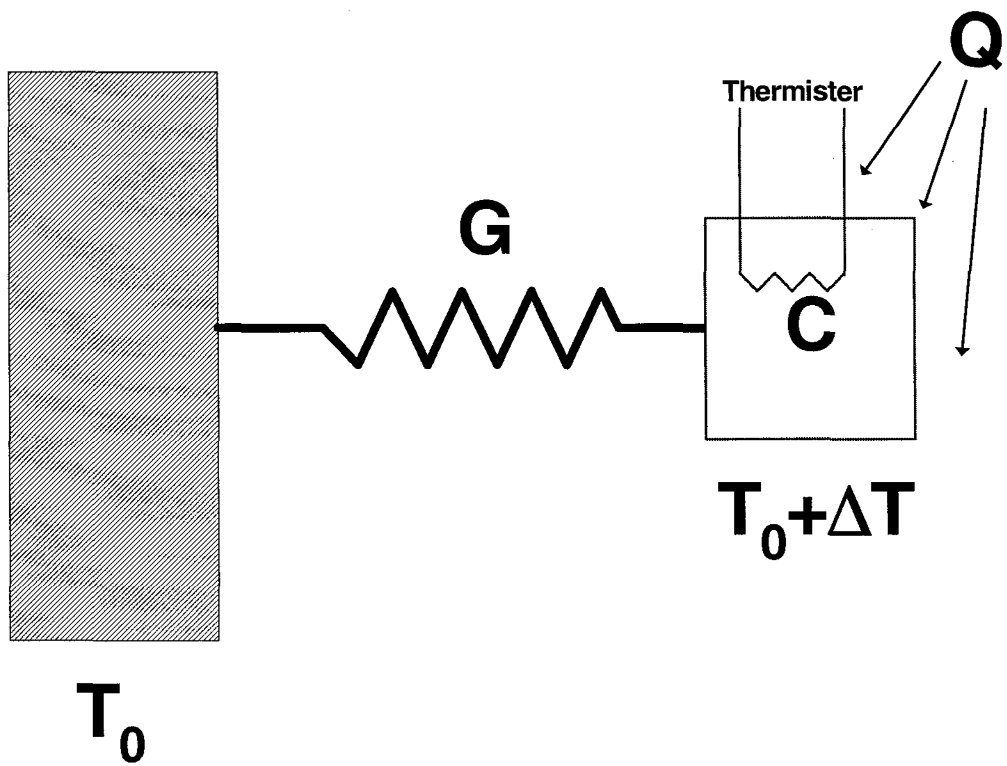
Overview

- What is a the Bolometer?
- Spider Web Architecture Bolometer?
- Applications
- Etching Technology
- Deep Trench RIE
- Bolocam Fabrication Processes
- Summary and Future Work

What is the Bolometer?

; thermal radiation detector

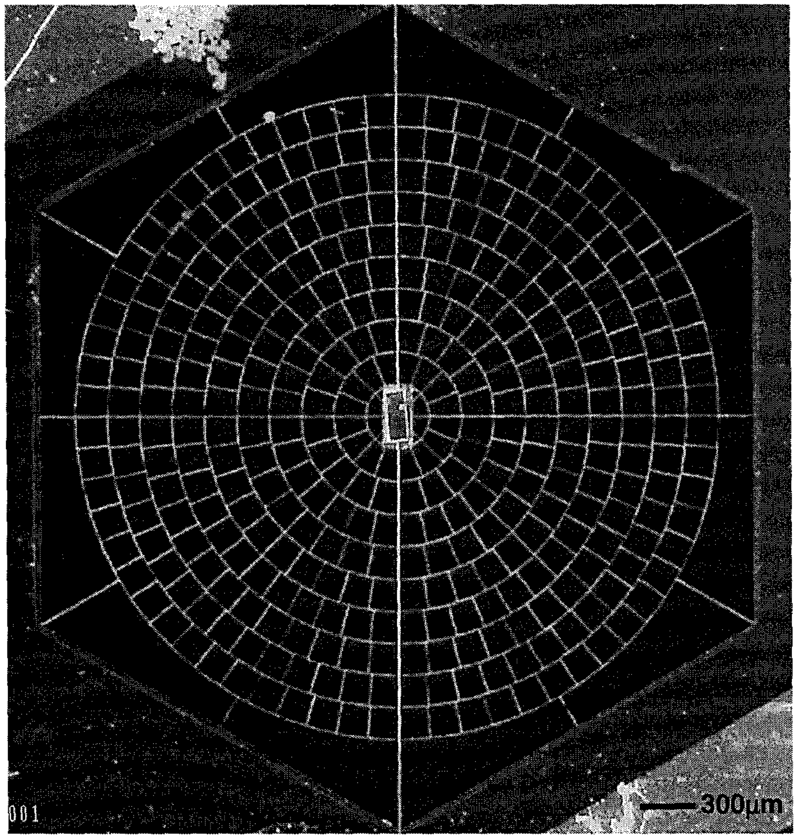


$$NEP_{Bolo} = \frac{4}{3}\sqrt{4k\tau^2 G}$$

$$\tau = \left(\frac{2}{3}\right)\frac{C}{G}$$

- NEP ; Noise Equivalent Power [w/Hz$^{(1/2)}$]
- Q ; Energy
- G ; Thermal Conductivity
- C ; Heat Capacity
- *k*; Initial Temperature
- τ ; Thermal Time Const.
- TΔ ; Temperature Change

Spider Web Bolometer?



Spider web architecture and centered NTD chip

Spider-web architecture provides

- low absorber heat capacity
- minimal suspended mass
- low-cosmic ray cross-section
- low thermal conductivity = high sensitivity

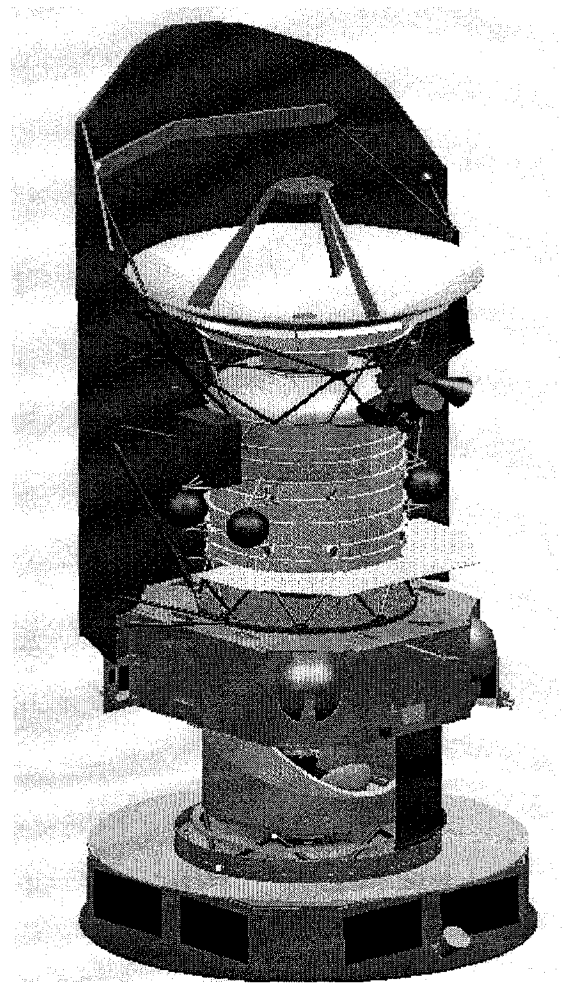
Applications

- HSO (Herschel Space Observatory)
- Planck HFI (High Frequency Instrument)
- Maxima
- Boomerang

Planck and HSO will image the Cosmic Microwave Background, relic radiation from when the universe was 300,000 yrs old, and probe distant galaxies.

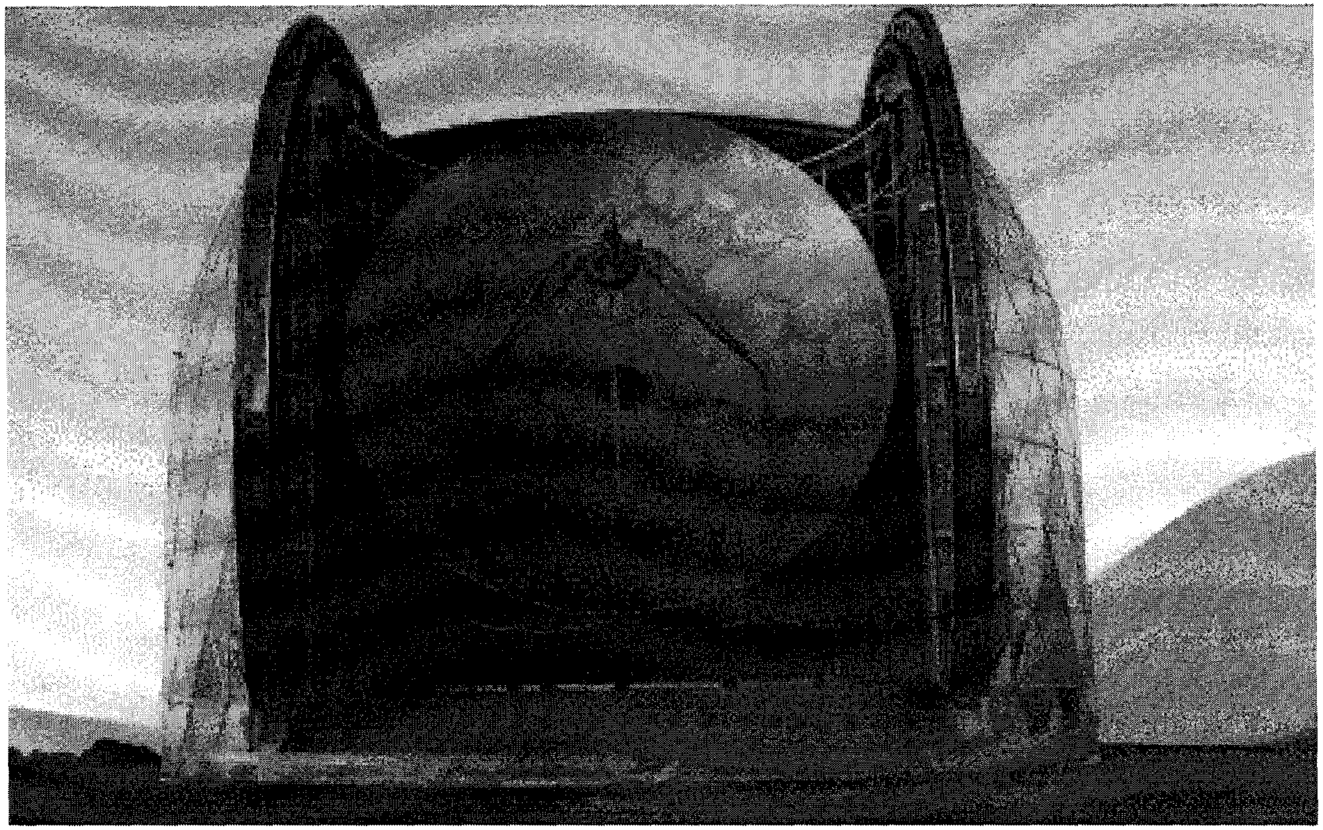
This will allow us to view and study the origins of our universe as it has never been possible to do until now.

Space-Borne Observatory



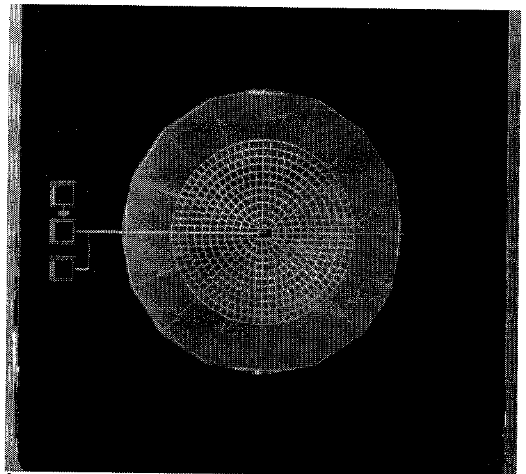
Applications

Earth-Borne Observatory



Caltech Submillimeter Observatory (CSO) located atop Mauna Kea in Hawaii.

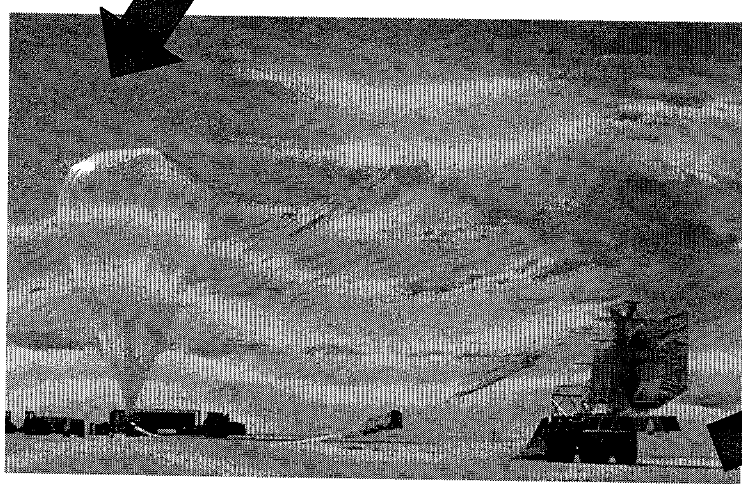
Applications



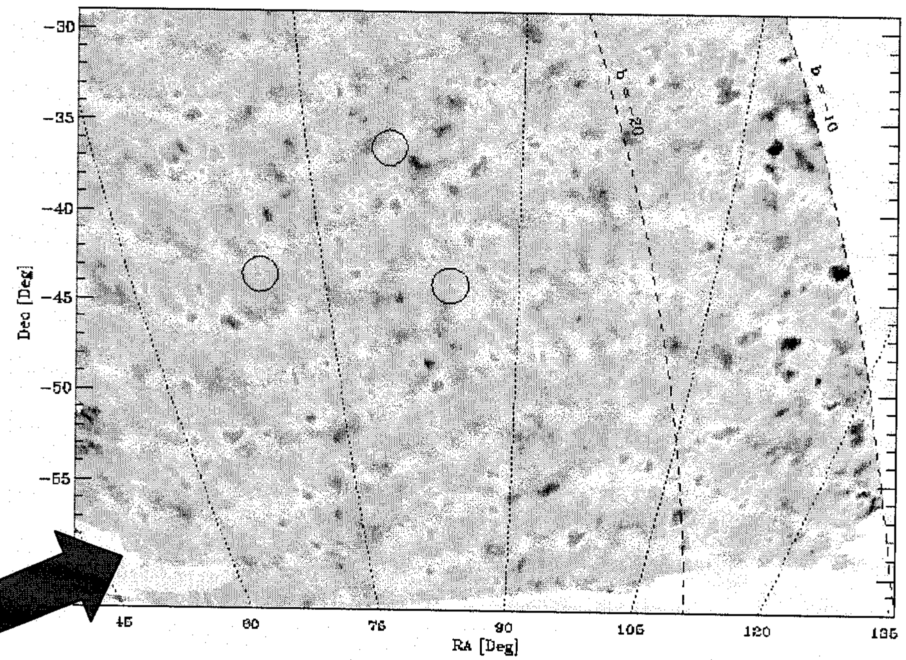
JPL Spider-web Bolometer

High Sensitivity Bolometers Operating at 0.1 K

BOOMERANG creates the first resolved map of CMB anisotropy demonstrating FIRST and Planck detector technology.



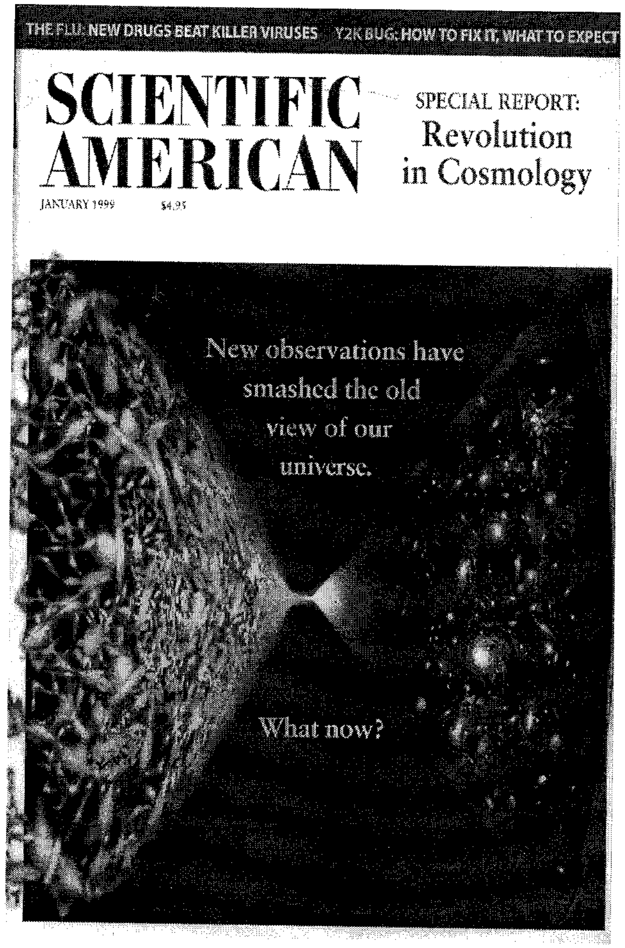
BOOMERANG Antarctic Balloon Experiment



First Resolved Map of CMB Anisotropy

Applications

Jan. 1999



Nov. 1999

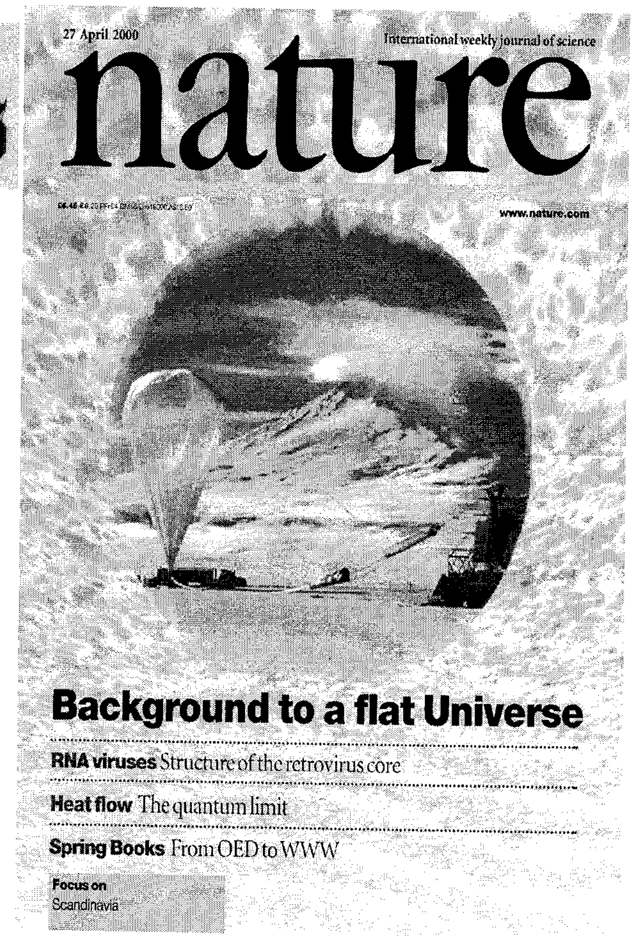

The New York Times

FRIDAY, NOVEMBER 26, 1999

Radiation Ripples From Big Bang Illuminate Geometry of Universe

By JAMES GLANZ

Apr. 2000



Bolometer Array (Bolocam)

- Why ?
  - Most significant problem of mm-wave ground-based observations: SKY! Sky noise

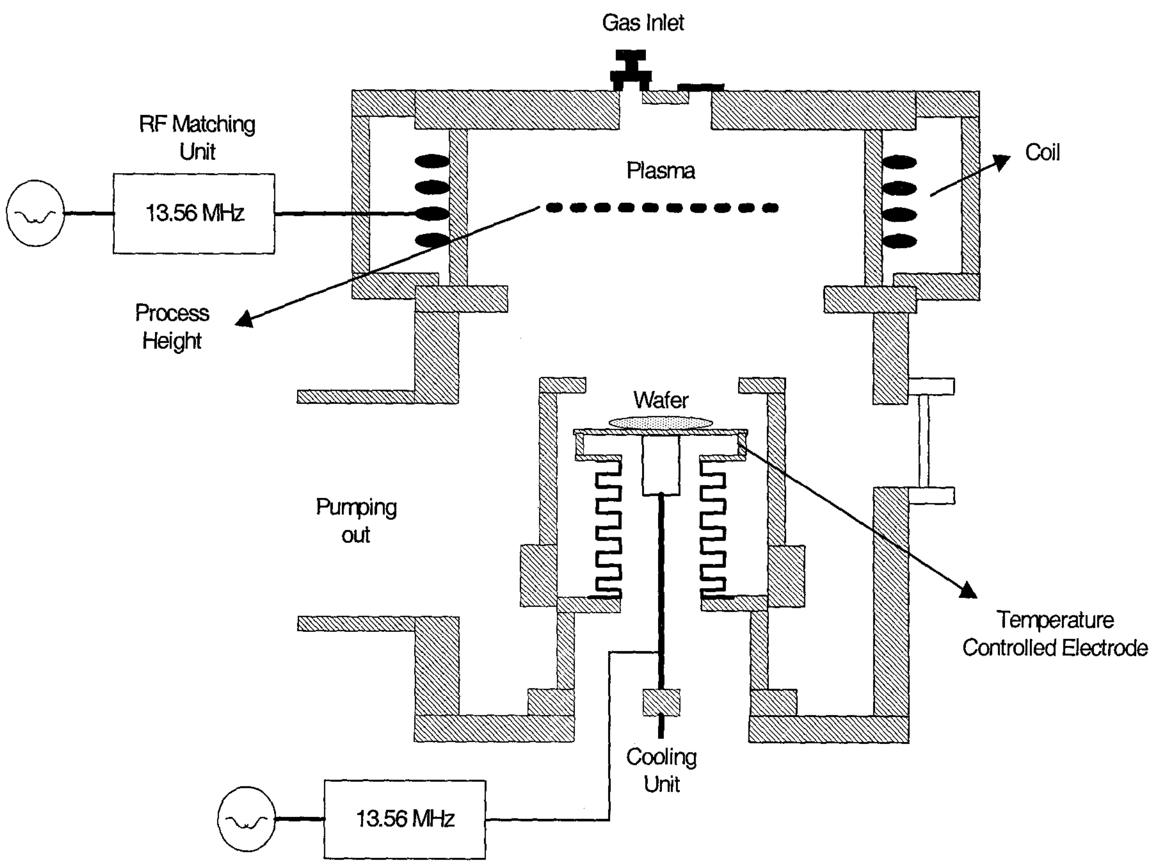
- Requirements
  - Observation bands: 1.1, 1.4, 2.1 mm
  - 144-pixel spiderweb bolometer array operated at ~ 270 mK
  - Operated at the Caltech Submillimeter Observatory (Mauna Kea): 10.4 m dish
  - $NEP_{det} \sim 3 \times 10^{-17}$ W/$\sqrt{\text{Hz}}$, C = 1pJ/K at 300 mK, 0.4 pJ/K at 100mK
  - Good overlap of beam transmission through atmosphere to give excellent instantaneous sky subtraction

Etching Technologies

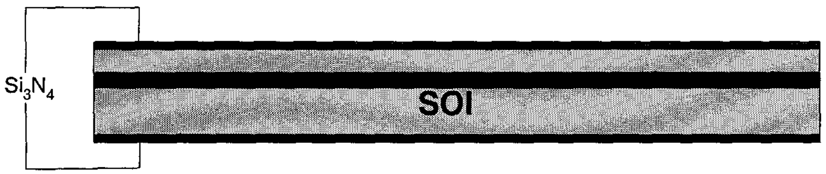
- Wet
  - Anisotropic Etching
    - •KOH Etching (Orientational Dependent Etching)
    - •EDP (ethylenediamine, pyrocatechol, and water)
  - Isotropic Etching
    - •HF Etching
    - •HND (HF + Nitric Acid + DI)
    - •HNA (HF + Nitric Acid + Acetic Acid)
    - •Mixture of Acids

- Dry (plasma chemistry)
  - Physical Etching
    - Ion bombardment (RIE ; reactive ion etching)
    - Directive (anisotropic)
    - High ion energy (could cause surface damage)
    - Most common in industry
  - Chemical Etching
    - Radical etching(ECR, electron cyclotron resonance)
    - Isotropic
    - Usually high density
    - Less ion energy

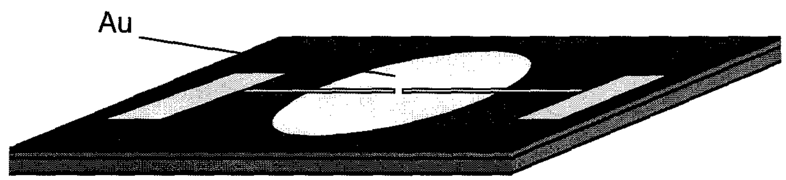
Deep Trench RIE (Reactive Ion Etching)



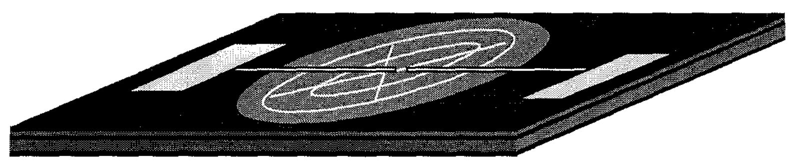
Fabrication of Detector Arrays, I



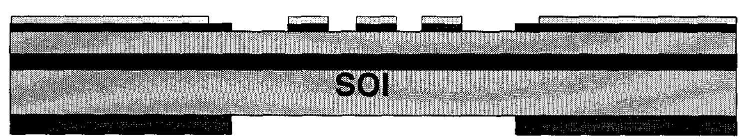
(a) Deposition of Silicon Nitride on SOI wafer



(b) Deposition of Au absorber layer

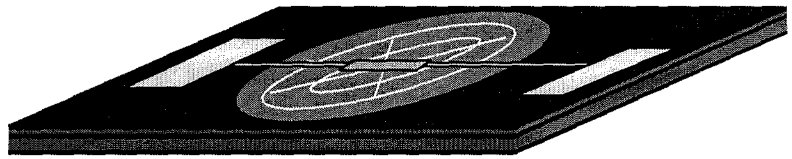


(c) Pattern Absorber and Si_3N_4 with photoresist

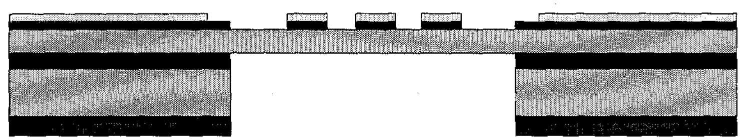


(d) Dry etch absorber and backside Si_3N_4

Fabrication of Detector Arrays, II

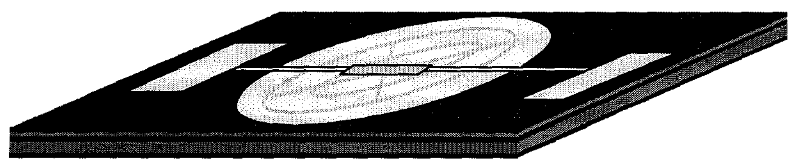


(e) In bump deposition and placing NTD Ge thermister chip



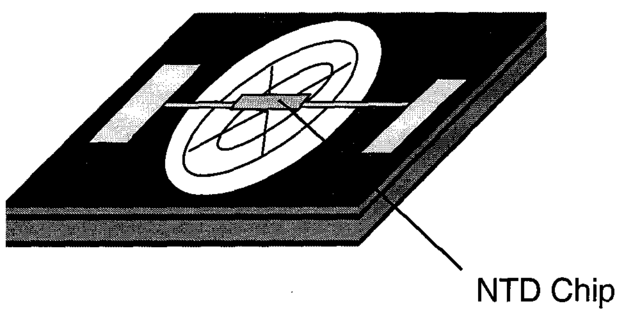
(f) Backside deep trench RIE and wet etching of buried oxide

(g) Final wet etching of top Si layer

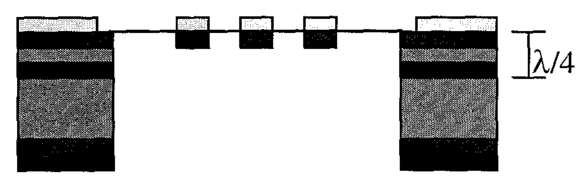


(h) Top view of the completed single detector

Fabrication of Detector Arrays (cont.)



Wet etch top Si from backside and release web



Cross-sectional view of the Arrays

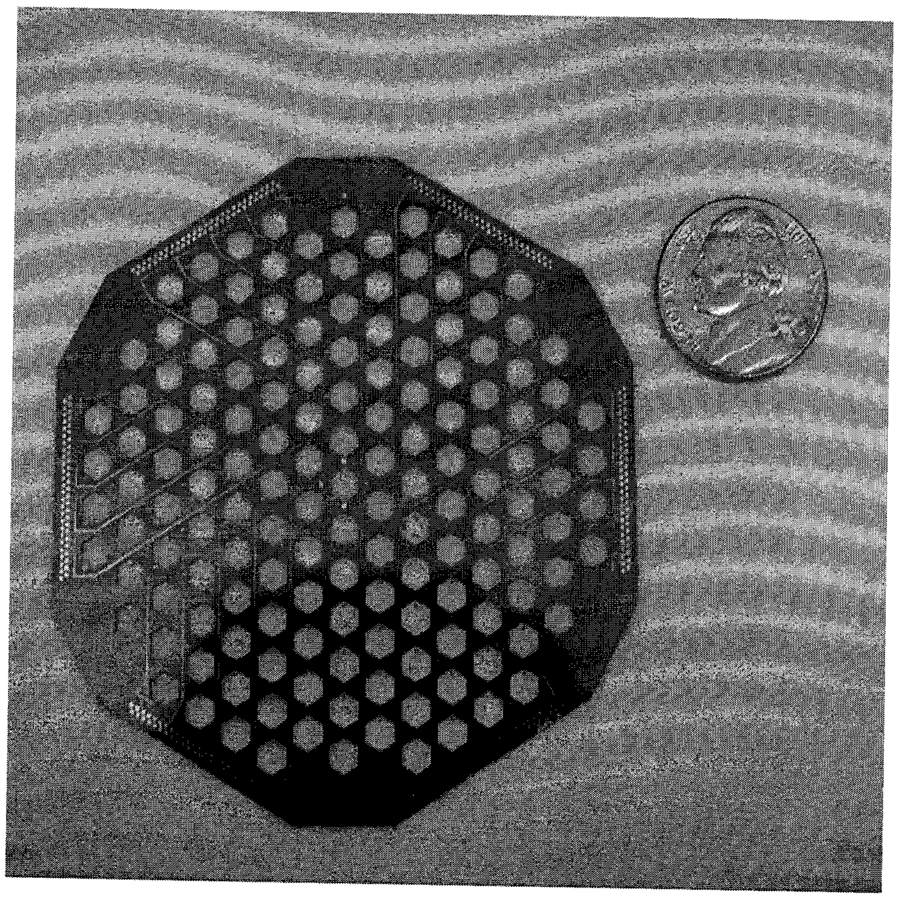
Process Summary

- 4" SOI wafer with 1μm thickness of LPCVD Si_3N_4 used.
- Stack of 6 masks used in the fabrication of the bolometer array (bolocam) device
- Etch processes have been developed

Wet etch ⟶ **Deep Trench RIE**

- Electron beam Lithographic employed to minimize lithographic errors
- Non-contact lithographic method (stepper) employed instead of contact method, and minimized surface contamination
- Plasma ash process has been used every interval to keep clean surface

Fabrication of Bolometer Arrays - Yield



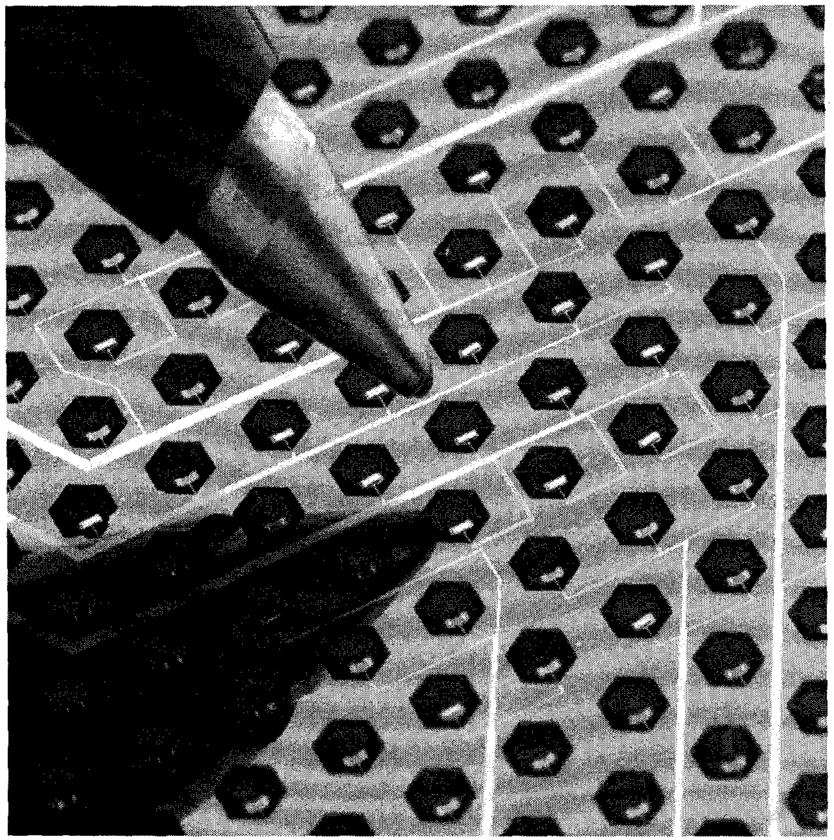
➢ **Bolocam ; 151 Detectors**

- Web Failure due to membrane breakage : 18
- Chip Failure due to electrically short or open: 10
- Lithographic Error : 2

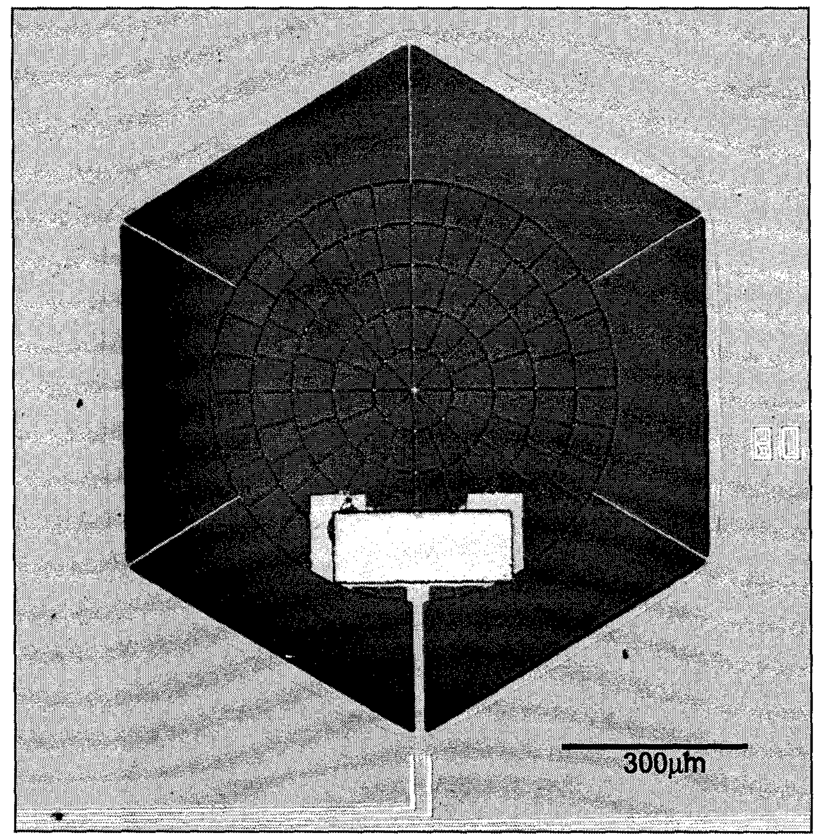
➢ **Yield = 80.2 % (121/151)**

We have successfully delivered the 151 detector array Bolocam with a better than 80% yield.

Fabrication of Bolometer Arrays



Bolocam (151 Detectors)

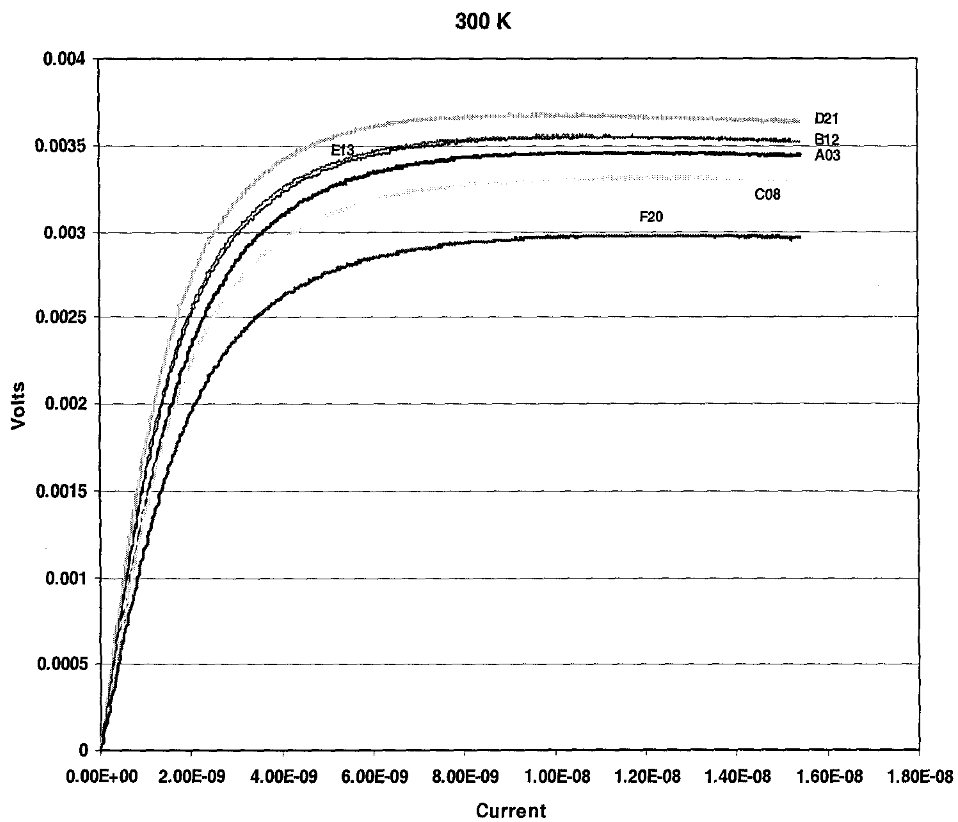


Single detector

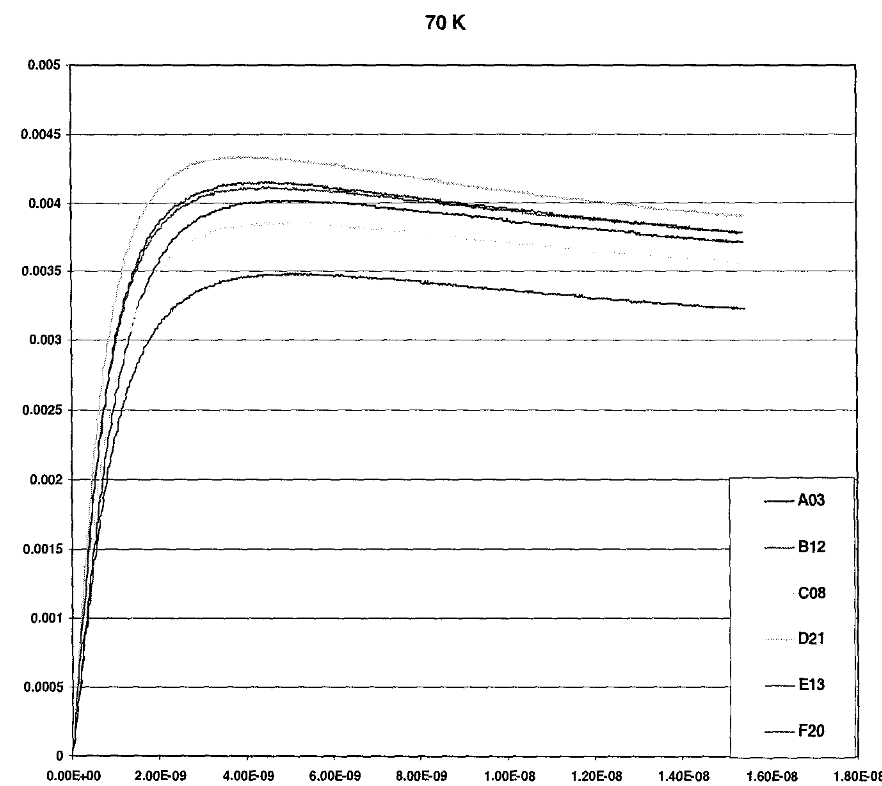
Challengings

- Lithographic Error
  - **Most critical lithography steps now use non-contact aligners (stepper, e-beam)**
- In bump
  - **Indium reacts with Au at high temperature above 130^{0}C in a short time . So establish the highest temperature to which the detector can be subject to and remain viable**
- Uniformity across surface
  - **Ultra clean process & Deep RIE development required because any residue on the surface could cause a bump**
- Final web structure treatment (releasing) from deep trench RIE needs to improve to increase yields

Electrical Characterizations



Bolocam array tested at 300 K



Bolocam array tested at 70 K

Summary and Future Work

- We have fabricated and developed extremely sensitive Si_3N_4 micromesh spider web bolometers with 151 detectors for sub-millimeter astrophysics using microelectromechanical system (MEMS) techniques
- Process techniques have been developed, resulting in an increase the viability of the applicable device fabrication. (ex. ; NTD chip bonding, stepper lithography)
- Final devices have 80% or better yield with array performance to specification
- To increase device yield, some processes such as cleaning and lithography are still required to improve
- Device performances are
  - **200 Å Au absorber on 1μm Si_3N_4 membrane, etched into "spider-web" to minimize C_{Au}, G**
  - **NTD Ge thermistor senses T of Au (actually dominates C)**
  - **G determined by thickness of Au leads ($G_{SiN} << G_{Au}$)**

Summary and Future Work

- **Optical efficiency**
  ; ratio between the observed and expected power difference. This includes absorber efficiency, filter efficiency, as well as geometric losses
- **Optical time constant**
  ; to determine that the bolometers arefast enough to respond to the astronomical signal
- **Beam-mapping**
  ; measures the sensitivity of the system as a function of angle from the optical axis
- **FTS**
  ; to measure the spectral bandpass
- **Dark run**
  ; to measure the intrinsic bolometer characteristics
- **Noise**
  ; to establish that the noise from the bolometers and the electronics are low enough to meet our sensitivity goals