A High-Power Wideband Cryogenic 200 GHz Schottky "Substrateless" Multiplier: Modeling, Design and Results

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Abstract — A high-power doubler for the frequency band 184 to 212 GHz has been fabricated and tested. The first circuit measured gives an output power over 30 mW across the band at room temperature with peaks around 48 mW at 190, 200 and 210 GHz. Even better results are expected from future testing under cryogenic conditions at approximately 100 K ambient. The multiplier is a high power design used as a first stage for multiplier chains spanning the frequency range of 1 to 3 THz. It is based on the "substrateless" monolithic integrated circuit topology reported earlier. Its strength is passive circuitry with lower-loss than conventional MMICs, due to the removal of the semiconductor substrate from beneath most of the metallic traces. Further, it facilitates the optimum design of broadband multipliers by simplifying the transitions between waveguide and diode sections of the circuit. Since the multipliers are operated at relatively high input power (up to 250 mW), low temperature (down to 100 K) and wide bandwidth (14 %), accurate analysis of the doubler characteristics affected by these conditions is important. The results of the continuing JPL Schottky diode physical modeling effort are discussed, including the effects of temperature and high power operation. A thermal analysis of the doubler is also shown.

I. Introduction

Currently there is a demand for a wide-bandwidth frequency multiplier chains [1-3] with outputs above 1 terahertz for use in sub-millimeter wave heterodyne receivers. These space-borne radiometers are primarily intended for astrophysical observation. The Jet Propulsion Laboratory maintains a concentrated effort to develop and implement novel technologies to produce robust, reliable and repeatable planar Schottky diode multipliers for these applications [4]. In order to produce useable output power at the output frequency, the first stage in the chains are being pumped at the 200 mW and above level at W-band [5]. This paper will focus a few of the consequences of operating at these high power levels.

II. Design and Performance

The multiplier consists of two components – nonlinear solid state devices (Schottky diodes) and the surrounding input, output and impedance matching circuitry. The circuit design process has been discussed previously [5–7] as has been the fabrication [8]. Figure 1 shows the 200 GHz doubler mounted in the bottom half of the split block. In order to allow matching and to distribute the power, the circuit employs six diode anodes in a linear array. The diodes are integrated with metallic circuitry using a GaAs MMIC process. Additional passive matching is accomplished in waveguide. The lines fabricated on GaAs act as waveguide transitions as well as part of the impedance matching, and much of it is etched away as discussed in the earlier references.

The doubler uses a balanced planar diode configuration [9,10], incorporating symmetrical series of diodes configured so that they only respond to odd harmonics at the input and even harmonics at the output. This makes it easier to separate the frequencies and which makes these wide band designs possible.

The performance of the doubler at room is shown in Figure 2. The peak power is around 50 mW, and the peak efficiency is around 30 percent over a broad band.

III. Thermal Model

The doubler was designed for an input power of 200 mW, and the test input power was greater than 200 mW over part of the band. In order to estimate the operating temperature, a basic one-dimensional "series-resistor" model has been developed with the help of Dr. Terry Cafferty at JPL. The system analyzed is depicted schematically in Figure 3. Since the chip is symmetrical about the center plane in the input waveguide, only half has been analyzed, with no heat assumed to flow across the symmetry plane.

Further assumptions are that all anodes dissipate the same power, radiation and convection can be neglected,

and that the block is at a known (ambient) temperature. Published thermal conductivity data for undoped GaAs between 100 to 600 K has been used, and the effect of doping neglected. The thermal conductivity of GaAs decreases with temperature in this temperature range. It is assumed that the beam lead is 1.5 microns thick and 50 microns wide by 40 microns long and is made of gold.

Shown in Figure 4 are maximum diode temperature as a function of input power, based on a conservative 25 percent conversion efficiency. Traces for ambient temperatures of 100 and 300 K are shown. This indicates that operation at room temperature is marginal, but at 100 K or so the multiplier should operate with a comfortable margin.

IV. Current Saturation

For the Herschel Space Observatory it has been decided to operate at a low temperature, both for thermal margin and to get improved multiplier performance [11]. We have an continuing effort at JPL to improve the modeling of the diodes, especially temperature and high frequency effects. Most of the effects have been covered previously, [12–14], but inclusion of the time dependence of the current saturation has not been previously included in multiplier design. A simple model has been developed for this purpose.

Current saturation at high fields in GaAs results from the *decrease* in velocity with field once a threshold field around 4 or 5 kV/cm has been reached. This is due to electrons gaining enough energy from the field to scatter into the upper, low-mobility valleys of the electron conduction band. This acts as a current limit in the undepleted epitaxial region of the diode. Current saturation reduces the efficiency of the diode as a multiplier because it decreases the ability of the charge at the edge of the depletion region to move around at the signal frequency and modulate the capacitance, generating the varactor non-linearity.

There are several equations used to describe velocity saturation. The simplest and oldest is the Kramer and Mircea formula [15]:

$$v(E)=\frac{\mu_0 E+v_s(E/E_N)^4}{1+(E/E_N)^4} \tag{1}$$

where v is the velocity, E the magnitude of the electric field, v_s the ultimate saturation velocity at about 20 kV/cm, and E_N is a characteristic field which determines where the peak velocity occurs. Usually current saturation, including transient effects are modeled using Monte Carlo simulations [16, 17]. In this case, single particle Monte Carlo simulations are used to determine the fitting parameters of equation (1). Since Monte Carlo calculations take large amounts of computer time, it is desirable to incorporate these effects into a harmonic balance (HB) circuit simulator using a simple model which can be integrated using the Runge-Kutta type integrators normally used in HB simulators. We propose to use a time constant based formulation somewhat similar to that introduced in [18]. The epi current is divided between two resistances representing the dominant two conduction band valleys in which electrons travel, as illustrated in Figure 13. Defining μ_0 as the lower valley mobility, (about 4000 cm^2/Vs or higher at reduced temperatures), and μ_1 is the upper valley mobility (about 400 cm^2/Vs) and n_0 and n_1 as the corresponding valley populations, the velocity in equation (12) can be written:

$$v(E)=\left(\mu_0\frac{n_0}{n}+\mu_1\frac{n_1}{n}\right)E \tag{2}$$

with n the total electron concentration in the undepleted epi. Then, several coupled differential equations are used to represent the time-dependent behavior of the velocity. The upper valley population is described by:

$$\frac{dn_1}{dt}=\frac{n_{1s}(V)-n_1(t)}{\tau} \tag{3}$$

where $n_{1s}(V)$ represents the static population of the upper valley, derived by combining equations (1) and (2) and noting that the total electron concentration is the sum of the populations of the two valleys, i.e. $n = n_0 + n_1$. V is the instantaneous voltage seen by the electrons (inside the carrier inertia inductance), and the field E is found by dividing V by the undepleted epi-layer thickness, t_{UD}. The time constant, τ depends on V.

The current through the inductor representing carrier inertia depends on the total epi voltage, V_{tot}:

$$\frac{di}{dt}=\frac{V_{tot}(t)-V(t)}{L_i} \tag{4}$$

where L_i is the carrier inertia inductance, equal to:

$$L_i=\frac{m^* t_{UD}}{q^2 nA} \tag{5}$$

with m^* the effective mass and A the area of the diode. The total current through the inductance is:

$$i=nvA. \tag{6}$$

To simulate the full diode, of course, other equations must be included to model the epi capacitance, as well as the junction capacitance and conduction current.

Currently, it appears that the above model, simple as it is, is impossible to incorporate into commercial HB simulators. Therefore a version of the Siegel/Kerr reflection algorithm HB simulator [19] has been written, and the model incorporated into it. Additionally, the

simple series resistor–diode junction model we normally use in commercial programs is modeled for comparison. In this case, only the diode efficiency was compared, neglecting the circuit resistive and mismatch losses.

At room temperature the two give similar results, indicated in Figure 6. Figure 6 indicates the improvement in efficiencygiven by reducing the temperature to 100 K. The embedding impedances have been assumed to be equal in the two cases.

IV. Current Saturation

Measured results of the performance of a wide-band high-power 200 GHz doubler have been presented with peak power of 50 mW and peak efficiency over 30 percent. A thermal analysis indicates the doubler will not over heat, and a sophisticated temperature-dependent diode model useful for high power and frequency has been described and tested.

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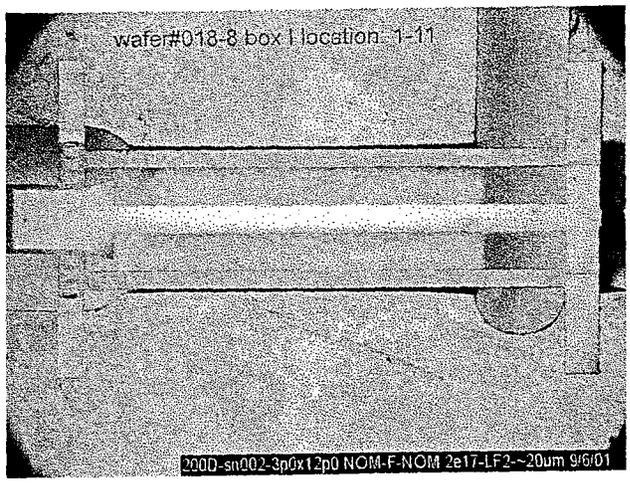

Figure 1. Photo of 200 GHz doubler in block.

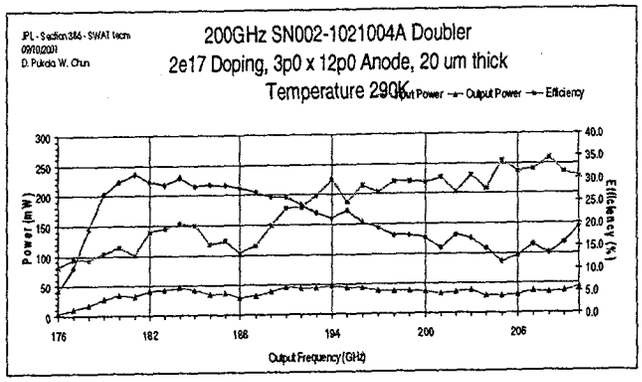

Figure 2. Measured performance of 200 GHz doubler.

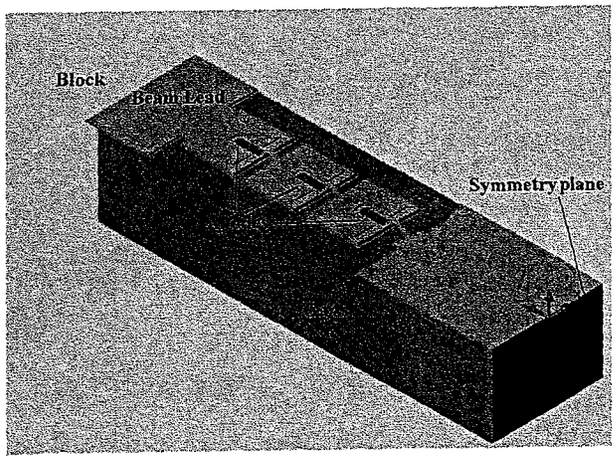

Figure 3. 200 GHz doubler thermal model. The anodes are heat sources and the block is a heat sink No heat flows across all other surfaces.

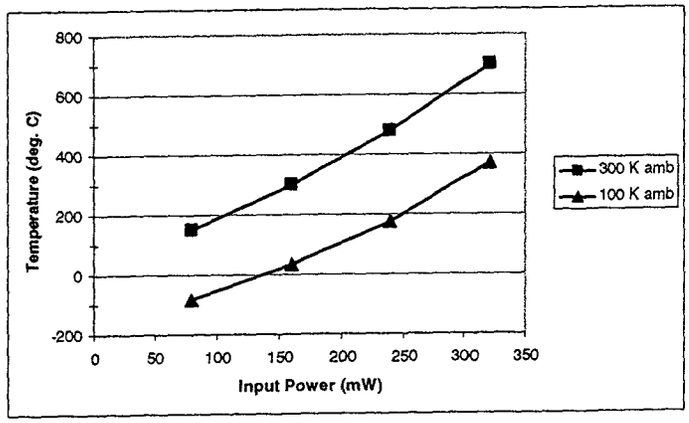

Figure 4. Worst case anode temperature at room temperature and 100 K.

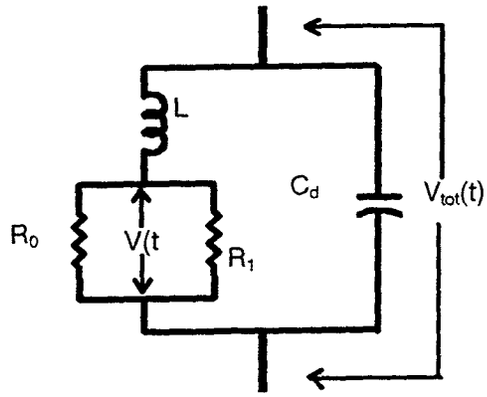

Figure 5. Model of undepleted epi. R_0 and R_1 are inversely proportional to μ_0 (high) and μ_1 (low).

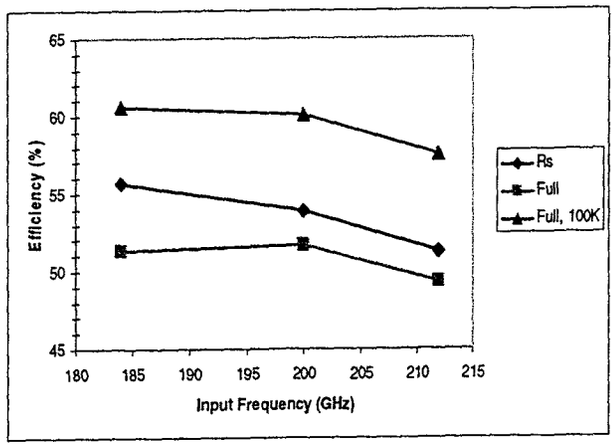

Figure 6. Comparison of performance calculated with fixed-Rs model with full model at 300 K and 100 K.