

Carrier Synchronization of Offset QPSK For Deep Space Telemetry

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Abstract—Offset Quadri-Phase Shift Keying (QPSK) will be the telemetry modulation scheme for many future deep space missions, in accord with new CCSDS standards. In particular, it will be used with relatively high bit rates, in excess of 2 Mbps. A carrier synchronization loop for offset QPSK has been incorporated into the Block-V Receiver of the Deep Space Network. This loop implementation is an appropriate design choice for bit rates in excess of 2 Mbps. However, the loop implementation that has been selected has the disadvantage that it permits four possible lock points within one cycle of carrier phase. This contrasts with only two possible lock points per cycle of carrier phase for the optimal offset QPSK loop. However, by a simple strategy of periodic bit inversions at the modulator coupled with a reciprocal operation at the demodulator, a simpler two-fold phase ambiguity is effected. The two-fold phase ambiguity is resolved by a unique synchronization word, just as is commonly done already with Binary Phase-Shift Keying (BPSK). This strategy of reducing the four-fold phase ambiguity to a two-fold phase ambiguity does require periodic bit inversions at the modulator. So this solution is not available for the general offset QPSK modulator that does not include the necessary periodic bit inversions.

TABLE OF CONTENTS

1. INTRODUCTION
2. OFFSET QPSK CARRIER LOOP
3. PHASE AMBIGUITY RESOLUTION
4. ALTERNATE LOOP DESIGN
5. CONCLUSIONS

1. INTRODUCTION

Deep space telemetry is received at the Deep Space Network (DSN) using mainly the Block-V Receiver. This receiver has carrier synchronization loops and coherent detectors and is designed to support both Binary Phase-Shift Keying (BPSK), with or without a residual carrier, and Quadri-Phase

Shift Keying (QPSK).[1] The carrier synchronization loop for QPSK can also be made to support offset QPSK by the simple addition of a delay element. It is the QPSK loop of the Block-V Receiver, as modified by a delay element for operation with offset QPSK, that is the subject of this paper.

Offset QPSK has a well-known advantage over QPSK. If a filter is used at the transmitter for spectral shaping, a nonlinear power amplifier will cause spectral regrowth of the sidebands for QPSK, defeating the effort to shape the spectrum. The most power-efficient amplifiers are nonlinear, so for deep space telemetry, the power amplifiers are always nonlinear. The worst of this spectral regrowth is the result of the instantaneous 180° phase transitions inherent in QPSK. Since offset QPSK eliminates the 180° phase transitions, offset QPSK experiences much less spectral regrowth. This advantage of offset QPSK over QPSK is well documented elsewhere [2] and is not the subject of the present paper.

There is another advantage of offset QPSK over QPSK. This concerns the phase ambiguity arising in the carrier synchronization loop. With QPSK, there is a four-fold phase ambiguity. On the other hand, with offset QPSK, it is possible to reduce the phase ambiguity to two-fold, which is easier to resolve. This advantage of offset QPSK is of some importance for deep space telemetry.

The two-fold phase ambiguity of BPSK is routinely resolved within the DSN by means of unique word detection. The possibility of achieving the better bandwidth efficiency of QPSK without complicating the problem of resolving phase ambiguity is quite attractive. If offset QPSK is carefully implemented, the phase ambiguity is two-fold, as with BPSK, and a uniform method of resolving phase ambiguity becomes possible. This is an important operational consideration.

In the Block-V Receiver, the QPSK carrier loop was designed for excellent performance in the tracking of a QPSK signal under the circumstance of a low energy-per-symbol to noise

spectral density ratio, E_s/N_0 . A QPSK carrier loop that is motivated by Maximum *A Posteriori* (MAP) estimation of carrier phase is described in [3]. The Block-V Receiver QPSK carrier loop is an approximate implementation of the MAP QPSK carrier loop for the case of low E_s/N_0 . There is a four-fold phase ambiguity associated with this carrier loop. Within the Block-V Receiver, this QPSK carrier loop is modified for operation as an offset QPSK loop by switching in a delay element. This modified loop, the (low E_s/N_0) MAP QPSK carrier loop with added delay element, is shown in Figure 1. The T second delay in the signal processing of the signal V is the added element that makes this carrier loop suitable for offset QPSK. Unfortunately, since the loop of Figure 1 is a simple modification of a QPSK carrier loop, it retains the four-fold phase ambiguity. However, as this paper will show, by adding some elementary signal processing to both the transmitter and the receiver, it is possible to reduce this four-fold phase ambiguity to two-fold. The phase ambiguity can then be resolved in the same way as is done for BPSK.

It is important to comment that although the E_s/N_0 may be low, as it typically is for deep space telemetry employing an advanced error-correction code, the carrier loop Signal-to-Noise Ratio (SNR) is not necessarily low. It is anticipated that offset QPSK will only be used for bit rates that are high (by the standards of deep space telemetry), 2 Mbps or more. E_s/N_0 is given by

$$\frac{E_s}{N_0} = \frac{PT}{N_0} \quad (1)$$

where P is the received signal power, T is the binary symbol period (the period of the coded bits emerging from the encoder), and N_0 is the one-sided noise spectral density. On the other hand, the carrier loop SNR is given by

$$\begin{aligned} \text{Carrier Loop SNR} &= \frac{PS_L}{N_0B} \\ &= \frac{E_s}{N_0} \cdot \frac{S_L}{BT} \end{aligned} \quad (2)$$

where B is the carrier loop bandwidth and S_L is a “squaring loss”. The carrier loop bandwidth is selectable in the Block-V Receiver but is typically about 1 Hz. So for bit rates of 2 Mbps or more, BT will be a very small number. As is clear from Eq. (2), the carrier loop SNR will be quite large even while E_s/N_0 is small. For bit rates of 2 Mbps or more, the carrier loop SNR will ordinarily be more than adequate. SNR will not be a further concern in this paper.

2. OFFSET QPSK CARRIER LOOP

A block diagram of the offset QPSK carrier loop in the Block-V Receiver appears in Figure 1. The front-end of the receiver is not shown. The receiver front-end includes amplification of the received carrier and downconversion to an intermediate frequency. Then follows analog-to-digital

conversion. Figure 1 shows what comes next. The received signal is multiplied by a sinusoid coming from the Numerically-Controlled Oscillator (NCO). In parallel, this same received signal is multiplied by a version of the NCO sinusoid that has been delayed in phase by 90° . The output of the multiplication involving the undelayed NCO sinusoid is delayed by T seconds and then accumulated over one quaternary symbol period ($2T$); this result is called V . The output of the multiplication involving the delayed NCO sinusoid is accumulated (without further delay); this result is called U . The V and U accumulators report their sums once each $2T$ seconds, and these accumulators are reset after each report so that the next sum starts at 0. In other words, accumulators V and U implement the integrate-and-dump function in discrete-time. The carrier loop error signal is generated from V and U .

It is also necessary to synchronize to the quaternary symbols. The V and U accumulators report values and initiate new sums at epochs defined by a clock signal provided by the symbol synchronizer. (The signal paths for this clock signal are not shown in Figure 1.) The symbol synchronizer, like the carrier loop, works on the basis of closed-loop control. The symbol synchronizer takes its input from both the input and output of the U accumulator, and it tracks the quaternary symbol timing. In this way, the carrier and symbol synchronization loops are coupled so that the dynamics of one affect the other.

It is important to know the conditions under which the carrier loop achieves phase lock. Any analysis must begin with an assumption about the form of signals V and U . The initial assumption here is that V and U are of the following form.

$$V = d_{2k} \cos \phi + \frac{1}{2} (d_{2k-1} + d_{2k+1}) \sin \phi + n_{2k} \quad (3)$$

$$U = -\frac{1}{2} (d_{2k} + d_{2k+2}) \sin \phi + d_{2k+1} \cos \phi + n_{2k+1} \quad (4)$$

Eqs. (3) and (4) collectively are called “Model 1” in this paper. The phase ϕ is the difference between the phase of the received carrier and the phase of the (undelayed) NCO sinusoid. The bits are denoted $\{\dots, d_{2k-2}, d_{2k-1}, d_{2k}, d_{2k+1}, d_{2k+2}, \dots\}$, where $d_j = \pm 1$. The noise components n_j have zero mean and are Gaussian. Moreover, each noise component is uncorrelated with every other. This is a consequence of the fact that the receiver noise may be modeled, to an excellent approximation, as white. A few remarks about the reasonableness of this model are in order. In offset QPSK, as in QPSK, the individual bit persists for one quaternary period, $2T$. Whenever the symbol synchronizer is locked to the quaternary symbol timing, the V and U accumulation windows will coincide with some bit boundaries and will be centered on the boundaries of others (the offset bits). Thus, for example, in Eq. (3) the V accumulation window coincides with the even-indexed bits (d_{2k}) and is centered on the boundary between two adjacent odd-indexed bits (d_{2k-1} and d_{2k+1}). Furthermore, because

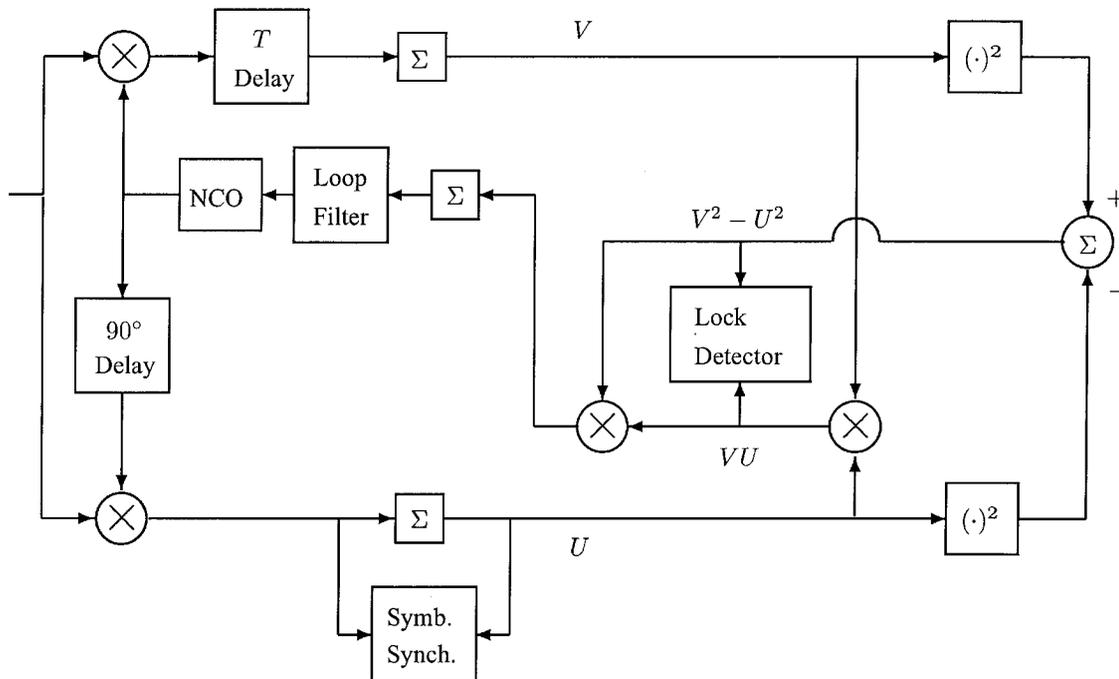


Figure 1: Offset QPSK carrier loop for the Block-V Receiver

the input to the V accumulator is delayed by T seconds, the bits in Eq. (3) are delayed by T seconds (one-half of a quaternary symbol period) relative to those of Eq. (4). With respect to carrier phase, U is advanced in phase by $\pi/2$ relative to V . This can be explained as follows. The local oscillator used in generating U is delayed in phase by 90° . Therefore, the phase difference between the received carrier and the delayed NCO sinusoid is $\phi + \pi/2$. It should be noted that $-\sin \phi = \cos(\phi + \pi/2)$ and $\cos \phi = \sin(\phi + \pi/2)$. Model 1, as represented by Eqs. (3) and (4), is not the only model that must be considered here.

Another set of equations that satisfy all the above-mentioned reasonableness criteria follow.

$$V = \frac{1}{2} (d_{2k-2} + d_{2k}) \cos \phi + d_{2k-1} \sin \phi + n_{2k-1} \quad (5)$$

$$U = -d_{2k} \sin \phi + \frac{1}{2} (d_{2k-1} + d_{2k+1}) \cos \phi + n_{2k} \quad (6)$$

Eqs. (5) and (6) collectively are called "Model 2" in this paper. As before, the noise components n_j are zero-mean, Gaussian random variables and are uncorrelated, one with another.

The analysis begins with the model of Eqs. (3) and (4). The carrier loop computes $VU(V^2 - U^2)$ once every $2T$ seconds. This result is then accumulated. The loop error signal is proportional to the expected value of $VU(V^2 - U^2)$. This expected value is here denoted $\epsilon(\phi)$.

$$\epsilon(\phi) = E \{ VU(V^2 - U^2) \} \quad (7)$$

If each bit d_j is equally likely to be $+1$ or -1 and if each bit is uncorrelated with every other, then

$$\epsilon(\phi) = 2 \cos^3 \phi \sin \phi - \cos \phi \sin^3 \phi \quad \text{Model 1} \quad (8)$$

As mentioned above, the loop error signal is proportional to $\epsilon(\phi)$. In this paper, values of ϕ corresponding to stable lock points are of interest. If the loop bandwidth or the loop transient response were being calculated, then it would be necessary to keep track of all multiplicative factors. In that case, it would be necessary to know what the loop error signal *equals*, not just that it is *proportional to* $\epsilon(\phi)$.

The positive-going zero crossings of $\epsilon(\phi)$ are the stable lock points. Figure 2 plots the $\epsilon(\phi)$ of Eq. (8) as the solid curve labeled "1", where the label serves as a reminder that this is the $\epsilon(\phi)$ derived from the first model for V and U , that of Eqs. (3) and (4). In each cycle of carrier phase, there are four stable lock points: $\phi = 0, \pi/2, \pi,$ and $3\pi/2$. The substitution of $\phi = 0$ into Eqs. (3) and (4) gives

$$\phi = 0 : V = d_{2k} + n_{2k} \ \& \ U = d_{2k+1} + n_{2k+1} \quad (9)$$

The substitution of $\phi = \pi$ into Eqs. (3) and (4) gives

$$\phi = \pi : V = -d_{2k} + n_{2k} \ \& \ U = -d_{2k+1} + n_{2k+1} \quad (10)$$

These are legitimate solutions. However, if $\pi/2$ or $3\pi/2$ is substituted for ϕ in Eqs. (3) and (4), the results are inconsistent with the known tracking characteristics of the symbol synchronizer. For example, the substitution $\phi = 3\pi/2$ in Eq. (4) gives $U = (d_{2k} + d_{2k+2})/2 + n_{2k+1}$, and this falsely

suggests that the symbol synchronizer window is offset from proper alignment by one-half of a quaternary symbol. This really means that the first model for V and U , that of Eqs. (3) and (4), is inappropriate for the lock points $\phi = \pi/2$ and $3\pi/2$.

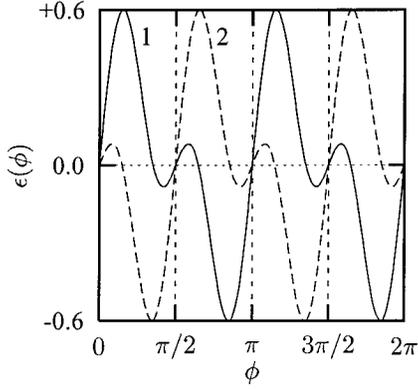


Figure 2: $\epsilon(\phi)$

The second model for V and U is now explored. It is anticipated that Eqs. (5) and (6) are appropriate for the lock points $\phi = \pi/2$ and $3\pi/2$. For this second model,

$$\epsilon(\phi) = \frac{1}{2} \cos^3 \phi \sin \phi - 2 \cos \phi \sin^3 \phi \quad \text{Model 2} \quad (11)$$

Figure 2 plots the $\epsilon(\phi)$ of Eq. (11) as the dashed curve labeled “2”, where the label serves as a reminder that this is the $\epsilon(\phi)$ derived from the second model for V and U , that of Eqs. (5) and (6). As before, the stable lock points are $\phi = 0, \pi/2, \pi,$ and $3\pi/2$. Of these, $\phi = \pi/2$ and $3\pi/2$ are consistent with the tracking characteristics of the symbol synchronizer. It is concluded that

$$\phi = \pi/2: V = d_{2k-1} + n_{2k-1} \ \& \ U = -d_{2k} + n_{2k} \quad (12)$$

$$\phi = 3\pi/2: V = -d_{2k-1} + n_{2k-1} \ \& \ U = d_{2k} + n_{2k} \quad (13)$$

There are four stable lock points in each cycle of carrier phase. These lock points and the resulting signals V and U are given in Eqs. (9), (10), (12), and (13). In the case $\phi = 0$, the even-indexed bits appear at V and the odd-indexed bits appear at U . In the case $\phi = \pi$, the bits appear in the same place as with the previous case, but are inverted. In the case $\phi = \pi/2$, the odd-indexed bits appear at V and the even-indexed bits appear inverted at U . In the case $\phi = 3\pi/2$, the odd-indexed bits appear inverted at V and the even-indexed bits appear at U . This four-fold phase ambiguity must somehow be resolved. This issue is treated in the next section.

The lock detector of Figure 3 is appropriate for the (nonoffset) QPSK carrier loop [4] of the Block-V Receiver. It is also used with the offset QPSK carrier loop of Figure 1. The lock

detector signal is an accumulation of

$$(V^2 - U^2 + 2VU)(V^2 - U^2 - 2VU).$$

The lock detector signal is proportional to

$$\Lambda(\phi) = E \{ (V^2 - U^2 + 2VU)(V^2 - U^2 - 2VU) \} \quad (14)$$

As before, it is assumed that each bit d_j is equally likely to be +1 or -1 and that each bit is uncorrelated with every other. For lock points $\phi = 0$ and π , Eq. (14) is evaluated with the expressions for V and U from Eqs. (3) and (4), and the result is

$$\Lambda(\phi) = -\frac{1}{2} \sin^4 \phi - 4 \cos^4 \phi + 6 \cos^2 \phi \sin^2 \phi \quad (15)$$

For lock points $\phi = \pi/2$ and $3\pi/2$, Eq. (14) is evaluated with the expressions for V and U from Eqs. (5) and (6), and the result is

$$\Lambda(\phi) = -\frac{1}{2} \cos^4 \phi - 4 \sin^4 \phi + 6 \cos^2 \phi \sin^2 \phi \quad (16)$$

The $\Lambda(\phi)$ of Eq. (15) and the $\Lambda(\phi)$ of Eq. (16) are plotted in Figure 4 as the curves labeled “1” (solid) and “2” (dashed), respectively. The first of these curves shows that a large absolute value is obtained at lock points $\phi = 0$ and π . The second of these curves shows that a large absolute value is obtained at lock points $\phi = \pi/2$ and $3\pi/2$. Although the lock detector of Figure 3 was originally designed for use with the (non-offset) QPSK carrier loop, it is clear that it will also work in conjunction with the offset QPSK carrier loop of Figure 1.

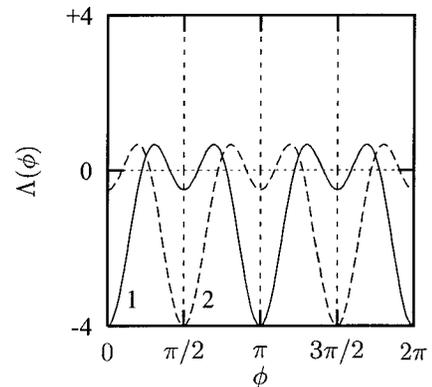


Figure 4: $\Lambda(\phi)$

3. PHASE AMBIGUITY RESOLUTION

The offset QPSK carrier loop of Figure 1, which has been incorporated into the Block-V Receiver, has a four-fold phase ambiguity. Methods have been reported in the literature for resolving this four-fold ambiguity.[5] Another method is proposed here. The idea is to first reduce the four-fold phase

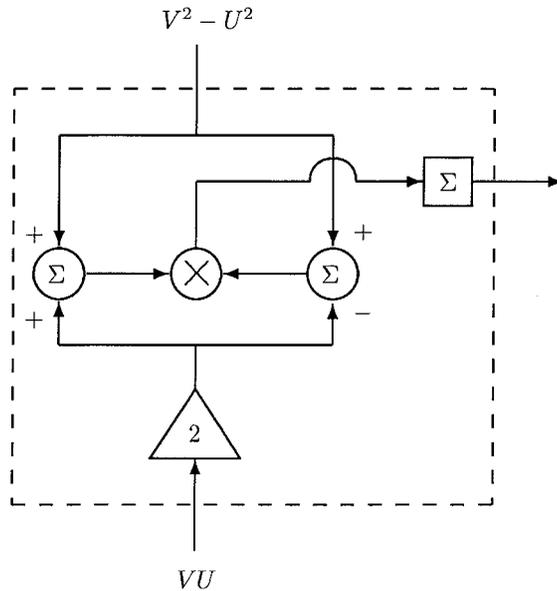


Figure 3: Lock detector

ambiguity to a two-fold phase ambiguity. A two-fold phase ambiguity also occurs with BPSK signaling (with suppressed carrier). In the tracking of deep space BPSK signals, such two-fold phase ambiguities are routinely handled by unique word detection. In order to reduce from four-fold to two-fold the phase ambiguity of the Figure 1 carrier loop, it is necessary to introduce new signal processing functions in the transmitter as well as in the receiver.

Figure 5 shows a typical offset QPSK modulator along with the new signal processing needed to assist the reduction of phase ambiguity. The new signal processing at the transmitter is placed just before the offset QPSK modulator. (It should be noted that signal flow is from right to left in Figure 5.) In this paper, the new transmitter function will be termed *transmitter periodic inversions*. This new function takes the incoming bit stream destined for the offset QPSK modulator and partitions it into groups of four bits. The last two bits of every group of four are inverted. Thus, in the example shown in Figure 5, $d_0 d_1 d_2 d_3$ becomes $d_0 d_1 \bar{d}_2 \bar{d}_3$. In this analysis, $d_j = \pm 1$, so an inverted bit could also be written $\bar{d}_j = -d_j$. Because the modulator considered here is for offset QPSK, the bits on one output (the lower) of the demultiplexer are delayed by T seconds, which is one-half of a quaternary symbol period, relative to the other (upper) output of the demultiplexer. This delay is not explicitly shown in Figure 5.

Figure 6 shows the signal processing that must be appended to the demodulator. In this paper, this new receiver signal processing function will be termed *receiver periodic inversions*. This new function operates on the V and U coming out of the offset carrier loop of Figure 1. The discrete-time signals at V and U are clocked once per $2T$ seconds, and

the clock for U is offset by T seconds relative to that for V . Each discrete-time signal, at either V or U , is a soft symbol representing a data bit or an inverted data bit as observed in the presence of noise. Whether a given data bit (say, d_0 , for example) appears at V or at U and whether or not it is inverted depends on the lock point of the carrier loop. As explained in the previous section, there are four possibilities here. The four diagrams of Figure 6 show these four possible cases. From top to bottom in Figure 6, the identities of the soft symbols at V and U are illustrated for lock points $\phi = 0, \pi, \pi/2$, and $3\pi/2$. In truth, the soft symbols include noise, as indicated by Eqs. (9), (10), (12), and (13). The noise is not shown in Figure 6 because it would clutter the diagram and distract the reader from the focus of this section, the resolution of the four-fold phase ambiguity.

The operation performed by the receiver periodic inversions block is described here. This block does one of two things to every soft symbol. The soft symbol is either negated or the soft symbol is passed along without change. A negation of a soft symbol has the effect, of course, of inverting the data bit. An algorithm determines which soft symbols are negated and which aren't. With each soft symbol appearing at U , the same thing is done as for the immediately preceding soft symbol at V . For example, if the immediately preceding soft symbol at V was negated, then the new soft symbol at U is also negated. With each soft symbol appearing at V , the operation that is applied to the new soft symbol is the *opposite* of that which was applied to the immediately preceding soft symbol at U . If the immediately preceding soft symbol at U was negated, then the new soft symbol at V is not. But if the immediately preceding soft symbol at U was passed without change, then the new soft symbol at V

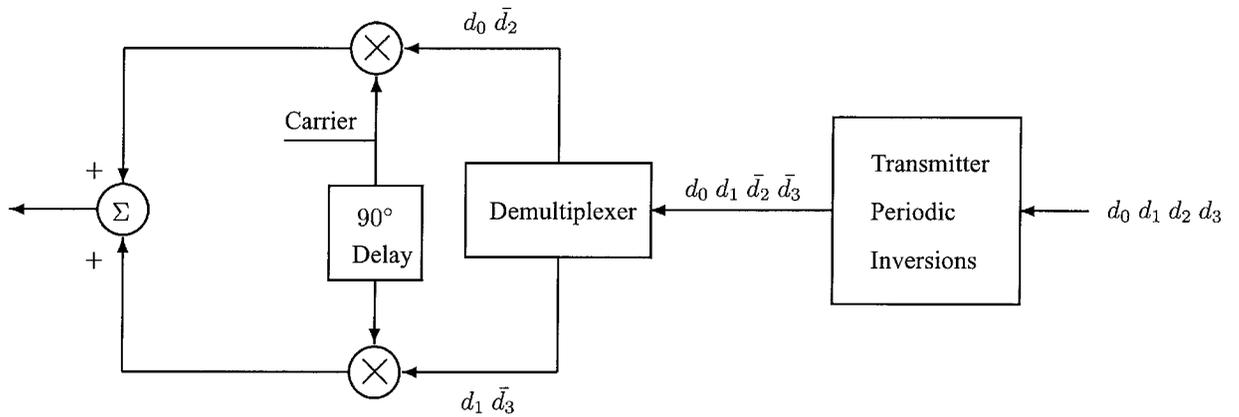


Figure 5: Offset QPSK modulator with periodic inversions

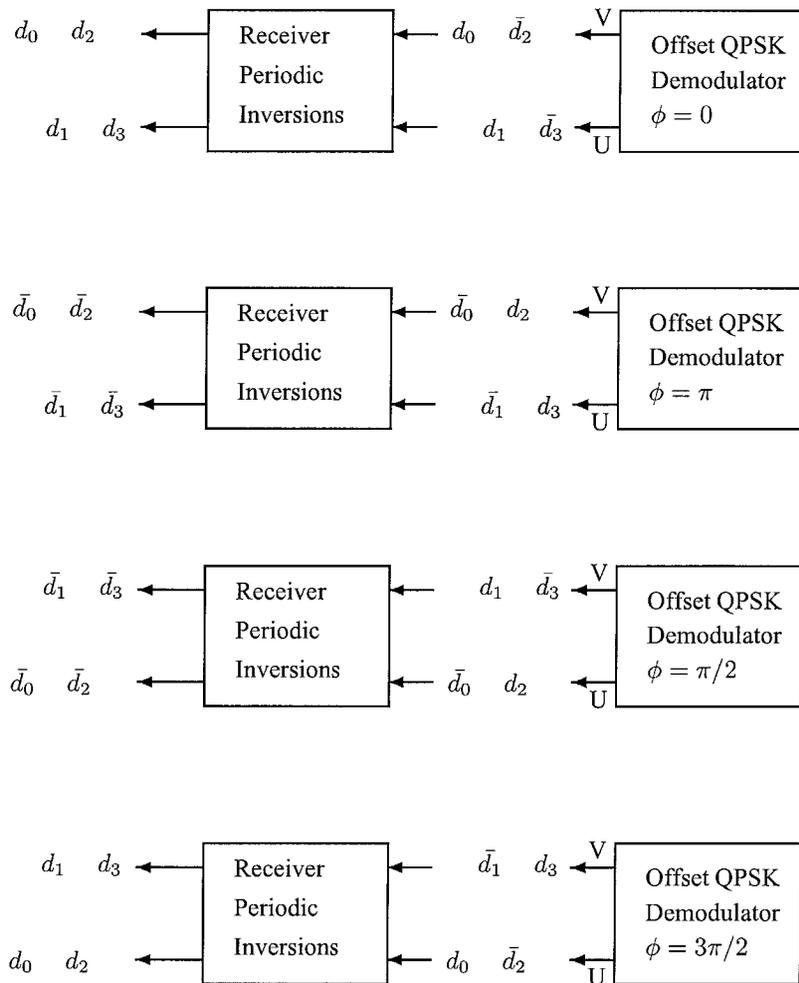


Figure 6: Offset QPSK demodulator with periodic inversions

is negated. The receiver periodic inversions block described here is easily implemented in hardware.

The reader may note a similarity between the transmitter periodic inversions and the receiver periodic inversions. Both invert two consecutive bits and then pass unchanged the next two consecutive bits. The reader may suspect that the receiver periodic inversions function is the reciprocal operation to the transmitter periodic inversions function. But this is not so! If it were, nothing would be accomplished: the four-fold phase ambiguity would remain. Referring to Figure 5, in the group of four bits $\{d_0, d_1, d_2, d_3\}$, the transmitter periodic inversions block inverts d_2 and d_3 . The first in the pair of inverted bits is even-indexed. At the receiver, on the other hand, the first of the pair of bits that will be inverted may be even-indexed or odd-indexed; it depends on the lock point of the carrier loop. In other words, the receiver periodic inversions block will not, in general, invert the same pair of bits that were inverted at the transmitter.

The situation for the lock point $\phi = 0$ is shown in the top diagram of Figure 6. The bits d_2 and d_3 are inverted at V and U because they were inverted by the transmitter periodic inversions block (see Figure 5) and because no further inversions occur in the demodulator for the lock point $\phi = 0$. It is assumed here that the receiver periodic inversions block does not invert d_0 , which appears at V . Then d_1 at U will not be inverted either. When \bar{d}_2 appears at V , it will be inverted, because d_1 was not. Finally, \bar{d}_3 will also be inverted. This has the effect of putting d_2 and d_3 right. (In binary logic, two wrongs do indeed make a right!). The net result, at the output of the receiver periodic inversions block, is that all bits are right. In this special case ($\phi = 0$ and d_0 not inverted), the receiver periodic inversions block does undo the inversions from the transmitter. But this is not true in general. By the very nature of offset QPSK, the lower soft symbols are delayed one-half of a quaternary symbol period relative to the upper soft symbols. Thus, the soft symbols are easily multiplexed into proper order. (This multiplexing is not shown in Figure 6.) It is worth asking what happens if the assumption about d_0 is reversed. What is the result if d_0 is inverted? Then, the output of the receiver periodic inversions block, after multiplexing, would be $\{\bar{d}_0, \bar{d}_1, \bar{d}_2, \bar{d}_3\}$. This is a legitimate answer. With lock point $\phi = 0$, it is in practice not possible to predict whether the bits will come out all right or all inverted. But this is consistent with a two-fold phase ambiguity, which is easily handled in practice.

When the lock point is $\phi = \pi$, as shown in the second diagram of Figure 6, the demodulator inverts d_0, d_1, \bar{d}_2 , and \bar{d}_3 ; but this has the effect of putting d_2 and d_3 right. If it is assumed that the receiver periodic inversions block does not invert \bar{d}_0 , then it also won't invert \bar{d}_1 , but it will invert d_2 and d_3 . The net result is that all bits are inverted. If, instead, it had been assumed that the receiver periodic inversions block does invert \bar{d}_0 , then the net result would have been that all bits are right. This is the same two-fold phase ambiguity as before.

When the lock point is $\phi = \pi/2$, as shown in the third diagram of Figure 6, the odd-indexed bits appear at V and the even at U , and the demodulator inverts d_0 and \bar{d}_2 . If it is assumed that the receiver periodic inversions block does not invert \bar{d}_0 , then it will invert d_1 and d_2 , but not \bar{d}_3 . The net result is that all bits are inverted. If, instead, it had been assumed that the receiver periodic inversions block does invert \bar{d}_0 , then the net result would have been that all bits are right.

When the lock point is $\phi = 3\pi/2$, as shown in the fourth diagram of Figure 6, the odd-indexed bits appear at V and the even at U , and the demodulator inverts d_1 and \bar{d}_3 . If it is assumed that the receiver periodic inversions block does not invert d_0 , then it will invert \bar{d}_1 and \bar{d}_2 , but not d_3 . The net result is that all bits are right. If, instead, it had been assumed that the receiver periodic inversions block does invert d_0 , then the net result would have been that all bits are inverted.

As Figure 6 and the preceding discussion demonstrate, there are only two possible outcomes for the carrier loop of Figure 1 with transmitter and receiver periodic inversions. There outcomes are:

$$\{d_0, d_1, d_2, d_3\}$$

and

$$\{\bar{d}_0, \bar{d}_1, \bar{d}_2, \bar{d}_3\}$$

That is to say, only a two-fold phase ambiguity remains.

The reduction of a four-fold phase ambiguity to a two-fold ambiguity by means of periodic bit inversions is not without precedent. But the authors of this paper have not seen this possibility discussed in the present context, so it was deemed worthy of presentation here. It must be said, though, that essentially the same technique for reducing the order of a phase ambiguity is used in Minimum-Shift Keying (MSK). A brief review of MSK follows.

The term MSK has several different meanings in the literature. Here the term is used in the same sense that it was used by those who coined the expression "Minimum-Shift Keying". The reader is warned, however, that many textbooks and papers define a related, but not identical, digital modulation scheme as MSK. For the purpose of this paper, MSK means binary Continuous Phase Frequency-Shift Keying (CPFSK) with a modulation index of $1/2$. The modulation index, usually denoted h , is defined for CPFSK as the dimensionless product of the bit period T and the spacing between the two signaling frequencies. This modulation scheme is called "Minimum-Shift Keying" because the spacing between the two signaling frequencies is, for $h = 1/2$, the smallest possible spacing that results in orthogonality for the $+1$ and -1 signals in a coherent detector. If CPFSK is used with $h < 1/2$, then better bandwidth efficiency is achieved, of course, but the loss of orthogonality means that power efficiency is lost. For this reason, MSK is a popular solution

when both bandwidth and power efficiency are of concern.

There is another way of describing MSK that is mathematically equivalent to the above.[6] MSK may be regarded as a modified form of offset QPSK. There are three modifications to offset QPSK:

1. A binary differential encoder precedes the modulator.
2. A transmitter periodic inversions block follows the binary differential encoder and precedes the modulator.
3. Half-sinusoid pulse amplitude shapes replace rectangular pulses.

The second modification above is exactly the same one that is proposed in this paper for offset QPSK. This second modification, together with receiver periodic inversions at the demodulator, makes it easy to reduce a four-fold phase ambiguity to a two-fold phase ambiguity. The binary differential encoder enables the resolution of the two-fold phase ambiguity. (It should be noted that a binary differential encoder cannot help resolve a four-fold phase ambiguity.) The half-sinusoid pulse amplitude shapes produce a faster roll-off of sideband power spectral density. MSK is of interest for several reasons. It effects a nice compromise between bandwidth efficiency and power efficiency. From a theoretical point-of-view, MSK represents the intersection of the CPFSK family of digital modulation schemes with the PSK (with shaped pulses) family of modulation schemes. Most important for the issues discussed in the present paper, MSK is an example of the use of periodic inversions for the reduction of phase ambiguity.

4. ALTERNATE LOOP DESIGN

An offset QPSK carrier loop that is motivated by MAP estimation of offset QPSK carrier phase is described in [7]. A low E_s/N_0 implementation of the MAP loop is also described there. Although this is not the loop used by the Block-V Receiver, it is instructive to consider this alternative. A discrete-time version of the low E_s/N_0 implementation of the MAP loop is shown in Figure 7. There are four accumulators producing the signals A , B , C and D that are used to generate the loop error signal. It is assumed here that the input and output of the B accumulator are used by the symbol synchronizer, although other configurations are possible. The A , B , C and D accumulators all receive a clock signal from the symbol synchronizer, but these clock signal paths are not shown. The outputs of the signal accumulators are taken to be of the following form.

$$A = \frac{1}{2} (d_{2k-2} + d_{2k}) \cos \phi + d_{2k-1} \sin \phi + n_{2k-1} \quad (17)$$

$$B = d_{2k} \cos \phi + \frac{1}{2} (d_{2k-1} + d_{2k+1}) \sin \phi + n_{2k} \quad (18)$$

$$C = -d_{2k} \sin \phi + \frac{1}{2} (d_{2k-1} + d_{2k+1}) \cos \phi + n'_{2k} \quad (19)$$

$$D = -\frac{1}{2} (d_{2k-2} + d_{2k}) \sin \phi + d_{2k-1} \cos \phi + n'_{2k-1} \quad (20)$$

The noise components n_j and n'_i are zero-mean, Gaussian random variables. Each random variable n_j is uncorrelated with every random variable n'_i . (On the other hand, the random variables n_{2k-1} and n_{2k} are correlated. Also, the random variables n'_{2k-1} and n'_{2k} are correlated. But these facts do not affect the search for stable lock points.) The carrier loop computes $AD - BC$ once every $2T$ seconds. The loop error signal is an accumulation of $AD - BC$; it is proportional to the expected value of $AD - BC$. If each bit d_j is equally likely to be $+1$ or -1 and if each bit is uncorrelated with every other, then

$$\begin{aligned} \epsilon(\phi) &= E\{AD - BC\} \\ &= \cos \phi \sin \phi \\ &= \frac{1}{2} \sin 2\phi \end{aligned} \quad (21)$$

Since stable lock points occur at positive-going zero crossings of $\epsilon(\phi)$, it is clear from Eq. (21) that there are only two stable lock points, $\phi = 0$ and π , for each cycle of carrier phase.

$$\phi = 0 : B = d_{2k} + n_{2k} \ \& \ D = d_{2k-1} + n_{2k-1} \quad (22)$$

$$\phi = \pi : B = -d_{2k} + n_{2k} \ \& \ D = -d_{2k-1} + n_{2k-1} \quad (23)$$

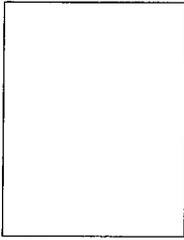
With this MAP loop for offset QPSK, there exists only a two-fold phase ambiguity. Furthermore, this is achieved without the need for anything like periodic inversions at the transmitter. A complete noise analysis of this MAP loop for offset QPSK is given in [7], where it is shown that this loop has better performance in the presence of noise than the loop of Figure 1. The offset QPSK loop of Figure 7 will be an attractive design choice for future receivers.

5. CONCLUSIONS

The Block-V Receiver can track offset QPSK with a synchronization loop that is a modification of its QPSK carrier loop. The QPSK loop is modified by the addition of a delay (of one-half of a quaternary symbol period) after one of the coherent detectors. This offset QPSK loop is shown in Figure 1. The resulting loop tracks offset QPSK with a four-fold phase ambiguity. This four-fold phase ambiguity may be reduced to a two-fold ambiguity by the addition of simple signal processing functions at both the transmitter and the receiver. This is of some importance, as it allows a uniform method of dealing with phase ambiguities from offset QPSK and BPSK.

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