ABSTRACT

An FPGA based test bench for non-volatile memory testing

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A test bench is developed for testing memory chips from various non-volatile memory technologies, using a XILINX XC4010E (10,000 gate) FPGA. The test bench is being used to perform the endurance and reliability testing. A MATS + memory test, which can detect address decoder faults and stuck-at faults and cycles through all the addresses in the memory, was chosen for reliability testing. For endurance testing, specific data patterns are written to and read from the same address range of the memory continuously, which allows for faster endurance testing, especially when slower memory technologies are used. The error data logged upon each error includes the error number, the address at which the error occurred, the cycle number (where one cycle is defined as one read and write operation to a single address), the incorrect data value read, and (for the MATS+ test) which portion of the test the error occurred on. The error data can either be logged on a PC through the parallel port, or the tester can be used by itself independent of a PC by using an EEPROM to load the bit stream file and displaying the error information on a 7-segment LED. This test bench offers several advantages over commercial testers when used for reliability and endurance testing. Endurance testing to a chip's specifications could involve more than 10^{10} read/write cycles, which can take up to 28 days for the Ramtron FM24C04 serial FRAM. Commercially available memory testers with high hourly rates may prove extremely expensive for testing NVMs with 10^{12} to 10^{15} read/write cycles. In comparison, the FPGA-based testers are inexpensive and more flexible. If several FPGA boards are used, many chips can be tested simultaneously at a fraction of the cost compared to the commercial testers.

Tests to date have shown no errors in the endurance test after reaching three times the endurance specifications of the RAMTRON FM24C04 serial FRAM ($3x10^{10}$ read/write cycles). Reliability testing has shown no errors either to date. Tests are underway on the RAMTRON FM1808 Parallel FRAM and the Northrop-Grumman's 256k Rad-Hard EEPROM. Extensive data with analysis will be presented in this paper.