Europa Orbiter/X2000 Avionics
Industry Briefing

Europa/X2000 Avionics Overview

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Key Technologies/Driving Requirements

- Next generation spacecraft microprocessor technology
- Open architecture for advanced spacecraft systems based on commercial interfaces
- Advanced digital ASIC technology (SOI, HX3000, 1 M gates)
- Low voltage, low power system architectures
- Advanced power management and control
- Next generation Power Activation and Switching Module (PASM)
- Advanced high efficiency power converter
- Advanced mixed signal ASIC technology (SOI, HX2000)
- 1 Mrad radiation requirement
- New, low-cost approach to avionics system development using commercial IP
- Initiating first step towards System on a Chip for future missions
- Fault tolerant tree topology using IEEE-1394a (Firewire) bus
- Low power, fault tolerant I²C serial bus
- compactPCI 3U form factor packaging approach
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SFC - System Flight Computer
* PowerPC 750Compact PCI based
* 128 Mbytes DRAM; 256Kbytes EEPROM
* Baseline 240 MIPS; variable speed
* Contractor: BAE Systems

SIO - System Input/Output
* PCI/1394/I²C Bridge; 2 UARTs
* Includes node reset control; general fault protection logic; discretes
* Assembly developed by JPL

NVM - Non Volatile Memory
* 2 Gbit/slice Flash Memory
* Includes power management control and erase/write cycle tally
* Contractor: SEAKR Engineering, Inc.

SIA - System Interface Assembly
* Includes 1553, SPI and high speed serial interfaces
* Assembly developed by JPL

TIF - Tzero Interface
* Contains critical safety relays controlled from LCE
* Tzero/LV interface circuits
* Assembly developed by JPL

PCA - Power Converter Assembly
* Two 30 W primary to secondary Power Converter Modules (PCMs) on 1 slice
* Two versions: dual 3.3V PCMs or one 3.3V and one 5V PCM
* Contractor: Lockheed Martin CSS

PSS - Power Switch Slice
* Used to switch power loads, valves and pyros (all three functions)
* 16 switches/slice
* Redundant PC bus
* Contractor: Lockheed Martin CSS

PCS - Power Control Slice
* Primary spacecraft power bus regulation
* Includes shunt regulator control
* Redundant PC bus
* Contractor: Lockheed Martin CSS

TAS - TRIO Assembly Slice
* Temperature and analog collection
* 6 Temperature Remote I/O (TRIO) ASICs split between 2 PCI buses
* 96 telemetry channels; 10 bit A/D
* Contractor: Johns Hopkins University/Applied Physics Laboratory

X2000 Avionics Hardware

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EO ACS/Avionics Functional Block Diagram

SRU
IMU
LV
STAR 48
SSA
SSE
PSS PDE
TIF
SFC
SIA

PSS VDE
TAS
TVC
RWE
RWM

Main Engine
MITs
RCS Engines
ALR
Main tank Pres xducer
STAR 48 Pres xducer

On time cmds
ALR step cmds
ALR step tim
Tank pres tim
Pres tim

LV Sep Signal
STAR Sep Sig

Axis tim
Gain sw
LV Sep Signal
STAR Sep Sig

Gimbal posn cmds
Posn/pressure tim

Anlg dry
LVDT posn tim

Drive cmds
Wheel speed

key
I2C --- 1553 --- analog
RS422 ---

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## Command & Data Handling Subsystem ASICs

<table>
<thead>
<tr>
<th>ASIC</th>
<th>Function</th>
<th>Slice</th>
<th>Designed By</th>
<th>Proc By</th>
<th>Fab By</th>
<th>FIB Line Type</th>
<th>Gate Count</th>
<th>Pin Count</th>
<th>Status</th>
</tr>
</thead>
<tbody>
<tr>
<td>1  Power PCI Bridge Chip</td>
<td>Bridge between the Compact PCI (cPCI) bus, memory (EEPROM, SDRAM) and the RAD750 processor. Includes UART and JTAG interfaces for software support and diagnostics.</td>
<td>SFC</td>
<td>BAE</td>
<td>BAE</td>
<td>BAE</td>
<td>Digital</td>
<td>700K</td>
<td>624</td>
<td>First fab run completed. Parts installed on EM SFCs currently going through qualification. (Enhanced Bridge Chip = 200 Krad)</td>
</tr>
<tr>
<td>2  RAD750</td>
<td>Rad hard version of the PowerPC 750 processor.</td>
<td>SFC</td>
<td>BAE</td>
<td>BAE</td>
<td>BAE</td>
<td>Digital</td>
<td>10M</td>
<td>360</td>
<td>First fab un completed 5/01. Parts in test.</td>
</tr>
<tr>
<td>3  DIO (Digital VO)</td>
<td>Bridge between the 1394/fC buses and the cPCI bus. Implements the link layer of the 1394 bus, the two fC bus controllers, and logic for fault tolerance enhancements. Includes a UART to support software development and discrete VO signals for miscella</td>
<td>SIO</td>
<td>JPL + Mentor/ISI</td>
<td>JPL</td>
<td>Honeywell SSEC</td>
<td>Gate Array HX311G</td>
<td>170K gates + 250K RAM</td>
<td>220 Sig 100 Per</td>
<td>FPGA version in checkout. PDR date: 6/27/01</td>
</tr>
<tr>
<td>4  MSIO (Mixed Signal VO)</td>
<td>Implements the physical layer of the 1394 bus and the drivers of the fC buses.</td>
<td>SIO</td>
<td>SSEC/DMC + Mentor/ISI + JPL</td>
<td>JPL</td>
<td>Honeywell SSEC</td>
<td>Mixed Signal HX2300</td>
<td>50K gates + analog 1394 if/i</td>
<td>200 Sig 150 Per</td>
<td>CDR completed 5/18/01</td>
</tr>
<tr>
<td>5  SIA (System Interface ASIC)</td>
<td>Provides interface between the cPCI bus, the 1553 bus controller ASIC, buffer memory (SRAM), SDST (RS422) and 4 high speed serial interfaces (instruments/sensors).</td>
<td>SIA</td>
<td>JPL + Aegard ASIC</td>
<td>JPL</td>
<td>Honeywell SSEC</td>
<td>Digital HX311G</td>
<td>-</td>
<td>FPGA version in checkout. PDR date: 11/01</td>
<td></td>
</tr>
<tr>
<td>6  Memory Controller ASIC</td>
<td>Interface between cPCI bus and memory (flash), includes Reed Solomon EDAC and flash power control.</td>
<td>NVM</td>
<td>SEAKR</td>
<td>SEAKR</td>
<td>Honeywell SSEC</td>
<td>Digital HX2160</td>
<td>-70K</td>
<td>ASIC in fabrication. POGs received 5/30 and in checkout. (300 Krad)</td>
<td></td>
</tr>
<tr>
<td>7  TRIO (Temperature Remote VO)</td>
<td>Includes 16 analog inputs for temperature or voltage measurement, 10 bit ADC and I2C interface.</td>
<td>TAS</td>
<td>APL</td>
<td>APL</td>
<td>Honeywell SSEC</td>
<td>Custom RICMOS4</td>
<td>-46K</td>
<td>84</td>
<td>ASIC in fabrication. EM parts due: 8/01</td>
</tr>
</tbody>
</table>

**NOTES:**
- All ASICs are 1 Mrad except as noted.
- ASICs to be fabricated via the JPL Multilab Contract.
# Europa Orbiter/X2000 Avionics

## Industry Briefing

### Power Subsystem ASICs

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<tr>
<td>SCAH (Switch Control ASIC High)</td>
<td>Provides the floating current limit, overcurrent trip and MOSFET drive function for the power switch inside the PASM.</td>
<td>PSS PCS</td>
<td>Boeing</td>
<td>JPL</td>
<td>Honeywell SSEC</td>
<td>Mixed HX2040</td>
<td>&lt;10K</td>
<td>60</td>
<td>On track for a CDR on 6/28/01. JPL is completing a worst case data base of the analog cells and will complete a formal worst case analysis by 5/31/01.</td>
</tr>
<tr>
<td>SCAL (Switch Control ASIC Low)</td>
<td>Provides the ground referenced command I/F and charge pump for the power switch inside the PASM.</td>
<td>PSS PCS</td>
<td>Boeing</td>
<td>JPL</td>
<td>Honeywell SSEC</td>
<td>Mixed HX2040</td>
<td>&lt;10K</td>
<td>60</td>
<td>On track for a CDR on 6/28/01. JPL is completing a worst case data base of the analog cells and will complete a formal worst case analysis by 5/31/01.</td>
</tr>
<tr>
<td>PWMA (Pulse-Width Modulator ASIC)</td>
<td>Provides pulse width modulation control for a dual forward topology on the primary side of the Power Converter Module (PCM).</td>
<td>PCA</td>
<td>Boeing</td>
<td>JPL</td>
<td>Honeywell SSEC</td>
<td>Mixed HX2080</td>
<td>&lt;10K</td>
<td>128</td>
<td>Completed fabrication of the first pass on 12/15/00. The part is fully functional with the exception of the autozero amplifier. Second pass specification for new MOSFET baseline has been started and detail design will start in June.</td>
</tr>
<tr>
<td>SRCA (Synchronous Rectifier ASIC)</td>
<td>Provides synchronous rectifier drive and output voltage and current sense on the secondary side of the PCM.</td>
<td>PCA</td>
<td>Boeing</td>
<td>JPL</td>
<td>Honeywell SSEC</td>
<td>Mixed HX2040</td>
<td>&lt;10K</td>
<td>60</td>
<td>Completed fabrication of the first pass on 12/15/00. The part is fully functional with the exception of a POR timing issue. The second pass specification for new MOSFET baseline has been started and detail design will start in June.</td>
</tr>
<tr>
<td>AIA (Analog Interface ASIC)</td>
<td>Provides the system I2C bus interface and drops the signal across transformers for isolated interface with the CIA.</td>
<td>PSS PCS</td>
<td>JPL + SSEC</td>
<td>JPL</td>
<td>Honeywell SSEC</td>
<td>Custom HX2040</td>
<td>~20K</td>
<td>33 Sig 20 Grd</td>
<td>Tape out is scheduled for 7/11/01 and will be fabricated with the SCA. Analog cells will be complete by 4/23/01.</td>
</tr>
<tr>
<td>CIA (Command Interface ASIC)</td>
<td>Provides local command and control for the PCS and PSS including A/D conversion.</td>
<td>PSS PCS</td>
<td>JPL + SSEC</td>
<td>JPL</td>
<td>Honeywell SSEC</td>
<td>Mixed HX2000</td>
<td>87K gates + 1Kb RAM + 64Kb ROM</td>
<td>184 Sig 50 Grd</td>
<td>CDR is scheduled for 10/4/01. Analog cell layout, firmware and verilog code will be complete by 6/25/01.</td>
</tr>
</tbody>
</table>

**NOTES:**

- All ASICs 1 Mrad unless otherwise noted
- ASICs to be fabricated via the JPL MultiFab Contract

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Future Status Updates

- Europa Orbiter Project Website:
  http://www.jpl.nasa.gov/europaorbiter/index.htm
- Presentations, status information, hardware specifications will be placed there as available
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<tr>
<td>ACS</td>
<td>Attitude Control Sensors</td>
<td>RTG</td>
<td>Radioisotope Thermoelectric Generator</td>
</tr>
<tr>
<td>AIA</td>
<td>Analog Interface ASIC</td>
<td>RWE</td>
<td>Reaction Wheel Electronics</td>
</tr>
<tr>
<td>CDH</td>
<td>Command and Data Handling</td>
<td>RWM</td>
<td>Reaction Wheel Motor</td>
</tr>
<tr>
<td>CIA</td>
<td>Command Interface ASIC</td>
<td>SCA</td>
<td>Switch Control ASIC</td>
</tr>
<tr>
<td>DIO</td>
<td>Digital I/O ASIC</td>
<td>SCRA</td>
<td>Synchronous Control Rectifier ASIC</td>
</tr>
<tr>
<td>IMU</td>
<td>Inertial Measurement Unit</td>
<td>SDST</td>
<td>Small Deep Space Transponder</td>
</tr>
<tr>
<td>MSIO</td>
<td>Mixed Signal I/O ASIC</td>
<td>SFC</td>
<td>System Flight Computer</td>
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<td>NVM</td>
<td>Non Volatile Memory</td>
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<td>System Interface Assembly</td>
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<td>PASM</td>
<td>Power Activation and Switching Module</td>
<td>SIO</td>
<td>System I/O Board</td>
</tr>
<tr>
<td>PCA</td>
<td>Power Converter Assembly</td>
<td>SRU</td>
<td>Stellar Reference Unit</td>
</tr>
<tr>
<td>PCM</td>
<td>Power Converter Module</td>
<td>SSE</td>
<td>Sun Sensor Electronics</td>
</tr>
<tr>
<td>PCS</td>
<td>Power Control Slice</td>
<td>SSH</td>
<td>Sun Sensor Head</td>
</tr>
<tr>
<td>PSS</td>
<td>Power Switch Slice</td>
<td>TAS</td>
<td>TRIO Assembly Slice</td>
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