System Interface Assembly

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June 6, 2001
Europa Orbiter/X2000 Avionics
Industry Briefing

Description

- The System Interface Assembly development is in-house (JPL)
  - Prototype SIA (PT) – based on Xilinx Virtex 1000e 560 pin Ball Grid Array FPGA
  - Engineering Model (EM) – baseline replaces FPGA with Honeywell HX3800 ASIC
  - Flight Model (FM)

- System Interface Assembly components
  - Double-sided Compact PCI card
  - Radhard SIA ASIC
  - Radhard UTM BCRTM ASIC
  - Radhard BAE SYSTEMS 128Kx32 SRAM Modules
  - Radhard Intersil RS422 Driver/Receivers
  - Radhard QTECH 12MHz Oscillator

- Interfaces
  - CompactPCI bus
  - Redundant SDST or STM Uplink and Downlink Interfaces
  - Redundant 1553 Interfaces (low power differential implementation)
  - Four High Speed Synchronous Serial Command and Telemetry Interfaces
  - Tz (Time Zero) Umbilical Support Interface
SIA ASIC Description
SIA ASIC Description

- The SIA ASIC provides most of the functionality of the SIA card.
  - The EM/FM SIA ASIC operates on 3.3 volts

The ASIC provides the following major blocks:
- PCI Target Core
  - 33 MHz, 32-bit operations
  - 1 PCI Interrupt
- PCI Rate Buffer Core
  - 1 write (35 x 8 words) and 4 read (32 x 8 words) FIFOs
- Memory FIFO Control Core
  - Configures 1 Mbyte SRAM partitioned into 10 buffers
    - This memory is used as buffer memory between PCI system card and serial interface peripherals. It can be partitioned up to 10 individual buffers, i.e. configurable to optimize a target system whether it uses 1 or all 10 of the buffers.
  - Watermarks, Stale-Timer and “frame done” interrupts provide software flexibility
  - Memory Arbiter – A Fair Round-Robin arbiter
SIA ASIC Description

- **Uplink Core**
  - Configurable to support SDST or STM redundant Uplink Command bit serial interfaces
  - **SDST Mode:**
    - Hardware Command Decoder
    - Provides pulsed decode capability to enable spacecraft reset independent of software
    - 7 level discrete general-purpose hardware decoded commands
    - Performs error checking and bit stream polarity resolution
  - **STM Mode:**
    - Uplink Command Serial Peripheral Interface (SPI)

- **Downlink Core**
  - Configurable to support SDST or STM redundant Downlink Telemetry bit serial interfaces
  - **SDST Mode:**
    - Configurable to support 3 encoding modes: Reed-Solomon, Turbo or no encoding
    - Configurable to provide Pseudo-Randomization of the data
  - **STM Mode:**
    - Downlink Telemetry Serial Peripheral Interface (SPI)

Note: Either STM or SDST style interfaces may be selected by software (triplicate voted in hardware)

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SIA ASIC Description

- **UTMC BCRTM 1553 ASIC Controller Core**
  - Typically used as Bus controller to command and retrieve housekeeping data to/from SDST/STM
  - The BCRTM Controller Core, controlling the UTMC ASIC, can be used as a general purpose Bus Controller or Remote Terminal for many other applications
  - Timed command capability allowing 1 μs resolution command issuance
  - Direct Access tap (intended for RS422 buffers) provides for the 1553 users to monitor 1553 traffic during integration and for closed loop testing support

- **Four high-speed synchronous serial command interface Cores**
  - SIA → sensor/instrument interfaces typically used to command a sensor or instrument
  - 1 Mbps serial interface
  - Timed command capability allowing 1 μs resolution command issuance
  - Three wire hardware interface (clock, data, frame)

- **Four high speed synchronous serial telemetry interface Cores**
  - Sensor/instrument → SIA interfaces typically used to collect sensor or science data
  - SIA supports interface rates to 6 Mbps
  - Three wire hardware interface (clock, data, frame)
SIA ASIC Description

- Time Zero (Tz) Umbilical Support Functions
  - Tz Uplink
    - Uplink commands may be directed toward SIA HCD or may be rerouted to STM
  - Tz Echo Command Monitor
    - Provides method to monitor the spacecraft command source whether it is Tz, SDST or STM
  - Tz Downlink
    - Serial data and clock interface which forwards STM produced telemetry data (if STM mode selected) or SIA encoded telemetry (if SDST mode selected)

- Targeted to a radiation hardened ASIC Foundry.

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Picture of the SIA PT
Key Requirements

- The SIA provides the PCI bridge function to:
  - Four sensors
  - Two Telecommunication Subsystems
    - SDSTs (Small Deep Space Transponder) OR
    - STMs (Spacecraft Transponding Modem).
- PCI Target: 32 bit 33 MHz CompactPCI Bus Specification, PCIMG 2.0 R2.1
  - 1 PCI interrupt (INTA): all interrupts sources are maskable
- SIA clock: 32 bits and 1 µsec resolution (read/write)
- Buffer memory: 1 Mbyte
  - Configurable by software for each interface
    - Configurable Pointers: Top, Bottom, Watermark
- Double-Sided CompactPCI 3U card
  - Mass estimate: 0.5Kg
  - Power Estimate:
    
    |        | Idle | Typ  | Max  |
    |--------|------|------|------|
    | PT:    | 3.2W | 6.5W | 7.1W |
    | EM/FM: | 3.5W | 5.5W | 6.2W |

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Key Requirements

• Spacecraft Transponding Modem (STM) interface:
  – Redundant 1553 interface for engineering data, status and control
  – Redundant Serial Peripheral Interface (SPI)
    • Issues instantaneous serial telemetry output data rate of 4.1 Mbps to the STM
    • Uplink rate on SPI command interface is 2.0 Mbps

• Small Deep Space Transponder (SDST) interface:
  – Redundant 1553 interfaces for engineering and status and data
  – Redundant serial interfaces (one each for command and telemetry) to each transponder
    • Downlink encoding: no encoding, the Reed Solomon Encoder or the Turbo Encoder
    • Downlink telemetry rates: 5 bps and 250 kbps
      (actual maximum rate could be higher to support test activity)
    • Uplink Hardware Commands: 8 discrete outputs settable
      (One output is an active low pulsed signal used as a hardware decoded reset)
    • Direct Access port: supports command data rate up to 250 kbps

• High speed synchronous serial interfaces (4 input and 4 output)
  – Command interface: 1 Mbps instantaneous serial link data transfers per channel
  – Telemetry interface: 6 Mbps instantaneous serial link data transfers per channel
  – Instrument interfaces can be reset independently of all other interfaces

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Current Status

- PDR – August 2000
- CDR – August 2001
- First SIA PT (to test) – February 2001
- SIA ASIC Pre-PDR Tape Out – October 2001
- SIA ASIC PDR Tape Out – November 2001
- SIA ASIC CDR – January 2002
- First SIA EM (POD ASIC) – May 2002
- First SIA EM (EM ASIC) – August 2002
- EM QUAL Complete – August 2002
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Picture of the SIA PT

X2000 System Interface Assembly
SIA PT S/N 002

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