System Flight Computer

Dwight A. Geer
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June 6, 2001
Europa Orbiter/X2000 Avionics
Industry Briefing

Description

- The System Flight Computer development contract with BAE SYSTEMS, Manassas
  - Two performance versions:
    - Baseline: 33 MHz on-board oscillator (EM boards delivered)
    - Enhanced: 66 MHz on-board oscillator plus additional Power PCI functionality (new effort)
  - Commercial SFC (Prototype)
  - Engineering Model (EM)
  - Flight Model (FM)
- System Flight Computer components
  - Double-sided Compact PCI card
  - RAD750 radiation hardened PowerPC 750
  - Power PCI radhard (radiation hardened) PCI bridge chip
  - Shielded Stacked SDRAM
  - RadPack Maxwell (SEI) EEPROM
  - Radhard QTECH oscillator
  - Radhard Omnirel linear regulator
- Interfaces
  - CompactPCI bus
  - UART Interface
  - Interrupts and Discretes – Programmable I/O Discretes
  - JTAG Interface

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Power PCI ASIC Description

- Power PCI provides all required on-card support functions including interfaces to:
  - PCI
  - Memory
  - CPU
  - Test equipment (UART/JTAG)

- Power PCI architecture features
  - Multiple on chip bus structure for highest throughput
    - Dedicated processor - memory bus with ECC
    - High performance processor - PCI bus with parity
    - Lower performance peripheral and test bus
  - Bit and nibble memory error correction
  - Clock generation and control (System, PCI, CPU)
  - PCI Version 2.2 master / target and central arbiter
  - Asynchronous PCI interface
  - JTAG diagnostics (master and slave capable)
  - 16550 compatible UART
  - Programmable interrupts and timers
  - Error recovery embedded micro-controller function

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June 6, 2001
Key Requirements

- Exceeds SPEC95 performance benchmarks (3.2 SPECint95, 2.5 SPECfp95)
  - 6.5 SPECint95, 3.9 SPECfp95 and 240 Dhrystone 2.1 MIPS
  - Performance degradation < 20% while PCI DMA activity is at 66 MB/s
- Power conservation modes controllable by software
- 32 bit 33 MHz CompactPCI Bus Specification, PCIMG 2.0 R2.1
- > 128 MBytes main memory
- > 128 KBytes (256 KBytes actual) SUROM
- EDAC mechanism for all memory
- JTAG and built-in self-test (BIST) capability
- JPL Double-Sided CompactPCI Mechanical ICD (MICD)
- Software includes:
  - Test routines to support BIST functions executed out of SUROM or RAM
  - BSP interface functions and SFC configurable hardware drivers
  - SUROM software to initialize the SFC to a known operational state
### Key Requirements

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<tr>
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<tbody>
<tr>
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<td>242 MIPS</td>
<td>132 MHz</td>
<td>6.0</td>
<td>0.3</td>
<td>1.5</td>
<td>2.0</td>
<td>0.2</td>
</tr>
<tr>
<td>3x Speed</td>
<td>181 MIPS</td>
<td>99 MHz</td>
<td>4.9</td>
<td>0.3</td>
<td>1.5</td>
<td>1.9</td>
<td>0.2</td>
</tr>
<tr>
<td>2x Speed</td>
<td>121 MIPS</td>
<td>66 MHz</td>
<td>3.8</td>
<td>0.2</td>
<td>1.5</td>
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<td>0.2</td>
</tr>
<tr>
<td>High</td>
<td>60 MIPS</td>
<td>33 MHz</td>
<td>2.6</td>
<td>0.2</td>
<td>1.5</td>
<td>1.6</td>
<td>0.2</td>
</tr>
<tr>
<td>Half</td>
<td>30 MIPS</td>
<td>17 MHz</td>
<td>2.1</td>
<td>0.1</td>
<td>1.3</td>
<td>1.3</td>
<td>0.2</td>
</tr>
<tr>
<td>Quarter</td>
<td>15 MIPS</td>
<td>8 MHz</td>
<td>1.8</td>
<td>0.1</td>
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<td>1.2</td>
<td>0.2</td>
</tr>
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<td>4 MHz</td>
<td>1.6</td>
<td>0.1</td>
<td>1.1</td>
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<td>0.2</td>
</tr>
<tr>
<td>Doze</td>
<td>132 MIPS</td>
<td>132 MHz</td>
<td>2.4</td>
<td>0.1</td>
<td>1.0</td>
<td>0.5</td>
<td>0.2</td>
</tr>
<tr>
<td>Doze</td>
<td>99 MIPS</td>
<td>99 MHz</td>
<td>1.9</td>
<td>0.1</td>
<td>1.0</td>
<td>0.5</td>
<td>0.2</td>
</tr>
<tr>
<td>Doze</td>
<td>66 MIPS</td>
<td>66 MHz</td>
<td>1.4</td>
<td>0.1</td>
<td>1.0</td>
<td>0.5</td>
<td>0.2</td>
</tr>
<tr>
<td>Doze</td>
<td>33 MIPS</td>
<td>33 MHz</td>
<td>0.9</td>
<td>0.1</td>
<td>1.0</td>
<td>0.5</td>
<td>0.2</td>
</tr>
<tr>
<td>Doze</td>
<td>17 MIPS</td>
<td>17 MHz</td>
<td>0.7</td>
<td>0.1</td>
<td>1.0</td>
<td>0.5</td>
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</tr>
<tr>
<td>Doze</td>
<td>8 MIPS</td>
<td>8 MHz</td>
<td>0.5</td>
<td>0.1</td>
<td>1.0</td>
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</tr>
<tr>
<td>Doze</td>
<td>4 MIPS</td>
<td>4 MHz</td>
<td>0.5</td>
<td>0.1</td>
<td>1.0</td>
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</tr>
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<td>Nap</td>
<td>132 MIPS</td>
<td>132 MHz</td>
<td>0.3</td>
<td>0.1</td>
<td>1.0</td>
<td>0.5</td>
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</tr>
<tr>
<td>Sleep</td>
<td>132 MIPS</td>
<td>132 MHz</td>
<td>0.2</td>
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</tr>
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**SFC Mass**

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<td>0.549</td>
<td>3%</td>
</tr>
<tr>
<td>0.564 KGS</td>
<td></td>
</tr>
<tr>
<td>1.207 LBS</td>
<td>1.241 LBS</td>
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Picture of the first SFC EM

X2000 System Flight Computer
SFC EM S/N E003

June 6, 2001
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Picture of the first SFC EM

X2000 System Flight Computer
SFC EM S/N E003

June 6, 2001
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- Power PCI internal operation at 66 MHz (baseline is 33 MHz)
  - Reduces memory latency for cache miss
- DMA Controller with the following features:
  - Executes a linked list of DMA commands in RAM.
  - Performs transfers in all combinations of PCI and RAM access
    (RAM → PCI, PCI → RAM, PCI → PCI, RAM → RAM)
  - Generates CPU interrupts on the occurrence of certain events
    - Example: command completion, command list completion and error
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Block Diagram

Flight Model Configuration

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<td>0.2</td>
</tr>
<tr>
<td>Doze</td>
<td>4 MIPS</td>
<td>4 MHz</td>
<td>0.5</td>
<td>0.1</td>
<td>1.0</td>
<td>0.5</td>
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</tr>
<tr>
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