Update on JPL-led CSP/SIP Activities (chip scale package/systems-in-a-package

Abstract

Chip scale packages are now widely used for many electronic applications including portable and telecommunication products. The CSP definition has evolved as the technology has matured and refers to a package with a pitch of 0.8 mm and lower. Packages with fine pitches, especially those with less than 0.8 mm, and high I/Os may require the use of microvia printed wiring board (PWB) which is costly and they may perform poorly when they are assembled onto boards.

JPL-led chip scale package and systems-in-a-package (CSP/SIP) Consortia of enterprises, composed of team members representing government agencies and private companies, have joined together to pool in-kind resources for developing the quality and reliability of CSPs/SIPs for a variety of projects. A test vehicle (TV-1) with eleven package types and pitches was built and tested by the JPL MicrotypeBGA Consortium during 1997 to 1999. Lessons learned by the team were published as a guidelines document for industry use and is distributed by Interconnection Technology Research Institute (ITRI).

The CSP Consortium team jointly concentrated their efforts on building the second test vehicle (TV-2) with fifteen (15) packages of low to high I/O counts (48 to 784) and pitches of 0.5 mm to 1.27 mm. In addition to the TV-2 test vehicle, other test vehicles were designed and built by individual team members to meet their needs. At least one common package was included as control in each of these test vehicles in order to be able to compare the environmental test results and understand the effects of PWB build and manufacturing variables. The most update test resuts on TV-2 and plan for subsequent activities under SIP Consortium will be presented.