ELECTRICALLY ISOLATING SUBSYSTEMS IN SOAC TECHNOLOGIES. R. M. Boyd[1], W. B. Kuhn[1], M. M. Mojarradi[2], and E. A. Shumaker[1], [1]Kansas State University, wkuhn@ksu.edu, [2]Center for Integrated Space Microsystems, Jet Propulsion Laboratory, Mohammad.M.Mojarradi@jpl.nasa.gov.

Introduction: Integrated circuit fabrication technology has evolved to the point that it is possible to construct complete systems, including power, data processing, and communications, on a single chip. Such System-on-a-chip (SOAC) technologies can enable drastic reductions in spacecraft size and weight, lowering the cost of missions and presenting new mission opportunities. This paper overviews some key enabling technologies unique to the needs of spacecraft for outer-planet exploration and missions requiring extreme resistance to radiation such as Europa orbiters and Europa Landers. The work is being carried out by Kansas State University (KSU) under direction of the Center for Integrated Space Microsystems (CISM) at NASA's Jet Propulsion Laboratory.

Electrical Isolation using SOI Technologies: Missions such as the Europa Lander must withstand extreme radiation environments, demanding the use of hardened IC technologies. Silicon-on-Insulator (SOI) CMOS provides good hardness while permitting circuit densities compatible with SOAC design. In addition, SOI offers the unique opportunity to build spacecraft subsystems that are electrically isolated from one another. Since circuits are insulated from the underlying mechanical support structure (substrate), there is no need for a chip-wide common ground as there is in traditional CMOS design. Such isolation is essential in many system designs, including the IEEE 1394 data bus being adopted in X2000 spacecraft.

IEEE standard 1394 defines a high-speed (100 to 400 Mb/s) serial 6-wire bus and an associated parallel backplane bus operating at 12.5 to 50 MB/s. Included in the standard is a power/ground isolation boundary between systems communicating over the parallel bus. This isolation allows connected subsystems with power or ground potential differences and/or noise problems to pass bi-directional data at the full bus speed. The standard provides a suggested method of implementation utilizing transformers and associated driver/receiver circuits. Unfortunately, the physical size, weight, and power consumption implied by this solution is incompatible with the goals of SOAC technologies.

Beginning in the summer of 1999, CISM initiated a research program with KSU's department of Electrical and Computer Engineering to design a fully-integrated solution to the IEEE 1394 isolation requirement. A block diagram of the isolator circuits currently under development is shown in Figure 1. This design provides isolation by transmitting data across a transformer interface, as in the 1394 standard, but uses radio technology to allow significantly smaller transformers to be used. The data is modulated onto a high-frequency carrier, up-converting the spectrum from baseband to approximately 1 GHz. On-chip transformers measuring approximately 200x200 microns square then pass this RF signal across the boundary where it is demodulated and converted back to standard digital levels. The complete system is simple and robust, providing an effective solution that meets all 1394 requirements. Key circuits, including the required transformers have been prototyped in Honeywell's RICMOS IV 0.8um SOI process and are currently in test. A revised design targeting Honeywell RICMOS V (0.35um SOI) is also under development.

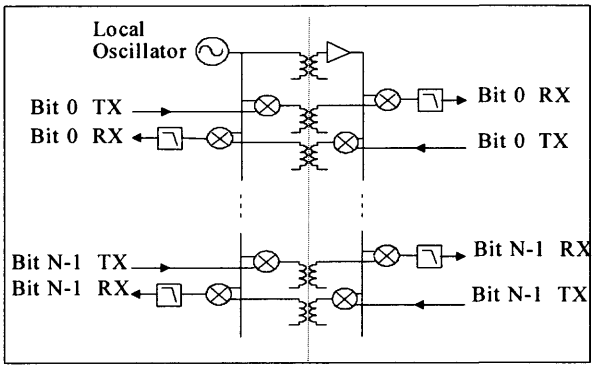

Figure 1. Block diagram of isolator circuits.

Conclusions: The integrated electrical isolation technique under development substantially outperforms all alternatives considered. It is faster and lower power than both traditional (non-integrated) electro-optic methods and recent MEMs based products [1]. Using 0.35um SOI, the design will operate at 2 GHz, consume approximately 15 mA total power (for 12 bi-directional channels), and occupy 1mm^2 of die area. Electrical breakdown is expected to exceed 50V, while noise immunity should exceed 10V/ns. Full-scale prototyping is scheduled to be completed in the 2002 to 2003 timeframe.

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References: [1] umIsolation™ Technology, Analog Devices Inc., www.analog.com/industry/umic.