Integrated Avionics System (IAS), Integrating 3-D Technology on a Spacecraft Panel[1,2]

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Abstract: As spacecraft designs converge toward miniaturization, and with the volumetric and mass challenges placed on avionics, programs will continue to advance the "state of the art" in spacecraft system development with new challenges to reduce power, mass and volume. Traditionally, the trend is to focus on high-density component packaging technologies. Industry has made significant progress in these technologies, and other related internal and external interconnection schemes.

Although new technologies have improved packaging densities, a system packaging architecture is required that not only reduces spacecraft volume and mass budgets, but increase integration efficiencies, provide modularity and flexibility to accommodate multiple missions while maintaining a low recurring cost. With these challenges in mind, a novel system packaging approach incorporates solutions that provide broader environmental applications, more flexible system interconnectivity, scalability, and simplified assembly test and integration schemes.

The Integrated Avionics System (IAS) provides for a low-mass, modular distributed or centralized packaging architecture which combines ridged-flex technologies, high-density COTS hardware and a new 3-D mechanical packaging approach, Horizontal Mounted Cube (HMC). This paper will describe the fundamental elements of the IAS, HMC hardware design, system integration and environmental test results

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1. Introduction

Since the late 1980's studies at JPL have shown that the largest contributor of total spacecraft dry mass is concentrated in two technology areas; structure and packaged electronics. Figure 1 shows the mass weighted average percent of spacecraft by technology area. This concentration of mass, points toward the most potentially fruitful area of technology development to provide significant spacecraft dry mass reduction.

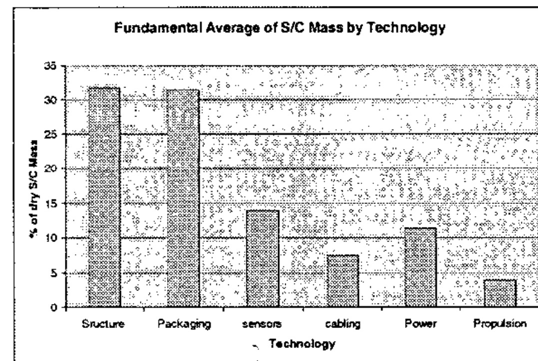

Figure 1

Within the next layer of underlying new technologies to generate mass saving are materials, bus architectures and/or integrating electronic chassis that also function as structural members. The challenge for packaging engineers with this mass reduction challenge is not only to encompass all areas of structural, electrical such as miniaturization of component packages, thermal elements and mission environments but in selecting a packaging configuration that meeting mission needs.

Available avionics packaging configurations include ruggedized 6U VME or 3U CPCI. Other options include free form packaging configuration combining electronics and structure as seen in Rovers. The pros with 6U and 3U configurations include the use of standard test equipment, ease of integration. The cons with 6U and 3U architectures include; heavy enclosure,

backplanes and the need for traditional cabled interfaces.

With these trade-off's and the advent of small, low-cost space missions has brought with it a need for new, advanced packaging technologies, which can enable missions to utilize smaller launch vehicles and lighter payloads. These advances include flexible architectures that can be customized to create a central or distributed system that not only reduce I/O counts and conventional cabling systems, but provide a modular flexible mechanical packaging systems that fits with the paces of spacecraft system architectures and configurations.

In an attempt to develop a new packaging architecture the Advanced Deep Space System Development Program (ADSSDP), comprised of three elements: Outer Planet Technology (X2000), the Center for Integrated Space Microsystems (CISM), and Advanced Radioisotope Power Source Program (ARPS), funded the research for the tasks described in this paper. These organizations make up part of the Outer planets New Millennium Program (NMP), a National Aeronautics and Space Administration (NASA) initiative for a new class of smaller missions.

2. Architecture

The combination of the New Millennium packaging technology with the X2000 system architecture reaches out to produce a product capable of meeting a wide range of mission needs with a flexible architecture that is capable of integrating different instruments, propulsion modules, power sources and telecommunication into a multiple mission platform. The goal is to develop and validate a modular building block design with standard interfaces, enabling this high level of integration with the foresight for future systems on a chip.

Electrical Architecture-- is configured to accommodate three different bus configurations. A PCI Bus to handle the high speed Command and Data Handling functions. The 1394 "firewire" Bus which will provide the high

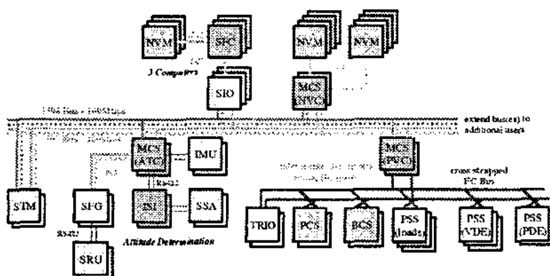

Figure 2

data rate for science data acquisition. And third bus, 12C, for a low power bus that is used to accommodate power switching, pyro and temperature sensor interfaces. figure 2 identifies possible system architecture.

Mechanical Architecture— is made up of three major elements. The first element, the Horizontal Mounted Cube (HMC) houses the command and data handling, power and attitude control electronics. The second element, the Network Bus provides the system interconnectivity from the HMC to the spacecraft. The third Element is made up of a spacecraft structural panel, integrating all three elements. Features incorporated in this panel provide access to the backside of the network bus, which maintains rework capability. The configuration shown in this paper conducts 60 watts from the HMC to its radiative surface These elements make up the Integrated Avionics System (IAS).

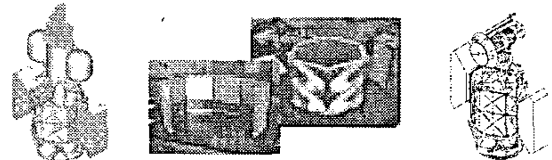

Figure 3

With this IAS approach new options in terms of a common bus become available to the system engineering team. For example, in a centralized architecture the IAS panel could possibly be a load-carrying member of the spacecraft and be configured as a hexagon as shown in figure 3. With the same IAS system reconfigured to a box shaped spacecraft configuration as shown in figure 4.

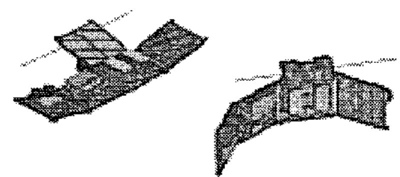

Figure 4

Interchangeability between engineering or flight subsystems provides flexibility for the system design teams to develop a spacecraft configuration independent of the Avionics. These components create the Integrated Avionics System (IAS). A unique multi-configurable system, which is designed across several engineering disciplines. The mission design, and the spacecraft, is optimized to reduce the workload and shorten the development, integration and test activities.

3. Key Technology Development

Configuration-- the Horizontal Mounted Cube (HMC) implements a packaging architecture that strives for modularity between subsystems, and scalability, by orientating frames, termed slices, mounted horizontally as opposed to the traditional vertical mounting. Each slice is made up of a 4.in ^{2} x 0.50-inch aluminum frame, machined to create a cavity and two mounting feet. The slice width's can accommodate three configurations: A singlewide version, a doublewide and a double-sided version. As shown in figure 5

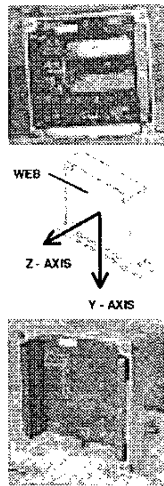

Figure 5

The machined cavity in the frame forms a web. The web serves three functions. First, provides for the attachment of the printed wiring board assembly (PWBA), second as a thermal conduction path. Third, two openings are incorporated along two edges, which provide for the z-axis connections between adjacent slices.

Retention-- each slice is captured to the adjoining slice using a guide pin retention design shown in figure 6. This device acts as a guide for aligning adjacent slices. Clamping is achieved with a #4-40 set screw, which rides on a machined incline. Four guide pin - retainers are located on each slice, one in each corner. The combined clamping force can be well over 100 pounds depending on the screw torque.

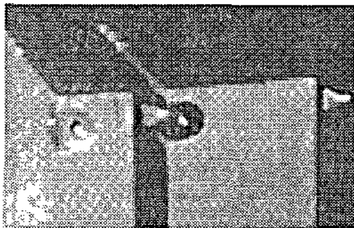

Figure 6

The design becomes scaleable by adding any number of additional slices to maximize mechanical spacecraft constraints for a centralized architecture or as few as four slices for a distributed system. In reverse, slice removal is accomplished by removing its associated four setscrews, on both adjacent slices, and sliding away the slice to be removed. This eliminates disassembly of the entire module and only effects the associated slice.

Analysis-- with the slices mounted in a horizontal configuration, the two mounting feet, machined as part of the frame, provide the dynamic and thermal paths for each slice. The web, described earlier, provides for the attachment of the printed wiring board assembly using a film adhesive by ABLESTIK. This film adhesive serves two roles. Its thermally conductive, specifically designed for bonding materials with mismatched coefficients of thermal expansion. Its conductivity of 0.87W/m ^{0}C, provides the medium for conducting the heat from the printed wiring board assembly to the web. Component junction can be controlled well within 110^{0}C, with a base plate temperature of 70^{0}C. Figure 7 shows the thermal gradient for a typical slice conducting 10 watts.

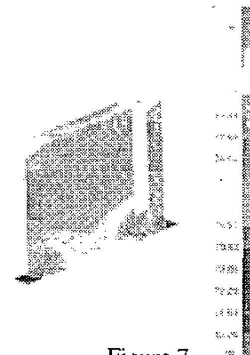

Figure 7

From a structural point of view the combined properties of the printed wiring board, the high bond strength with low shear modulus of the adhesive, combined with the size of the web, create a system with minimum board deflections as shown in figure 8

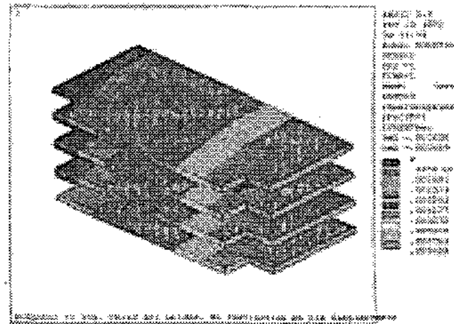

Figure 8

Interconnection Approach--since the HMC design provides for a two-axis interconnection scheme. The relationship between the printed wiring board (PWB) and the four guide pin-retainers plays a key role in the alignment relationship between slices and between slices to the embedded bus. The PWB is located within +/- 0.010-inch true position of the guide pin-retainers. This is accomplished with a process developed for the Mars pathfinder design. The tooling is designed to provide PWB to frame alignment and seconds as a bonding fixture. The fixture, frame, and PWB are laminated together under pressure and temperature.
The slice to slice, and slice to embedded bus, connectivity are accomplished using COTS hardware. Two Cinch CIN-APSE, 248 contact high-density solderless connectors (see Figure 9) are used for the z-axis, or slice to slice connection. A Teledyne Kinetics 112 contact high-density solderless connector (see Figure 10) is used for the y-axis, or slice to embedded bus connection. Both were selected for their $-100\ ^{0}$C plus, cold temperature capability.

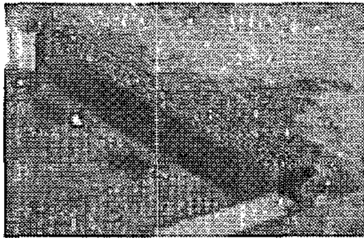

Figure 9

The Cinch connector shown in figure 9 is made up of a "plunger / fuzz-button / plunger" construction which mounts on the component side of the PWBA, with three 2mm flat head screws. The frame and PWBA construction allow the connector to extend above the assembly. When joining slices are mated together, the Cinch connector protrudes through the opening in the adjacent web and makes contact with copper and gold plated pads on the opposing slice or PWBA.

The Teledyne connector shown in figure 10 is a right-angled connection system. Its uniqueness comes from its ability to make two perpendicular solderless connections. The one edge of contacts mounts to the component side for the PWBA, and is captured in place using three 2-56 flat head screws

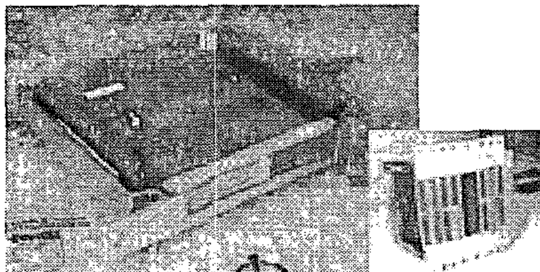

Figure 10

Per slice I/O capability in the current configuration is 608 connections, with the maximum contact count of 856. Both connectors have current carrying capability of 3 amps. This makes the power system robust and maintains design flexibility

Slice Alignment-- between adjacent slices is mainly controlled by the close tolerance of the guide pin – retainer design as refereed to under *Retention* section reference figure 6. Any misalignment between the Cinch connector to PWBA is accommodated with this teardrop shaped pad shown in figure 11. This pad also provides the inner board layer connection with via's located within the pad design.

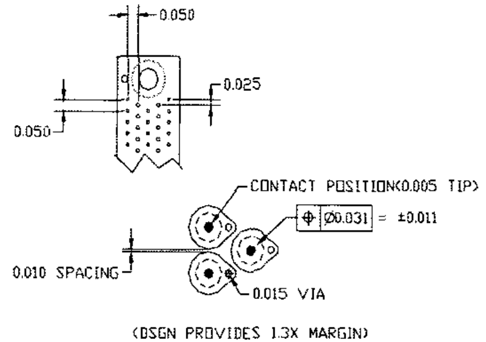

Figure 11

4. Network Bus Technology

The system interconnection design as shown in figure 12 for the IAS creates the ability to interconnect components in all three dimensions without the use of a conventional harness. Yet providing a unique approach for maintaining system level rework capability. The network bus incorporates three key design features. 1. The electrical approach for accommodating the 1394 Bus signals. 2. Provides for a reliable mechanical alignment design between the y-axis connector and the embedded bus. 3. Enables a method for maintaining rework capability at all levels of integration.

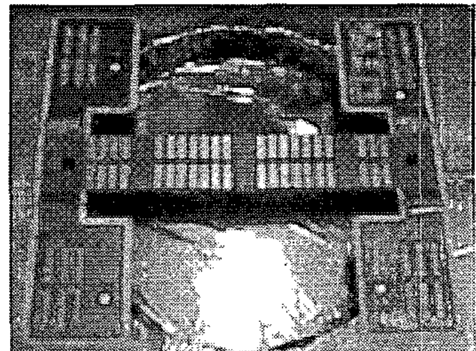

Figure 12

The Electrical Interconnection-- incorporates a standardpolyamide, multi-layer, ridge-flex construction. The configuration provides for a twenty four-slice HMC assembly, logic to drive the 1394 bus and panel to panel interfaces. Twenty-one of the twenty-four slices make up the y-axis interface to the 1394 and I2C Bus. IPC-D-317, design guide lines for high speed techniques was used to implement the 1394 bus signal propagation. The two approaches selected, incorporated a coincident straight and parallel pair schemes. These methods satisfied the capacitance requirements of an equivalent 1394 twisted shield pair system.

The mechanical alignment-- between the HMC's y-axis connector and the network bus is confined only to the relationship between the connectors centering pin and the circuit pad configuration on the bus as shown in figure 13. This is defined as the short axis or pitch of the connector contacts. The pad design provides for the appropriate pad width to accommodate the worst case slot edge to pad edge tolerance of +/- 0.009 true position. Well within PWB manufacturing tolerances

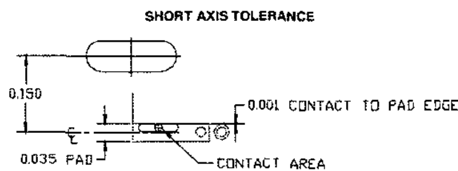

Figure 13

The total HMC slice to slice tolerance stack up defines the long axis tolerance. The pad design provides for the appropriate pad length to accommodate the worst-case tolerance build up of the 24-slice configuration. The long axis control only requires positional control to a selected slice as shown in figure 14. The circuit pads and HMC mounting hole provide for the balances of the tolerance.

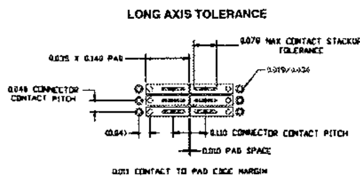

Figure 14

Rework—maintaining rework capability at all levels of integration is a key element for the success of the network bus approach. Since it's a direct replacement for the traditional cable harness. The approach taken is along the same lines as "cut etch" and haywire for circuit changes on a PWBA. The network bus incorporated a dual via interconnection system for each y-axis connection pad. Simply, the etch connecting the dual via's can be cut, disabling the circuit and allowing a haywire to be rerouted to it's new destination. See figure 15

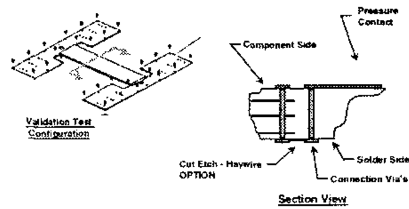

Figure 15

5. System Integration

The HMC module(s) is assembled into it's defined number of electronic slice for a centralized or distributed system. The Network bus is attached to the spacecraft panel. The HMC is lowered onto the bus relying on the y-axis center pin to guide the y-axis contacts to the circuit pads on the network bus. Figure 16 shows a centralized assembly. The HMC is bolted in place or clamped using ground test equipment during system integration. The IAS is now a completed testable subassembly. Signals can be tested using conventional means, which are accessible through the panel. The panel is integrated to the spacecraft.

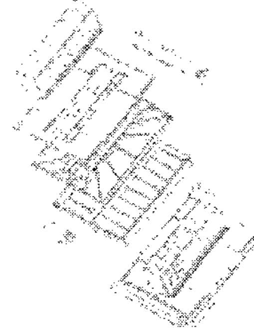

Figure 16

6. Validation Test

Dynamics and thermal test were performed to ensure that the baseline packaging techniques are structurally sound, provide sufficient thermal dissipation, and transmit electrical signals adequately based on flight predicted operating extremes. Figure 17 shows the dynamics and thermal test configurations.

Figure 17

Dynamics Test--included in situ testing of the Y and Z-axis connectors. Eight circuit paths threaded through over 11,000 pin contacts covering 91% of the total I/Os in the system. The IAS was instrumented to detect open pulses within 11ns. The primary testing was high-level random, augmented by low-level sine sweep for model correlation and detection of changes in response along with simulated pyrotechnic shock.

A simple finite element model of the panel was used to estimate the response of the panel and the electronics module. Since the electronics module was relatively stiff compared with the panel, the electronics module was simply modeled as a rigid body. This simplified model provided a reasonable estimate of the module response, as shown in this plot of the measured and predicted response on the electronics module normal to the panel for a low level (¼ g panel input) sine excitation. The responses and input levels (inputs to the panel) are shown in figure 18.

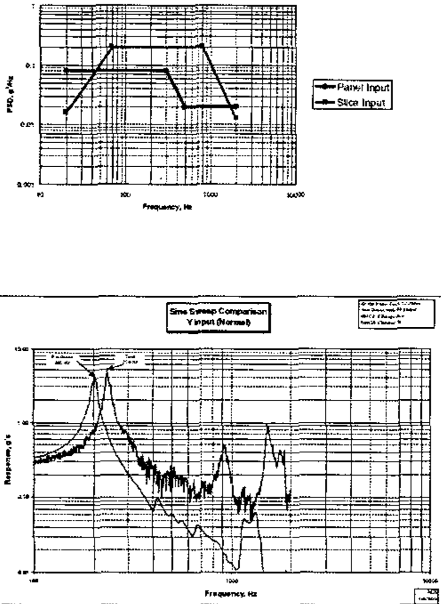

Figure 18

Thermal Vacuum Test-- was performed over a 3-day period in February 1999. The main objectives of the test were;

1) Verify electrical continuity of the Y- axis & Z-axis connectors as the entire panel was cycled 3 times over the qualification temperature range of -70°C to +75°C.

2) Determine the thermal performance of the prototype panel by measuring the temperatures of the panel and avionics slices at two different 3-D stack power levels (nominal and high).

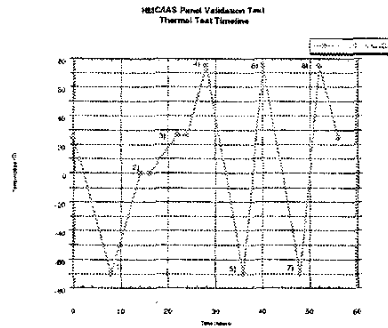

Figure 19

A thermal test timeline indicating the temperature of the slice-to-panel interface during the entire test is shown in the figure 19. The test began with a cold qualification test point at
-70°C and continued with two steady state performance test points (at stack power levels of 19W and 57W) and finished up with the remaining 3 temperature cycles between 75°C and -70°C.

The thermal performance of the 3-D stack and the IAS panel in the test agreed fairly closely with thermal analysis predictions. The analytical thermal model predicted the actual slice interface temperature within 10°C in the nominal power case and within 1°C in the high power case. Adjusting the longeron-to-panel thermal conductance in the model will improve model predictions. The maximum temperature rise from the slice interface to the middle of the flight computer PWB in the high power case (for a slice dissipation of 8.0W and a stack dissipation of 57W) was 20°C. The maximum flight computer PWB temperature in this case was 43°C. The 3-D stack and the IAS panel have been proven to efficiently reject heat to an external environment sink.

7. Conclusion

A number of challenges were met in the areas of mass and volume reduction and most importantly the implementation of technology that provide system flexibility. Figures 20 show a mass reduction and figure 21 shows a volume reduction between conventional packaging options and the Integrated Avionics System.

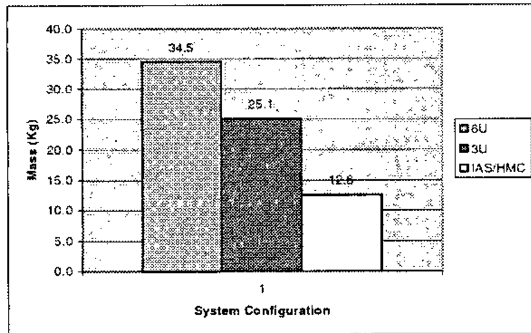

Figure 20

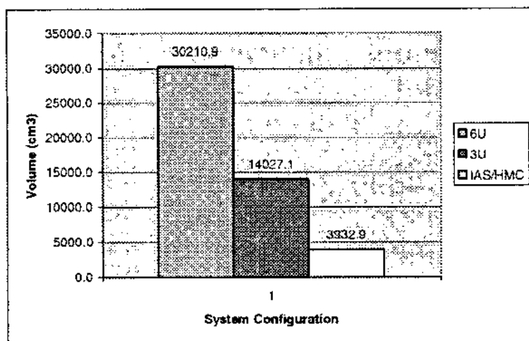

Figure 21

The dynamic and thermal environmental tests performed, validated that packaging design can meet or exceed predicted performance. The in situ dynamics test results indicated no opens during the entire test duration, and the thermal vacuum test proved the 3-D stack and IAS design to efficiently reject heat to an external environment.

The ADSSDP packaging architecture maintains a level of flexibility that can be customized to create both a central or distributed system. The three dimensional solution provides a more flexible system interconnectivity, scalability, and simplified assembly test and integration options. The low-mass modular design combines high-density packaging techniques, COTS hardware, along with standard technologies to create a product flexible to accommodate multiple missions.

8. Acknowledgements

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Don J. Hunter *is a Senior Member of the Technical staff in the Electronic Packaging and Fabrication Section at Jet Propulsion Laboratory. He started at the Laboratory in 1993 as the lead Packaging Engineer for the Mars Pathfinder Mission. His major contributions include; development of a ruggedized 6U-VME-flight systems design. As part of the early X2000 development Team, he received a Cal Tech and US Patent for work in an advanced packaging systems architecture, Integrated 3D Technology on a Spacecraft Panel. As member of the Outer Plants Advanced Study Team he has been involved in spacecraft system designs for future missions associated with Comet Nucleus Sample Return and a Europa Lander. As a member of the Center for Integrated Space Microsystems Team tasks include; development of technology testbed, feasibility studies for miniature science and navigation instruments and System on a Chip activities. Don has been involved in the Electro-Mechanical packaging environment for over 23 years. Experience ranging from commercial applications of deck top test equipment, Military (DOD) cold temperature and high-G integrated packaging applications. He has a Bachelor of Science in Mechanical Engineering from California State University Los Angles*

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