A MULTI-MISSION TESTBED FOR ADVANCED TECHNOLOGIES.

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Introduction: The mission of the *Center for Space Integrated Microsystem (CSIM)* at the Jet Propulsion Laboratory is to develop advanced avionics systems for future deep space missions. The Advanced Micro Spacecraft (AMS) task is building a multi-mission testbed facility to enable the infusion of CISM technologies into future missions. The testbed facility will also perform experimentation for advanced avionics technologies and architectures to meet challenging power, performance, mass, volume, reliability and fault tolerance of future missions. The testbed facility has two levels of testbeds: a *Proof-of-Concept (POC) Testbed* and an *Engineering Model Testbed*. The methodology of the testbed development and the process of technology infusion are presented in a separate paper in this conference. This paper focuses only on the design, implementation, and application of the *POC testbed*.

Testbed Design: In order to be used by multiple missions, the *POC Testbed* has to accommodate various advanced technologies and perform a wide range of architecture experiments. Therefore, flexibility is the primary concern in the design of the testbed. In order to maximize scalability, reconfigurability, and technology compatibility, the *POC Testbed* adopts a variety of commercial standard interfaces. Some of the standard interfaces are actually used in flight projects.

The initial configuration of the *POC Testbed* is based on the scalable, fault-tolerant, and distributed architecture developed by the X2000 project [1]. The architecture consists of a network of computing nodes and controllers that are connected by two redundant sets of buses; each set consists of an IEEE 1394 bus and an I^2C bus. Both of the buses are widely accepted industrial standards. When a node or bus media failure occurs, one of the redundant bus set can continue to operate while the failed bus set diagnoses and reconfigures itself. The bus architecture is designed to tolerate multiple faults.

In addition, each computing node has a Peripheral Component Interface (PCI) backplane bus that can accommodate a wide range of peripherals including other bus interfaces such as the 1553B or Ethernet. The PCI bus allows the IEEE 1394 or I^2C to be easily replaced by more advanced buses in the future.

The testbed can integrate with other advanced technologies developed by *CISM* through the standard interfaces. For example, a micro sensor can choose to use the IEEE 1394, I^2C, PCI, or any other available buses to interface with the testbed. The standard interfaces also enable the testbed to be configured into a variety of architectures to suit the needs of different flight missions.

Testbed Implementation: The current testbed has a network of five computing nodes, connected by two redundant sets of IEEE 1394 and I^2C buses [2]. The size of the testbed is chosen so that it can demonstrate interesting fault tolerance test cases. However, there is no restriction on the number of nodes in the testbed.

Physically, each computing node is a Compact PCI chassis housing two PowerPC 750 processors. One of the processors is the main processor of the node, while the other is used to simulate sensors, actuators, or other on-board instruments. Hence, experimentation of a flight system can proceed even if some of the hardware are not yet available. The PowerPC 750 processors also have UART ports and Ethernet. These standard interfaces enhance the flexibility of the testbed.

The testbed is supported by several testing and software development tools. This includes analyzers for the IEEE 1394, I2C, and PCI buses, and three Unix workstations. All the support equipment are connected to the testbed via the Ethernet. The implementation of the testbed is depicted in Figure 1. The implementation is expected to be completed by Spring 2001.

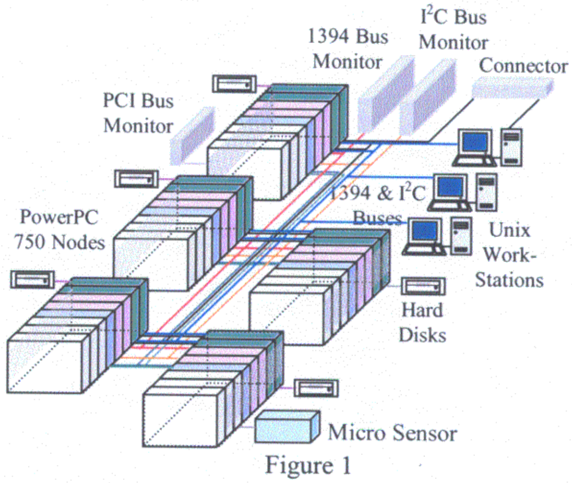

Figure 1

Testbed Application: The *POC Testbed* would be used to verify avionics systems for Europa Lander, Titan Explorer, Comet Nuclear Sample Return, and many other deep space missions.

References:

[1] S. Chau, L. Alkalai, A. Tai, and J. Burt, 351-359.
[2] S. Chau and Don Hunter, *X2000 Future Deliveries FY'01 Task Plan, JPL Internal Document.*

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