MEMS Reliability Alliance
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MINIMUM DIMENSION DIMPLE ANALYSIS

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The MEMS Reliability Alliance is composed of three core institutions:

(1) MEMScaP S.A., a MEMS software company who provides the MEMS-Pro design software.
(2) Cronos Integrated Microsystems, a wholly-owned subsidiary of JDS Uniphase. Cronos provides a polysilicon surface micromachining process (MUMPs™) to the international MEMS community
(3) Jet Propulsion Laboratory, which provides the MEMS test structure design, release etching, testing, and characterization.

Microstructures were designed at JPL using MEMS-Pro and fabricated using the MUMPs™ process at Cronos (see Figure 1).

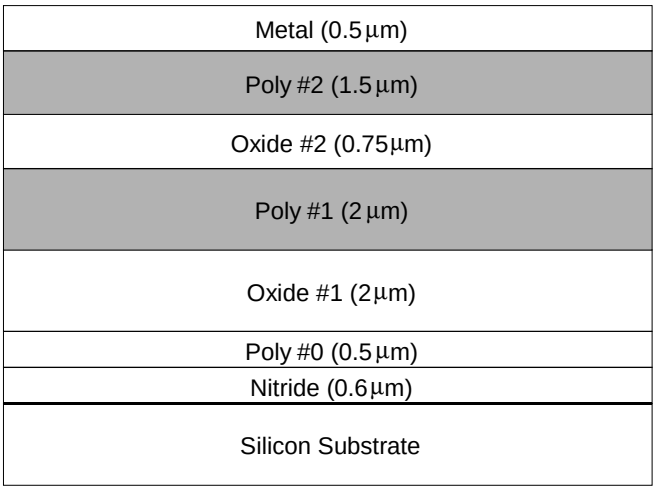

Figure 1. MUMPs™ layer stack. Poly1 and poly2 are structural polysilicon layers, while the oxides are sacrificial layers in that they do not appear in the final structure. Poly0 is used as a ground plane and the nitride is used for electric isolation. Metal layer on top (gold) is for optional contact metalization.

In this process, the first oxide layer (oxide #1) is lithographically patterned with the DIMPLE mask (dimples not shown in Figure 1). The dimples, 750nm deep, are reactive ion etched into the first oxide layer. When the first structural layer of polysilicon is deposited (poly1), it conformally covers the oxide and therefore fills in the recesses created by the dimple

etch. Thus, the polysilicon will be closer to the substrate in these areas (see Figure 3). When the oxides are etched away during the release etch, these recessed areas in the polysilicon are designed to reduce stiction by minimizing the amount of surface area actually in contact with the substrate after release. Usually, the dimples are pattered into small squares throughout the poly1 mask to create a periodic array of "bumps" or bushings that lift the majority of the polysilicon plate 750nm off the substrate.

According to the MUMPS design rules available from Cronos, the minimum feature size for the dimples is 2µm while the minimum spacing is 3µm. In the MUMPS36 run, minimum dimension dimples (i.e. 2µm × 2µm) do not appear in the final structure, but 3µm × 3µm dimples do appear. The test structure used to study this anomaly is a hinged poly1 plate, shown in Figure 2. After release etching the poly1 plate is free to rotate about the poly2 staples anchored to the substrate (see Figure 3).

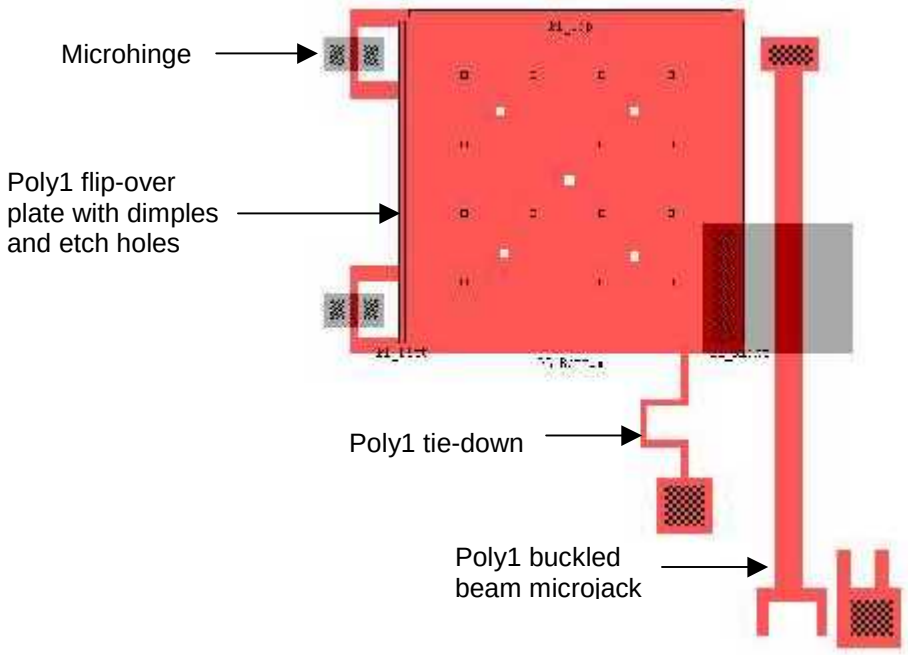

Figure 2. Top view of the hinge layout drawn using MEMS-Pro software. Plate dimensions vary from 100um x 100um to 500um x 500um. The tie-down is supposed to be broken after release etching. Microjacks are used to help lift the poly1 plate -- using a probe the free end is pushed towards the anchored end, buckling the beam, and lifting the poly1 tab. Then a second probe can then be safely slid under the plate to complete rotation about the hinges.

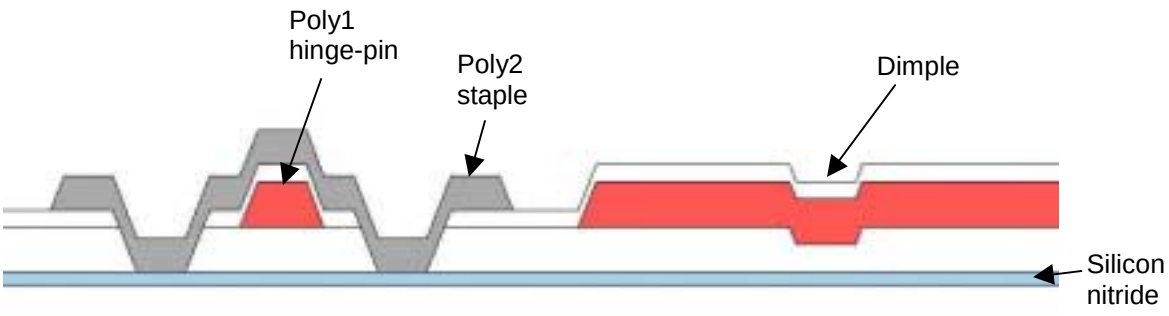

Figure 3. Cross-section through the hinge, as simulated using MEMS-Pro software. Also shown in this cross section are both sacrificial oxide layers (oxide 1 and oxide 2) and the silicon nitride layer that covers the whole substrate for electrical isolation. The dimple layer is also simulated, as shown by the dip in the poly1 layer.

Optical microscope photographs were taken of poly1 plates after release etching. Both sides were photographed -- i.e. the top side and the bottom side, which became visible once the plate was rotated 180° about the hinges. Clearly, if the dimples have dimensions 3μm × 3μm in the MEMS-Pro layout, they were fabricated (see Figure 4 and 5).

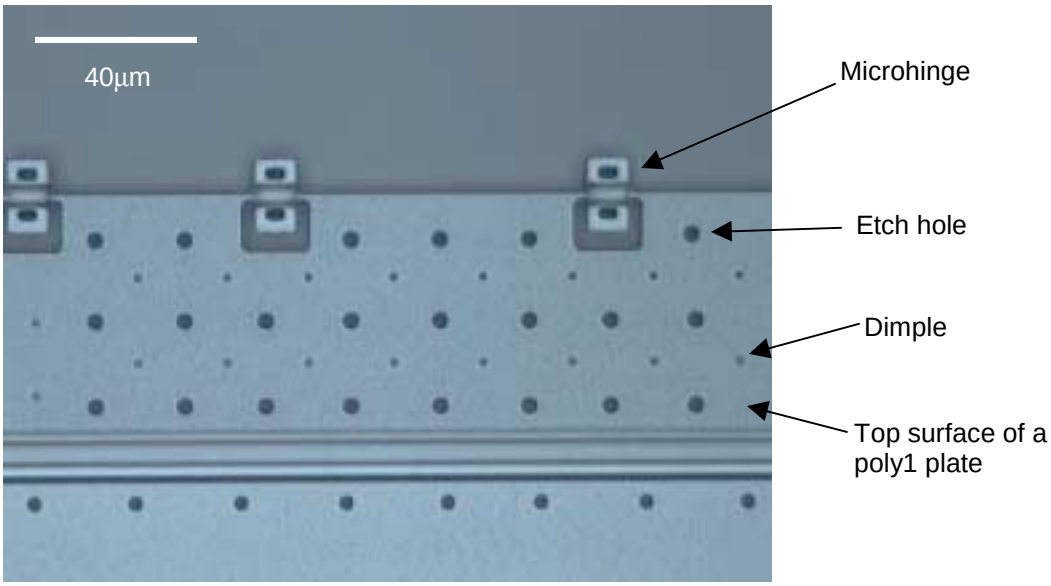

Figure 4. Top view of the top surface of an unassembled poly1 plate showing dimples. Although the dimples and etch holes have the same dimensions in MEMS-Pro (3μm ×3μm square), the etch holes are about 4μm in diameter and the dimples are about 1 - 1.5μm in diameter. This test structure is different from the one shown in Figure 1.

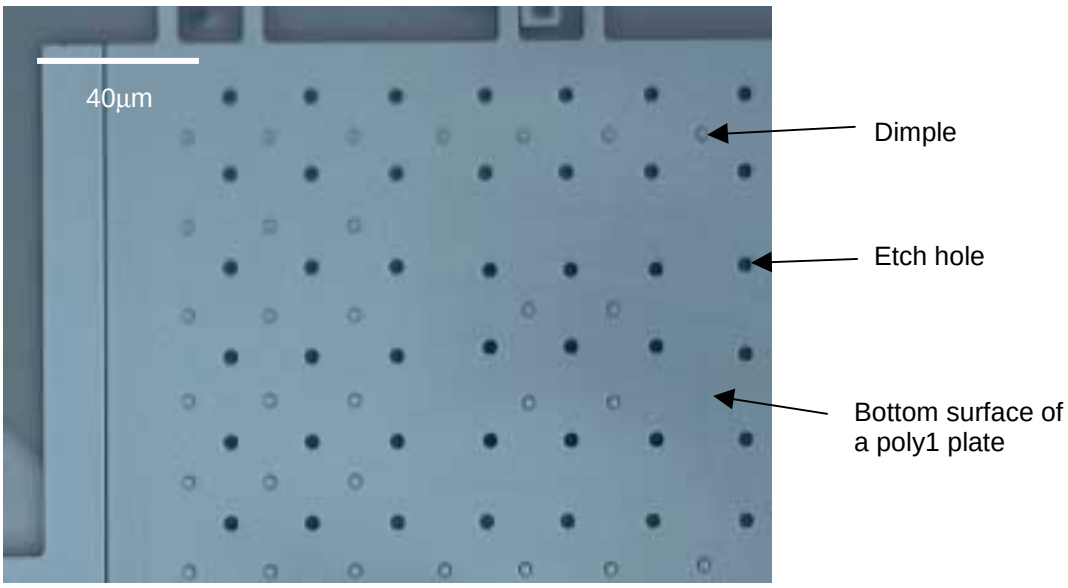

Figure 5. Vie w of bottom side of a poly1 plate after rotation about the hinges. The dimples and etch holes have similar dimensions. In this photograph, some of the dimples in the array are intentionally omitted. This test structure is different from the one shown in Figure 1 and Figure 4.

Conformal coverage of the 2µm -thick poly1 layer is indicated by the smaller visible feature on the top surface compared to the bottom surface. The polysilicon is expected to fill in the patterned hole in oxide1. The sidewalls of the feature may be thicker than 2µm, which would explain the smaller features on the top surface as shown below:

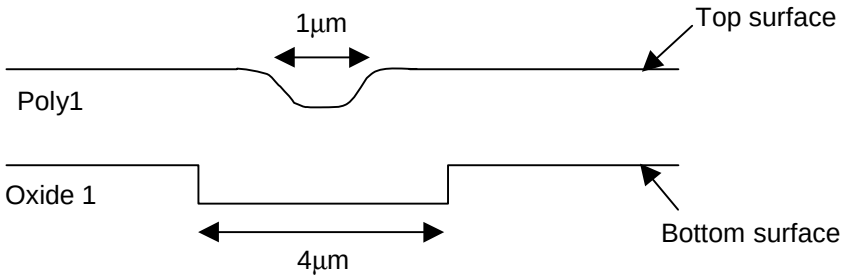

Figure 6. Side view diagram showing conformal coverage of the polysilicon over the recess etched into the oxide. Recess is 0.75µm deep. Imaging the top and bottom surfaces would produce features of different dimensions.

The test structure shown in Figure 1 was designed in MEMS-Pro such that the etch holes were 3µm × 3µm and the dimples were 2µm × 2µm. When the MUMPS36 chips came back from the fabrication facility, the dimples did not appear in the final structure, as shown in Figure 7 and 8. This indicates that either (a) 2µm × 2µm is not the minimum dimension for dimples or (b) there may be a dimple mask error at the fabrication facility. The 2µm × 2µm dimples are not being etched into oxide 1.

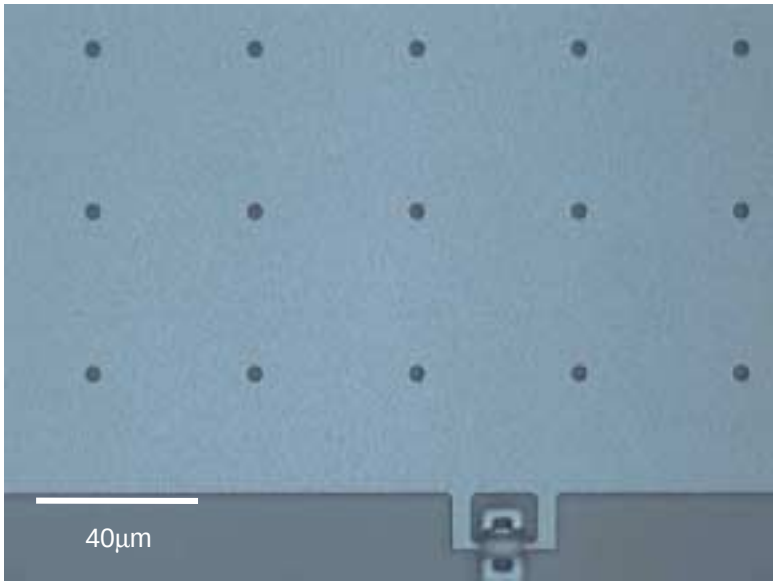

Figure 7. Top surface of the polysilicon flap test structure. Etch holes are clearly visible but the dimples are not.

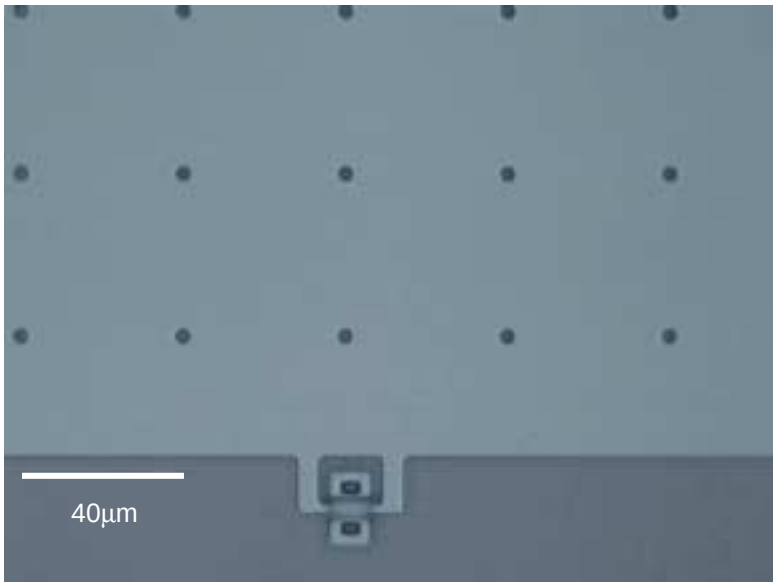

Figure 8. Bottom surface of the polysilicon flap test structure. Etch holes are clearly visible but the dimples are not.

Conclusions

- According to the MUMPS design rules, the minimum feature size for the dimples is 2µm while the minimum spacing is 3µm. In the MUMPS36 run, minimum dimension dimples (i.e. 2µm × 2µm) do not appear in the final structure, while 3µm × 3µm dimples do.