

# **Flight Qualifying SoC Devices**

Jonathan Perret

April 16, 2002

## **Flight Qualifying SoC Devices**

- 1. SoC technical challenges**
- 2. qualification scope**
- 3. technical approach**
- 4. conclusions**

# **1. SoC Technical Challenges**

**the qualification process for SoC devices needs to address:**

- **complexity**
  - **>10 million transistors**
  - **integrated digital IP cores & custom design at various abstraction levels**
    - **behavioral models (C++ or Verilog-A)**
    - **RTL Verilog (soft cores)**
    - **gate-level Verilog**
    - **transistor-level netlists**
    - **physical designs (hard cores)**
  
- **integrated analog circuits**
  - **ADCs and DACs**
  - **DC-DC converters and voltage references**
  - **amplifiers and transceivers**
  - **PLLs**
  
- **embedded software**

**this presentation identifies an approach to the qualification process for SoC devices intended for use in space applications.**

## **2. qualification scope**

**(description)**

- **qualification establishes that the SoC device will operate properly over the environmental conditions by verification of functionality and the key device parameters throughout the development process**
  - **Table 2.1 on the next page identifies the space environments**
  - **Table 2.2 on the next page identifies the key SoC device parameters**
  
- **the traditional ‘qualification’ steps per MIL-STD-883 include:**
  - (d) wafer probe acceptance tests**
  - (e) packaged device acceptance tests**
  - (f) 1000 hour lifetest at 125oC**
  - (g) ESD sensitivity tests**
  - (h) TID radiation tests**
  - (i) SEE radiation tests**
  - (j) other required tests per MIL-STD-883**
  
- **for SoC device qualification three steps should be added at the front of the development cycle:**
  - (a) specification quality review \***
  - (b) specification compliance review \***
  - (c) embedded software test coverage review \***

## 2. qualification scope (cont'd)

Table 2.1 space environment for SoC devices:

•lifetime	Mars: 5 years; Pluto:15 years
•temperature	55°C to +125°C (operating)-65°C to +150°C (storage)
•voltage	+ 3.3 Volts +/- 10%
•electrical latch-up sensitivity	no latch-up due to power sequencing or interface signals
•ESD sensitivity	Class 2 device i.e. survive an ESD pulse 2000 V min, 200 msec duration
•total dose radiation	Mars: 20 Krad(Si); Europa 1Mrad(Si); [50 rad(Si)/s dose rate]
•single event effects radiation	no latch-up [LET:75 MeV-cm <sup>2</sup> /mg; fluence: 10 <sup>7</sup> ions/cm <sup>2</sup> ] acceptable upset rate [LET:75 MeV-cm <sup>2</sup> /mg; fluence: 10 <sup>6</sup> ions/cm <sup>2</sup> ]

Table 2.2 key SoC device parameters measured:

•functional compliance	per the specification
•power consumption	static and dynamic and vs operational modes
•digital electrical characteristics	interface voltages and currents and timing margins
•digital testability	stuck-at-fault coverage, Iddq node toggle coverage
•analog performance	dynamic range, bandwidth, isolation and noise performance

# **3. technical approach**

**(three new qual steps)**

**(a) specification quality review**

- **verify that the specification is complete, satisfactory to the customer, and configuration controlled**
- **accomplish this via technical peer review and release of the SoC specification**

**(b) specification compliance reviews**

- **verify that the SoC complies with the specification at each level of abstraction:**
  - **behavioral / RTL verilog / netlist-level / physical design (layout) / silicon**
- **assure that adequate simulation testbench or test program coverage of the spec is provided**
- **accomplish this via technical peer review at completion of each design phase:**
  - **architectural design / verilog coding or schematic generation/ synthesis /layout) / device testing**

**(c) embedded software test coverage review**

- **verify that the SoC software complies with the specification**
- **assure that adequate software test coverage of the spec is provided**
- **accomplish this via technical peer review at completion of each design phase:**
  - **architectural design / C++ coding / FPGA prototype hardware tests**

- **these new qualification steps are depicted in the SoC development work flow in the appendix**

### **3. technical approach**

**(techniques)**

- **techniques that address the technical challenges for SoC devices:**
  - **complexity**
  - **integrated analog circuits**
  - **embedded software**

# **3. technical approach**

## **(techniques addressing SoC Complexity)**

- **maintain ‘design closure’ at the physical design level**
  - **Show that it’s going to work wrt: chip-level timing / die size / signal integrity**
  - **identify chip-level layout and routing constraints on the functional blocks early**
  - **partition functional blocks so that their complexity is within the design tools capabilities**
    - **(e.g. for back-annotation)**
- **maintain ‘design closure’ at the behavioral model level (C++ or Verilog-A)**
  - **modeling at behavioral level of abstraction**
    - **enables acceptable simulation times**
    - **enables observation of complete device behavior (e.g. bus transactions)**
    - **verifies integrated hardware (digital and analog) and software configuration**
    - **catches software bugs by using real SW to produce hardware stimuli**
    - **verifies the interactions of hardware IP core elements**
    - **enables definition/modification of the interfaces independent of functions and vice versa**
- **use ‘model checking’ to check RTL Verilog against specification**
  - **conversion from behavioral model to RTL Verilog is error prone**
  - **eliminate specification or spec compliance holes (i.e. test escapes)**
- **use ‘equivalence checking’ to match gate-level Verilog to RTL Verilog code**
- **re-use testbenches up and down the levels of design model abstraction:**
  - **behavioral / RTL verilog / netlist-level / physical design (layout) / silicon**
- **run ‘stress case’ simulations to check operational corners**

### **3. technical approach**

#### **(techniques addressing SoC Complexity cont'd)**

- **incorporate DFT design up-front, instead of ad-hoc (after-the-fact)**
- **basic testability techniques include: partitioning, controllability and observability**
  - **provide for initialization of the design to enable good test coverage**
- **use best combination of DFT techniques per design application and constraints:**
  - **boundary scan and 1149.1 (JTAG) port access**
  - **BIST for both digital *and analog* circuits (enables functional at-speed tests on-chip)**
- **include ‘test wrappers’ around integrated IP cores to allow:**
  - **IP cores outputs to be controlled**
  - **IP core outputs to be bypassed**
  - **IP core outputs to be monitored**
- **include ‘test-access collars’ and bypass logic around analog blocks to allow:**
  - **analog block inputs to be controlled**
  - **analog block outputs to be bypassed**
  - **analog block outputs to be monitored**
- **verify operation of the test modes via 1149.1 (JTAG) ports**
- **for test program**
  - **apply functional at-speed tests to the critical paths**
  - **balance functional at-speed tests with low-speed structural test vectors (due to test time)**
  - **correlate (match) test program test vectors with simulation testbench test vectors and results**

### **3. technical approach (cont'd)** **(techniques addressing Integrated Analog Circuits)**

- **digital switching noise coupling to analog circuits is crucial issue for SoC devices**
  - **reduce magnitude, frequency of current, voltage switching**
- **analog blocks will require special attention for:**
  - **power sources**
    - **utilizing separate analog and digital supplies**
    - **adequate power and ground pad distribution and interleaving in padding**
    - **utilizing gridded networks of high conductance, low inductance for power rails**
    - **adequate sizing of power connections**
  - **signal paths**
    - **signal routing, shielding, impedance matching**
    - **'soft-connects' that occur when nodes are inadvertently connected via the substrate**
  - **noise isolation**
    - **sampling crucial analog signals during 'quiet intervals'**
    - **utilize differential circuits to mitigate common-mode coupling and power supply noise**
    - **avoid capacitive noise pick-up by sensitive transistors**
      - **add 'antenna diodes' to protect sensitive FET gates)**

### **3. technical approach (cont'd)** **(techniques addressing Embedded Software)**

- **(phase 1) software verification: host-processor compiled simulations (with hardware stubs)**
  - **software designers preferred method: many tools available, debugging software is easier**
  
- **(phase 2) hardware/software verification: run/verify software code on FPGA prototype (with embedded uP)**
  - **keep software design tasks in synch with hardware tasks**
    - **visibility into both HW and SW is the key to fast debug**
    - **HW validations must have sufficient SW content to be realistic**
    - **check that software tests cover the whole application spectrum (need adequate test coverage)**
  - **use 'real software' to operate/verify the synthesized uP core**
    - **e.g. use the 'boot-code' early to check out the uP**

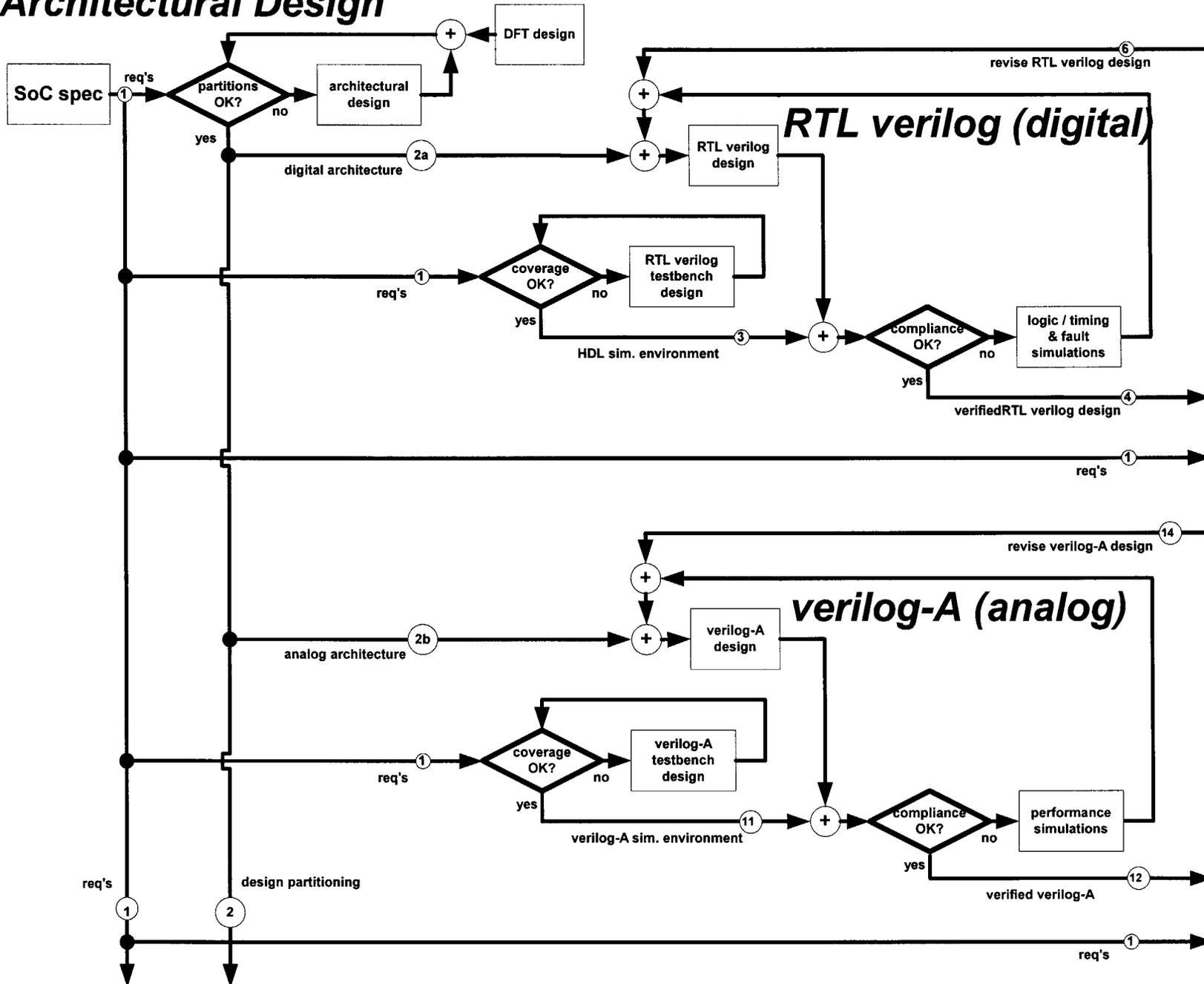
# **Flight Qualifying SoC Devices**

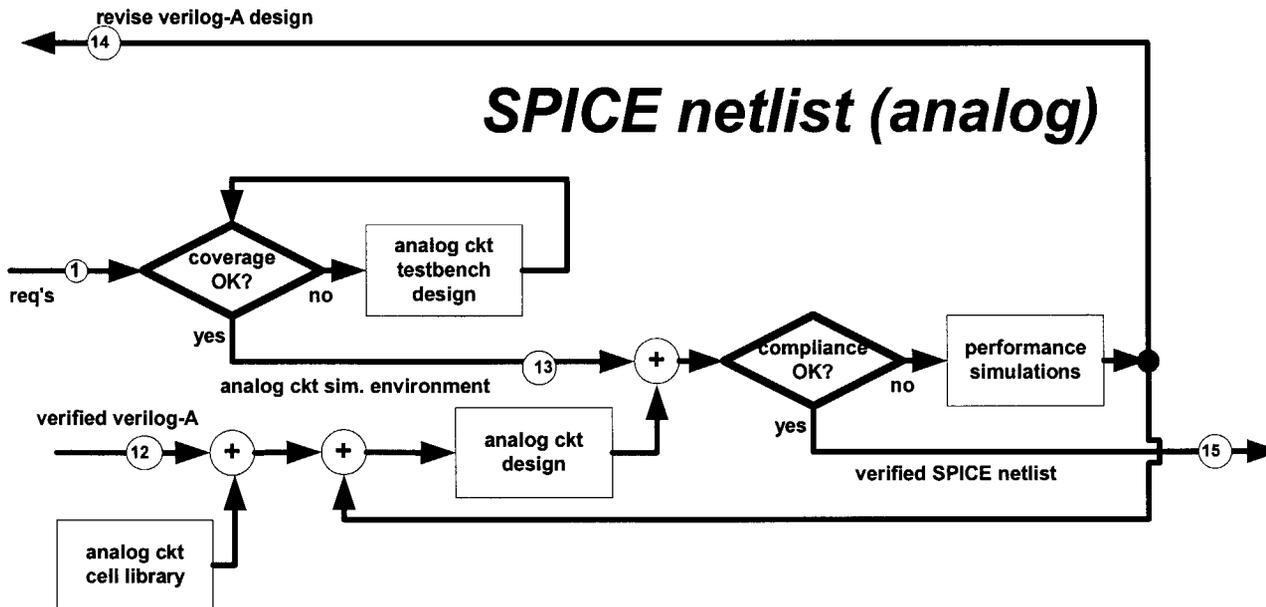
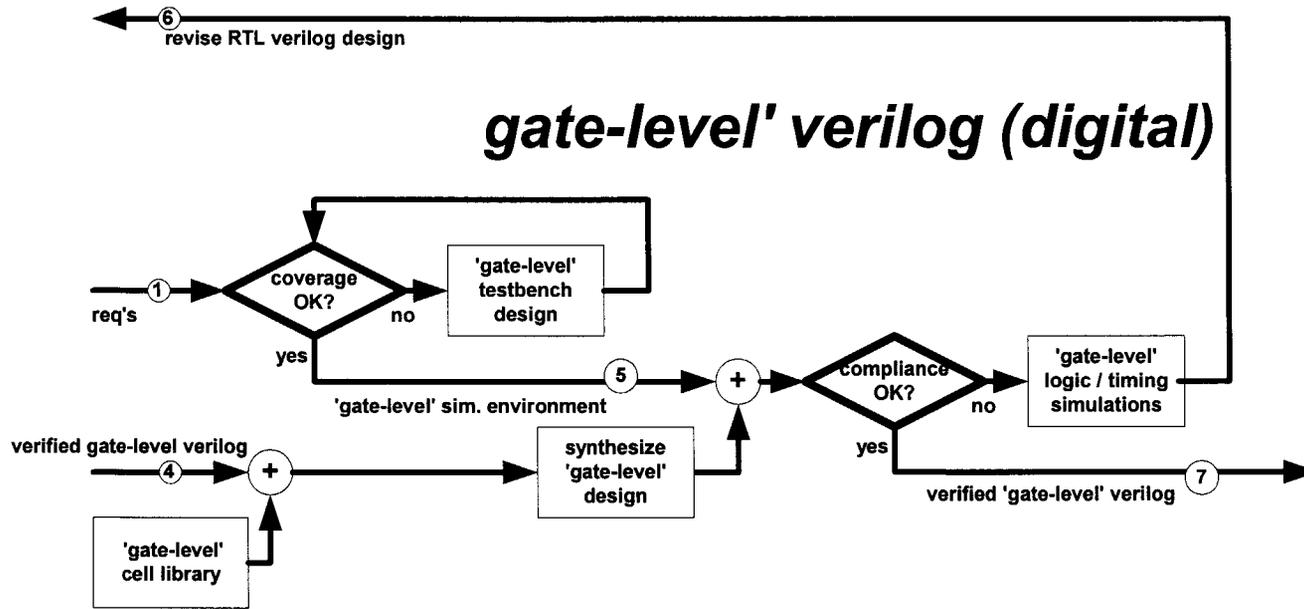
## **conclusions**

- **in addition to the traditional qualification steps three should be included at the front end:**
  - (a) specification quality review \***
  - (b) specification compliance review \***
  - (c) embedded software test coverage review \***
- **techniques for addressing SoC complexity, integrated analog circuits and embedded software have been identified**
- **the work flow for developing a SoC device is included in the appendix**

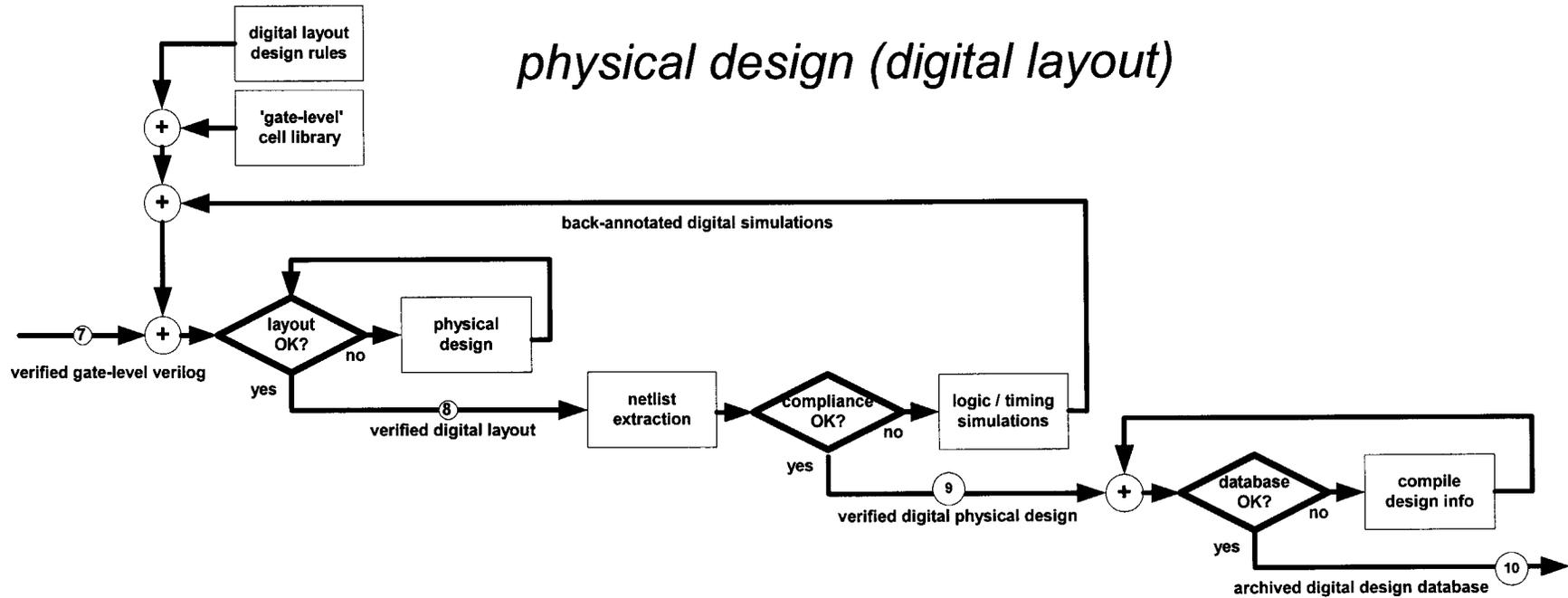
**Flight Qualifying SoC Devices**  
**appendix: SoC development work flow**

# Architectural Design

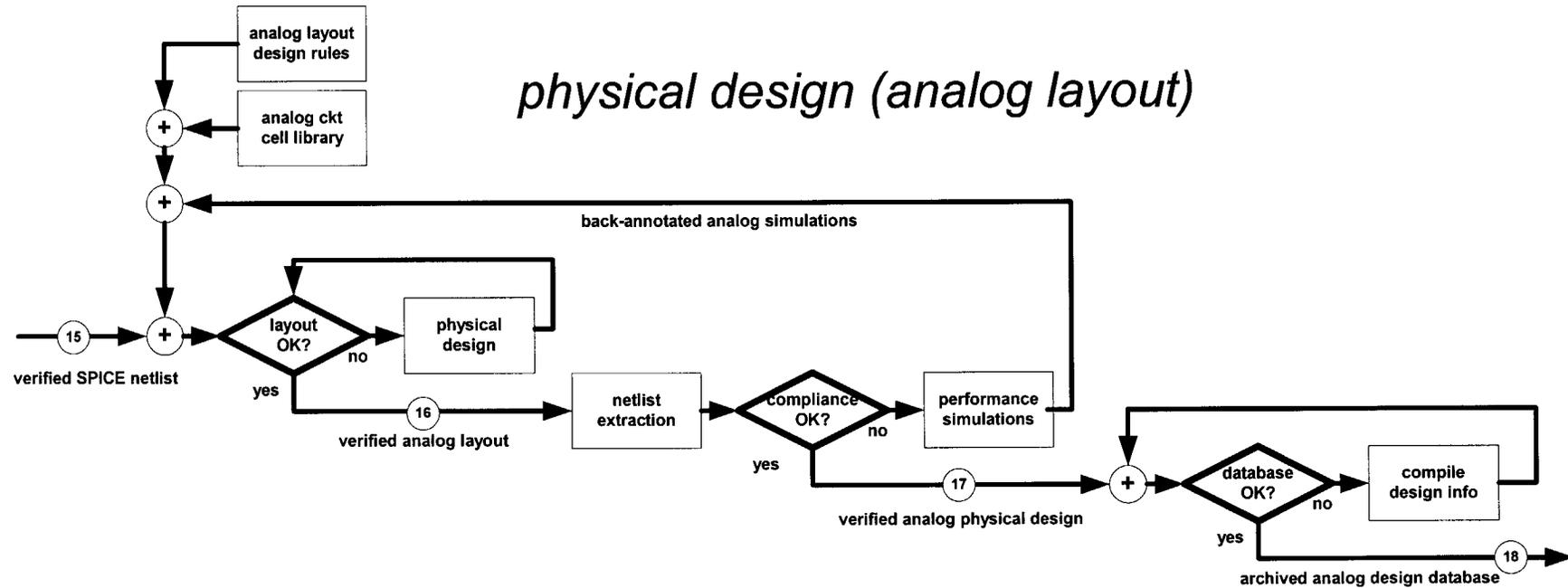




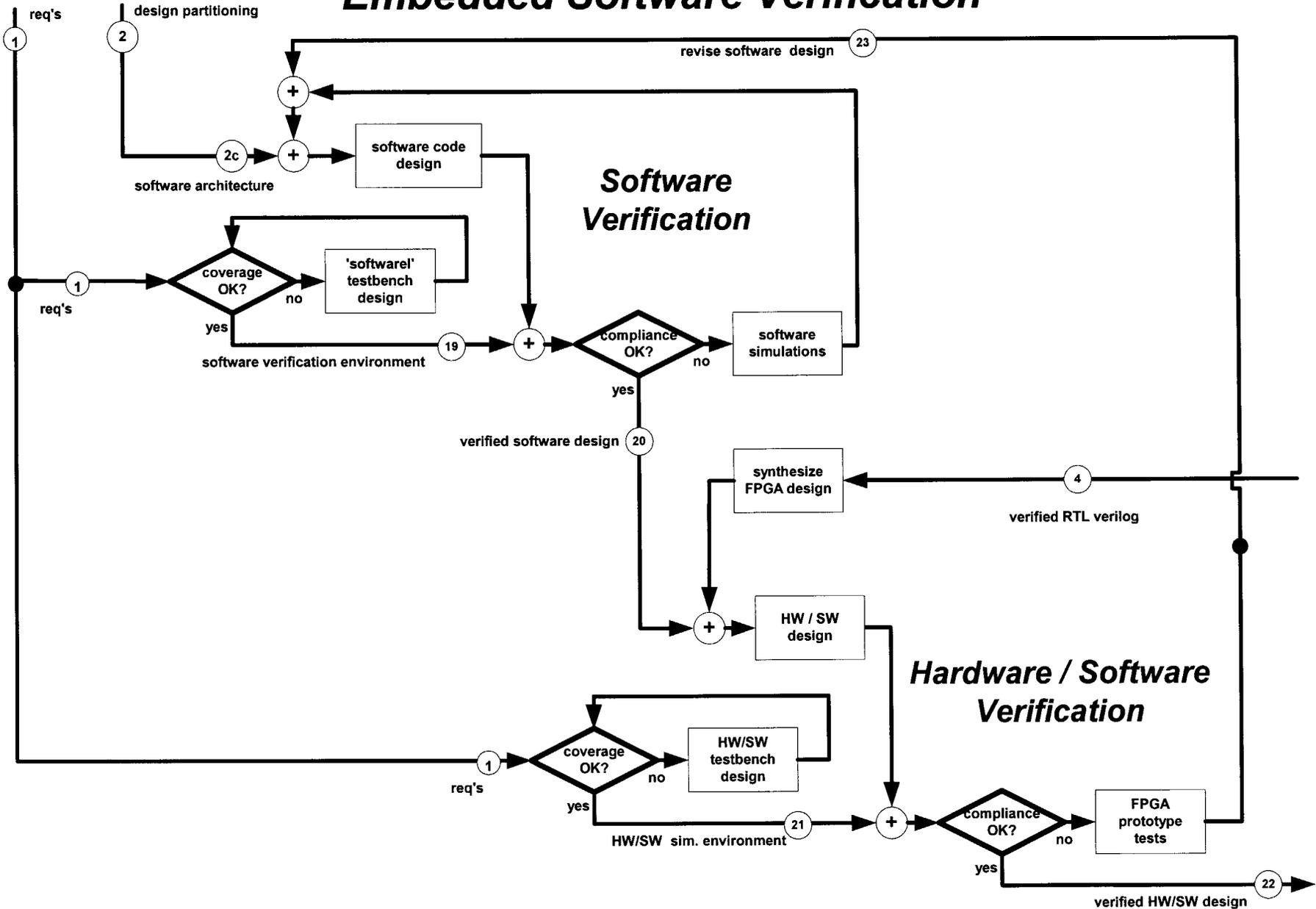
## physical design (digital layout)



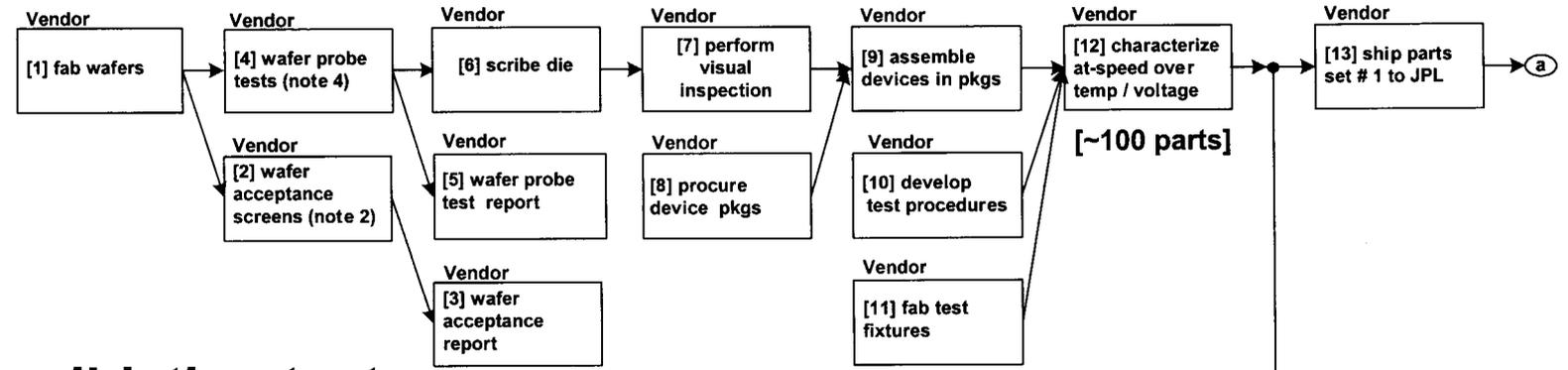
## physical design (analog layout)



# Embedded Software Verification

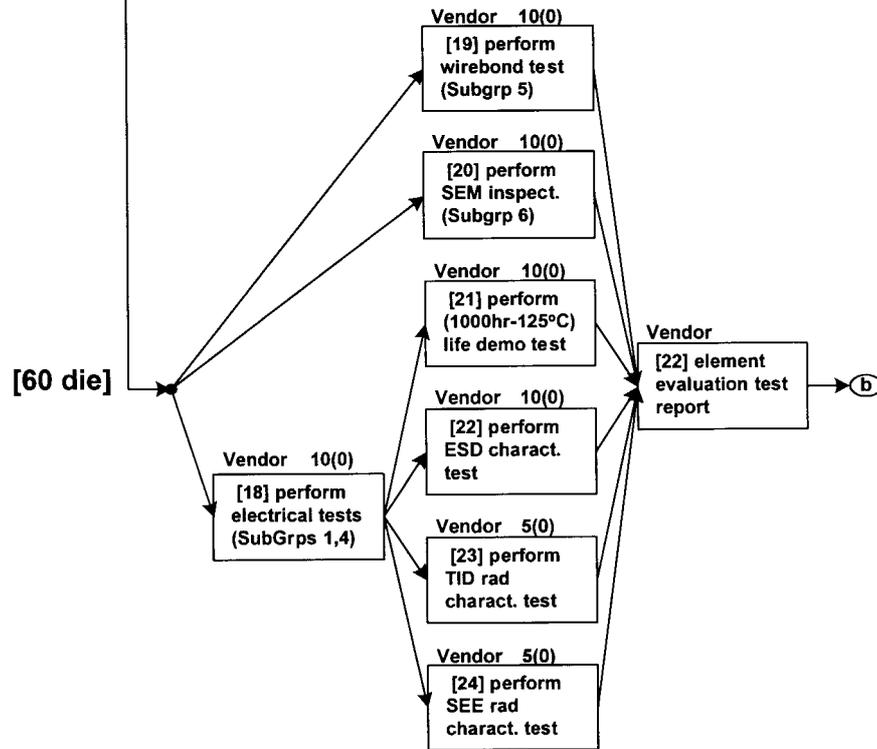


# Qual. Flow for Packaged Parts



validation tests

reliability tests



(2) wafer accept. tests include wafer structure, metallization and glassivation thickness and SEM