

2003 High Density Microelectronics Packaging Roadmap for Space Applications

Lissa Galbraith, PhD
Jet Propulsion Laboratory/NASA
California Institute of Technology
Pasadena, California
lissa.galbraith@jpl.nasa.gov

ABSTRACT

This Roadmap introduces current technologies, related strategic issues, and research recommendations for space applications. Transition from the traditional hierarchical network topology of circuit switching to a flat network topology for packet switching which is more conducive to data and Internet traffic is underway. Technology development required to support this includes single tunable lasers to replace multiple fixed wavelength lasers, ultrawide bandwidth fibers and optical amplifiers, and large capacity optical cross connects and routers for handling multi-terabit information rates on a single fiber. Also needed is the development of 13 GHz laser drivers and amplifiers, evolving 10 Gb/s to be as affordable as 2.5 Gb/s, defining standard metallic or fiber interfaces for 10 Gb/s, as well as further development of receivers and transmitters to use wave division multiplexing for 10 Gb/s traffic. The American Optoelectronics Industry Development Association forecasts that by 2005 chip computational power will reach 9,800 MIPS, and the smallest package feature size will be 0.1 micrometers or less. Satisfying these demands will require enhanced electronic performance with an associated improvement in packaging performance and better relief from thermal and mechanical stresses. Technical challenges and directions for high density interconnect microelectronics packaging also include understanding latent electromigration and dendritic growth, multilayer board hole wall wicking reliability issues, and characterization of reworkable underfill. NASA research with electronic noses, System-in-a-Package/System-on-a-Chip Technologies, and the identification of manufacturing processes, materials, quality, and reliability of embedded passive interconnects required for extreme temperature applications will be discussed. Technology challenges are described first for components, then the state of the art for high density materials and processes. Forecasts and recommendations for research direction are given for components, materials, and packaging.

Keywords

Roadmap, Packaging, Materials, Components, Predictions, Microelectronics

INTRODUCTION

The Roadmap is organized into three major sections: needs assessment, predictions, and recommendations for research direction. Radiation characterization and use of microelectronics in extreme environments is discussed within all three major topic areas. The first major section, needs assessment, is divided into packaging, materials and components. Predictions for microelectronics packaging are then presented in a series of tables. The predictions have been gathered from several industry roadmaps, journal articles, and discussions with experts. The predictions tables cover general research for microelectronics, material properties, laminate chip carrier design features, and thin film ceramics. The material properties table is divided into thermal, mechanical and substrate sections. The third major section, recommendations for research direction for space and other high reliability applications is discussed in six sections: commercial off the shelf components, reliability, extreme environments, optoelectronics/photronics, components, and materials. Many device types are discussed including ball grid arrays (BGA), chip scale packages (CSP), low temperature cofired ceramic components (LTCC), embedded passives, chip on board (COB), system on a chip, microelectromechanical systems (MEMS including optical applications), field-programmable gate arrays (FPGA), nonvolatile memory (NVM) components, complementary metal-oxide semiconductor (CMOS), plastic encapsulated microcircuits (PEM), and complementary heterostructure field effect transistors (CHFET).

NEEDS ASSESSMENT

Packaging

The need for greater functional density packaged in a smaller form factor is the most persistent challenge facing the microelectronics packaging research community. Feature size reductions are being introduced in silicon technology at an

accelerating rate. As a result there are more functions and Input/Outputs (I/O) within each Integrated Circuit (IC). In the year 2005 predictions are that ICs will have as many as 2000 I/Os⁴. Silicon on Insulator (SOI) components have established new design paradigms. Advanced chip carriers have migrated from ceramic to organic area array packages such as Ball Grid Arrays (BGAs), Chip Scale Packages (CSPs), and Flip Chips. In addition, the use of area array packages is driving the need for Printed Wiring Boards (PWBs) with microvias.

Use of plastic BGA packages (PBGA) continues to cause some problems. In addition to being moisture sensitive, the assembled package may have rework issues. The plastic BGA balls may be difficult to re-ball after collapse during rework. The PBGA package is also susceptible to warpage. Planarity defects cause the edges of the package to lift up, resulting in poor connection for the outer rows of balls. Larger PBGA packages are more susceptible to warpage than the smaller packages.

Materials

Finer particle sizes for eutectic solder is required to address the increased density and smaller component pitch. Lead free alloys will require further process optimization. No clean solder research should continue in the area of solder ball prevention and reduction of residue levels. Residue levels become more critical for finer pitch and array components. Solder mask research will be required to reduce solder balls and improve adhesion to underfill, encapsulants and conformal coatings. Standardization for fluxless systems is also needed.

Epoxies and Z-axis adhesives require faster curing times and more stable formulation. New failure prediction models are also needed for epoxies and Z-axis adhesives. The presence of moisture during the curing of epoxies can alter final properties including glass transition temperature (T_g), degree of cure, mechanical properties, the role of microvoids (near die metallizations), and the level of extractable ionics².

Softer unreinforced materials are becoming more common and are potentially more vulnerable to damage or distortion by testing. This could affect follow on processes. Microvia planarity could be altered affecting the soldering process. The need for higher conductivity conductors such as copper and silver is driving research into materials with lower loss dielectrics.

Process optimization is necessary for conformal coating for low Volatile Organic Compounds (VOC). Faster flowing and curing (snap cure) underfill formulation will be required for fine pitch arrays. Underfill match to interconnect Coefficient of Thermal Expansion (CTE) and combining flux and underfill also need further research.

Components

Increasingly miniaturized devices require higher power, even with operation at lower voltages. Research needs include development of attachment reliability modeling for array packages, including discrete arrays for extreme environment use. Efficiency of translation for converting different grid pitches from test bed to device or board I/O pattern is a looming problem. Test beds are commonly on 0.100" centers but devices are now being created with a variety of different pitches. Some features must be protected from damage and require nearby test points to be used rather than direct test. This presents a risk in that the link between the test point and the actual contact is potentially open and may require verification by other means (such as optical).

Moisture absorbed during field life can interact with ionic material contained within a plastic package. The level of ionic content strongly influences failure rates. Lower ionic content correlates strongly with higher reliability in humid environments. The ionic materials are present either as residues from IC fabrication or assembly, or can come from the constituent materials contained in encapsulants, die adhesives, or laminate substrates. The failure mechanisms include both corrosion of aluminum bond pads or IC circuit lines, and degradation of gold-aluminum interfaces in wirebonds. Power cycling during field life is another factor effecting moisture desorption and resorption².

Table 1. Ceramic Technology Trends⁴

Current Technology	Trend
Dielectric Paste	Tape/Low Temperature Cofired Ceramics (LTCC)
Screen Printed Dielectric/Vias	Dielectrics with Photopatterned or Imaged Vias Tape Dielectrics with Photopatterned Vias
Screen Printed Conductors	Photopatterned Conductors
Surface Passive Components	Buried Passive Resisitors Inductors Capacitors (RLC) Components
Loss Tangent < 10 ⁻³	Loss Tangent < 10 ⁻⁴

Table 2. Critical Design Parameters for Direct Chip Attach BGA Substrate Routing (µm)¹

Die Bump Pitch	200	180	150	130	100	50
Bump Diameter	100	90	70	60	40	20
Solder Pad Diameter	100	70	60	50	40	18
Die Bump Pitch	200	180	150	130	100	50
Via Diameter	50	40	35	30	25	10
Via Pad Diameter	100	75	60	50	40	18
Line Width (1 line/channel)	50	35	30	25	20	10
Line Width (2 lines/channel)	30	22	18	15	12	6

PREDICTIONS

The following tables summarize predictions accumulated from several industry roadmaps, journal articles and discussions with microelectronics packaging experts.^{2,3,4,5,6}

Table 3. General Predictions for Microelectronics Research for Space Applications

Metric	2004-2005	2006-2010
Extreme Environment Chip Rise Time (Nanoseconds)	1.5	0.8
On Chip Frequency (MHz)	300	350
Minimum Device Voltage (Volts)	2.5	2
Thermal Dissipation (Watts Avg/Max)	10/40	16/70

Table 3, continued

Metric	2004-2005	2006-2010
Usable Board Area (cm ²)	130	125
Thickness (mm)	1.5	1.52
Layer Count (Average)	4	2
Line Width/Space (Minimum Internal µm)	100/100	75/75
Minimum Microvia Diameter-Buried or Blind (µm)	125	N/A
Maximum I/O Count	512	760
Total Number of Components	300	290
Maximum Total Number of Array Components	42	52

Table 4. Predictions for Research in Material Properties

Metric	2004-2005	2006-2010
THERMAL		
T _g	150-260	170-260
x-y access CTE	10-16	8-16
Z access CTE (ppm below T _g 30-260 °C)	60-85	50-75
MECHANICAL		
Inner Layer (1oz.)	1.1-1.4	0.7-1.1
Outer Layer (½ oz.)	0.9-1.3	0.6-1.0
SUBSTRATE		
Dimensional Stability Variation after Etch (µm/cm)	< 2	1
Glass Reinforcement Weight Tolerance (%)	2-3	1-2
Resin Content Tolerance (%)	2	1-2
Single Ply Reinforcement (% of Multilayer)	15-30	25-50

Table 5. Predictions for Research for Laminate Chip Carrier Design Features

Metric	2004-2005	2006-2010
Line Width (µm)	25-50	12.5-25
Board Thickness (mm)	0.2	< 0.2
BGA Land Pitch (mm)	0.8	0.65
Device I/O	>1000	2000+

Table 6. Predictions for Research in Thin Film Ceramics

Metric	2004-2005	2006-2010
Size Reduction/Increased Density: (μm)		
via size	50	25
via pitch	150	75
Trace Geometry	50	25
Trace Pitch	50	30
Clock/Frequency Increase (GHz)	30	80
Intimate Electromechanical Interface (High Temp Performance $^{\circ}\text{C}$)	180	200

Recommendations For Research Direction For Space And Other High Reliability Applications

1. Commercial Off The Shelf (COTS)

COTS devices are of great interest to NASA because of their wide availability and cost. The use of COTS for space applications requires greater evaluation of reliability, life span and use in extreme environments.

- * MicroElectroMechanical Systems (MEMS) sensor packaging reliability for COTS components
- * Quality and reliability of COTS MEMS sensors and accelerometers
- * Reliability of COTS electronic nose packaging
- * Reliability of COTS PEMs packaging

2. Reliability

The high reliability testing required of space electronic packaging is shared by few other applications with the obvious exception of components used in medical electronics. The high cost of retrieval after deployment dictates the need for additional testing to ensure this high reliability.

- * Study of ultra fine conductors and contacts
- * COB reliability
- * Value of post programming burn-in for FPGA
- * Reliability of laser arrays
- * High power diode laser arrays
- * Thin, low/high k dielectrics
- * Radiation effects in new device dielectrics
- * Embedded passive devices
- * Radiation characterization of ultracapacitors
- * NVM devices
- * Multilayer board hole wall wicking

3. Extreme Environments

Space applications for electronics require that the electronics endure extremely low and high temperature environments. Electronics in launch

vehicles endure extremely high temperature at launch and extremely low temperature once in space.

- * Interconnect reliability of cold electronics
- * Packaging of high temperature silicon carbide (SiC) based electronics
- * MEMS pressure sensors reliability in extreme environments
- * Radiation qualification of components for extreme environments

4. Optoelectronics/Photonics

Technology development supporting the transition from a hierarchical network topology of circuit switching to a more flat network topology for packet switching includes single tunable lasers, ultrawide bandwidth fibers and amplifiers, and large capacity optical cross connects and routers for handling multi-terabit information rates on a single fiber. Optoelectronics are particularly effective in meeting the size and weight constraints of space applications for electronics.

- * Optoelectronic and photonic device reliability
- * Characterization of optical fiber cables for space applications
- * Photonic devices and data link radiation characterization
- * Radiation test guidelines for optocouplers

5. Components

The demand for greater functional density packaged in a smaller form factor provides the greatest impetus for microelectronics packaging research for space applications. The extremely high cost per kilogram for escaping Earth's gravitational pull requires minimal weight and size for space vehicle electronics.

- * Evaluation of Silicon on Insulator (SOI) processes for mixed signal ASICs
- * Hermeticity effects on GaAs and InP Devices
- * Radiation characterization of CMOS microelectronics
- * Radiation testing of SiGe high speed devices
- * PEMs qualification methods
- * Complementary Gallium Arsenide (CGaAs) CHFET component reliability
- * High density FPGA high reliability qualification
- * MEMS and MOEMS for Radio Frequency (RF) applications
- * MEMS and MOEMS interconnect tribology
- * System-on-a-chip ASIC design for reliability
- * Compound semiconductor/microwave device technologies
- * SiGe/Si Heterojunction Bipolar Transistor (HBT) microwave device reliability

6. Materials

Materials research underlies all other microelectronics research. The list that follows is short because materials research is embedded in all of the research topics shown above.

- * Reworkable underfill characterization and reliability
- * Copper metallization reliability
- * Latent electromigration and dendritic growth

ACKNOWLEDGMENTS

The research described in this paper was performed at the Jet Propulsion Laboratory, California Institute of Technology, under a contract with the National Aeronautics and Space Administration (NASA). The author wishes to thank several Jet Propulsion Laboratory research engineers for their gracious sharing of their expertise: Stephen Bolin, Saverio D'Agostino, Phillip Zulueta, Dr. Rajeshuni Ramesham, and Dr. Reza Ghaffarian.

REFERENCES

1. Fu, Chia-Yu, and Ring-Fong Huang, "BGA Reliability of Multilayer Ceramic Integrated Circuit (MCIC) Devices", *IMAPS International Journal of Microcircuits & Electronic Packaging*, Volume 23, Number 4, Fourth Quarter, 2000
2. Hagge, John K, "ROBOCOTS: A Program to Assure Robust Packaging of Commercial-Off-The-Shelf (COTS) Integrated Circuits", *IMAPS International Journal of Microcircuits & Electronic Packaging*, Volume 23, Number 4, Fourth Quarter, 2000
3. International Roadmap Committee (IRC) and the International Technology Working Groups, *ITRS International Technology Roadmap for Semiconductors 2000 Update*, July 2000
4. IPC, *National Technology Roadmap for Electronic Interconnections 2000/2001*
5. Irvin, Robert, "Designing an Optoelectronic Package", *Advancing Microelectronics*, January/February 2002
6. W. Simon, R. Kulke, A. Wien, I. Wolff, S. Baker, R. Powell, and M. Harrison, "Design of Passive Components for K-Band Communication Modules in LTCC Environment", *IMAPS International Journal of Microcircuits & Electronic Packaging*, Volume 23, Number 1, First Quarter 2000