

*Paper is cleared already  
CL#01-2137*

# **Ku-Band Receiver and Transmitter for Breadboard DSP Scatterometer**

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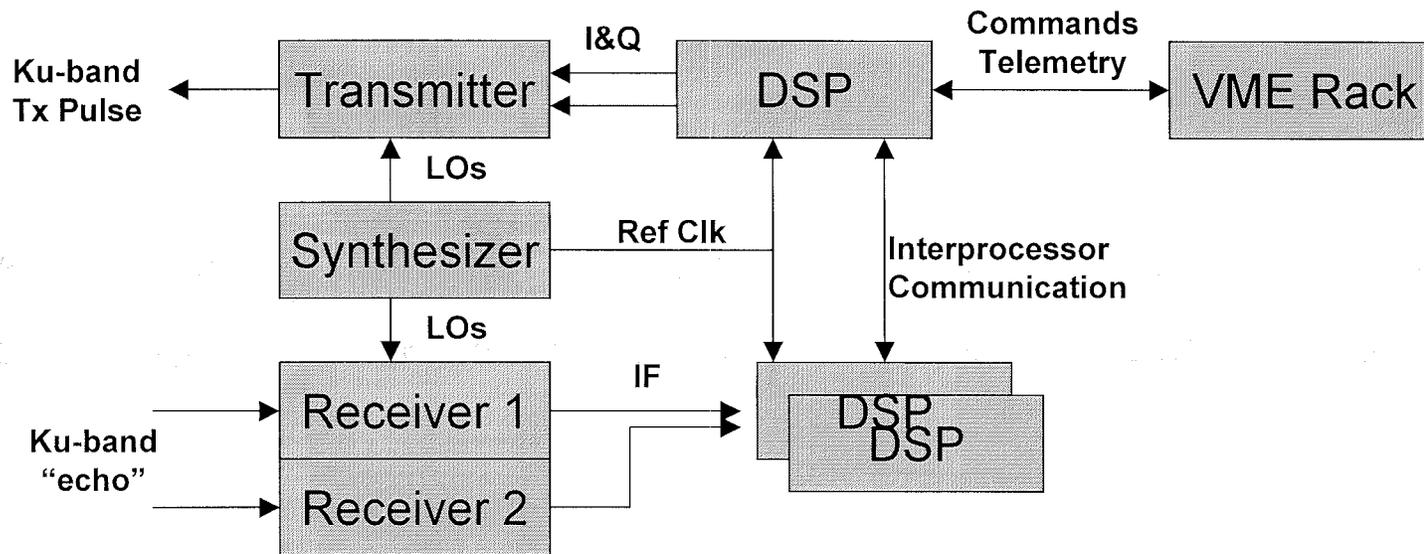
Jet Propulsion Laboratory



# DSP Scatterometer Breadboard

- Goals
  - Build on last year's evaluation of MMIC parts for receiver
  - Demonstrate feasibility of DSP based scatterometer using currently available space qualified hardware
  - Identify subsystem integration issues early by building end-to-end radar breadboard
  - Bring historically separate development areas together
    - Avionics software and hardware
    - Signal processing software
    - RF design

# DSP Scatterometer Breadboard Block Diagram



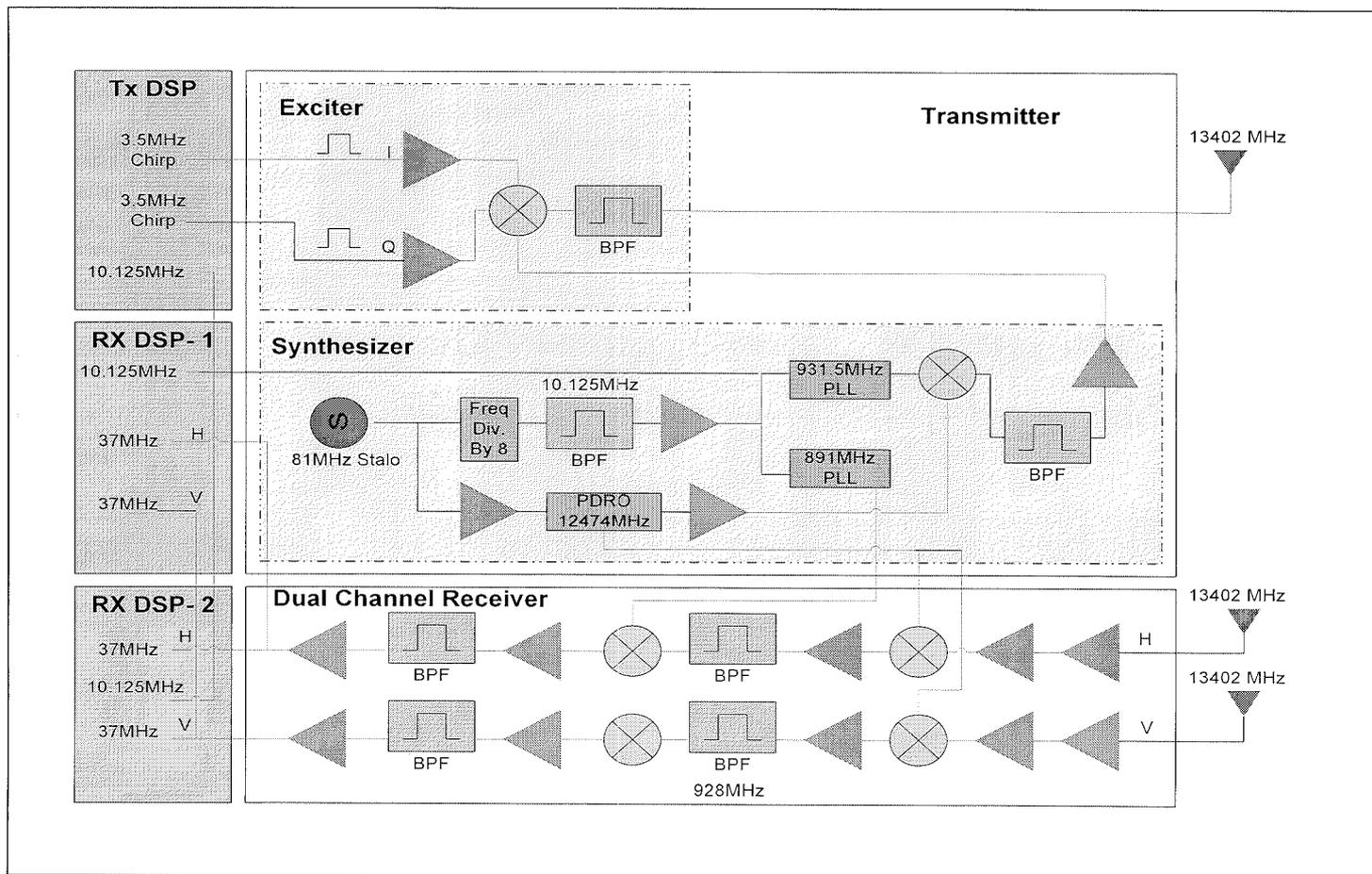
# RF Subsystem Requirements

- Patterned after Seawinds flight requirements with additions to cover possible future missions
  - polarimetry, flexible spacecraft platform
  - 13.402 GHz (Ku-band) input and output
  - 37 MHz Receiver outputs
  - 3.5 MHz I/Q Transmit Waveform input
  - Ref Osc Outputs for data converter and processor clocks
  - Noise figure approx 4.5-5 dB
  - Tx Power - few mW (in real radar, drives a TWTA)
  - Use only parts or modules available in flight qualified versions (MMICs, DSPs, oscillators, etc.)

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# RF Block Diagram



# Synthesizer/Exciter

- Reference Oscillator
  - Retuned to 81 MHz from from 1999 design (76 MHz)
  - Divide by 8 to generate frequency reference for digital part of system
- Local Oscillators
  - PLL brick for LO at 12.474 GHz
  - Commercial PLL for LO at 891 MHz and 928 MHz
  - Phase noise and lockup performance not an issue for breadboard (yet)
- I/Q mixer at Ku-band
  - Poor image rejection prompts change to I/Q mixer at 928 MHz IF



# Dual Channel Receiver

- Designed using MMIC front end evaluated in 2000
- Ceramic IF filters from cellular application
- Front end NF 4 dB
  - good enough for demonstration
- 37 MHz final output
  - offset conversion in A/D converter to “baseband”

# Integration Issues Encountered

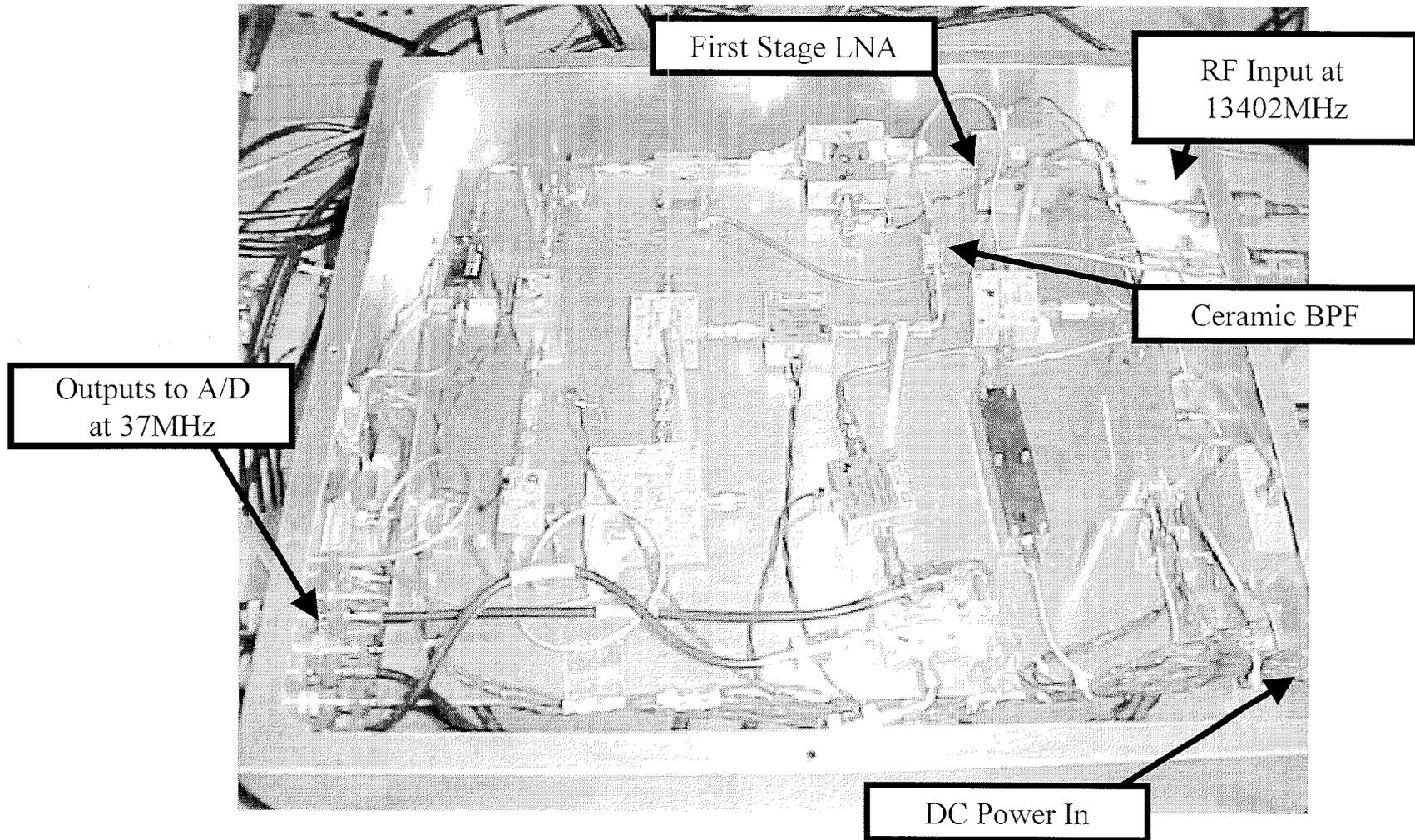
- I/Q drive from DACs
  - DAC swings -1 to 0 V
  - Choice of 3.5 MHz center frequency very close to 5 MSPS or 10 MSPS
    - Driven by original DSP design
    - 5 section Elliptic filter designed for DAC output with null at sample rate
  - Buffer amplifiers to increase drive to I/Q mixer
  - Change in exciter design (Ku vs IF modulation)
    - I/Q imbalance requires too high performance output filter

# Integration Issues Encountered

- Change in DSP processor clock requirements
  - forced change in STALO distribution frequency
- Original design - Output distributed at 81 MHz
  - DSP at 20.5, using on-chip divide by 2, with external divide by 2 from 81 MHz
- New Design - Output distributed at 10.125 MHz
  - DSP at 15.1875, DSP requires 4x (60.75 MHz) clock synthesizer in DSP subassembly
  - Synthesis done by HP 8110A pulse generator in breadboard - IC clock generator designed but not tested.



# Breadboard Receiver



# Breadboard Transmitter/Synthesizer

