RAD750 System Flight Computer

Anne Cady
BAE SYSTEMS
"Silicon to Systems"

Our core processes and technologies enable a wide range of advanced systems
91 satellites currently on orbit with 287 single board computers*

* As of January, 2002

Cassini GVSC processor

SBIRS Low/Orbview RAD6000

Over 500 flight boards delivered or ordered for new launches through 2006

CCP drop in tray (GVSC)

VME 6U RAD6000 board *

* as used on FHLP

Our processors have been the standard in space for many years, with millions of hours of flawless operation in a variety of applications
Three generations of radiation hardened microprocessors

The RAD750 represents our third generation product, with architectural and technological enhancements that improve power/performance.
SEE enhancements made to the RAD750™

- OTS's (Data Flow)
  - Harden latches and clock splitters
  - Replace dynamic logic with static equivalents
  - Design circuits to minimize injected pulses
  - Replace low Vt devices

- Custom Blocks
  - Harden RAM cells, sense amps, and decoders
  - Harden latches and clocks
  - Harden PLL and add temperature compensation
  - Replace dynamic logic with static equivalents
  - Design circuits to minimize injected pulses
  - Replace low Vt devices

Customization of the PowerPC 750 to improve SEE hardness required replacement of the circuitry while maintaining identical logic function
Radiation Results for RAD750™

**Prompt Dose**

**Test Specifics**
- 850 pulses, widths 20-60 ns
- Dynamic FFT test at 33, 116, 133 MHz

**Test Results**
- >1E9 rad(Si)/s at 133 MHz

**Total Ionizing Dose**

**Test Specifics**
- 73 Rad(Si)/s and 25°C
- Static bias in Gamma Cell

**Test Results:**
- >200 Krad(Si)

RAD750 is flight screened and available for delivery today

Witnessed by General Dynamics + NRL Independent Consultant
# RAD750™ specifications

<table>
<thead>
<tr>
<th>Specifications</th>
<th>Details</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Processor Speed</strong></td>
<td>110 to 133 MHz</td>
</tr>
<tr>
<td><strong>Process Technology</strong></td>
<td>0.25 um (0.18 um Left) CMOS, 6 levels of metal</td>
</tr>
<tr>
<td><strong>Die Size</strong></td>
<td>10.4 mm. by 12.5 mm.</td>
</tr>
<tr>
<td><strong>RAD750 Performance</strong></td>
<td></td>
</tr>
<tr>
<td>without L2 (est)</td>
<td>6.5 SPECint95 3.9 SPECfp95 @ 150 MHz.</td>
</tr>
<tr>
<td>with 1MB L2 (est)</td>
<td>7.0 SPECint95 4.7 SPECfp95 @ 150 MHz.</td>
</tr>
<tr>
<td><strong>Signal I/O</strong></td>
<td>266 (including L2 port)</td>
</tr>
<tr>
<td><strong>Power Supply</strong></td>
<td>2.5 V +/- 5% core</td>
</tr>
<tr>
<td></td>
<td>2.5 or 3.3 V +/- 10% I/O</td>
</tr>
<tr>
<td><strong>Power Dissipation</strong></td>
<td>5.0 watts at 133 MHz, 2.5V</td>
</tr>
<tr>
<td><strong>Temperature Range</strong></td>
<td>-55°C to +125°C</td>
</tr>
<tr>
<td><strong>Packaging</strong></td>
<td>25.0 mm. by 25.0 mm. by 6.22 mm. 360 pin Column Grid Array (CGA)</td>
</tr>
<tr>
<td><strong>Mass</strong></td>
<td>9.0 grams</td>
</tr>
<tr>
<td><strong>Radiation Hardness</strong></td>
<td>Total Ionizing Dose: 200 Krad (Si)</td>
</tr>
<tr>
<td></td>
<td>SEU: 1E-10 upsets / bit-day (W.C. 90% GEO)</td>
</tr>
<tr>
<td></td>
<td>Latchup: Immune</td>
</tr>
<tr>
<td><strong>Mean Time Between Failures (MTBF)</strong></td>
<td>&gt; 4.3M hours</td>
</tr>
</tbody>
</table>

## Data Cache

- **Data Tags**
- **L2 Cache Tags**
- **MMU**
- **Load Store Unit**
- **Floating Point Unit**
- **Instruction Sequencer**
- **6xx Bus Interface and Cache Control**
- **Instruction Tags**

## Instruction Cache
X2000 System Flight Computer Board

- **132 MHz RAD750 CPU**
  - 240 MIPS Dhrystone Performance

- **128MB SDRAM**
  - Uses 16Mx4 (64Mb) SDRAM packaged in 4-high stacks

- **256KB SUROM**

- **Power PCI Bridge chip**
  - Memory I/F, PCI, UART, JTAG, Timers, Programmable Interrupts/Discretes, etc

- **Conduction Cooled, 3U CompactPCI format**

- **3.3V (+/- 10%) is only required voltage**
  - Card power <10W (over 24 MIPS/Watt)

- **Qual testing complete (Vibe, Pyro, Thermal Life)**

- **Over 50 cards ordered or delivered. Customers include:**
  - JPL: Europa Orbiter, Deep Impact, ST3, and Mars
  - BAE SYSTEMS - Johnson City: Bold Strike Force
  - Also Lockheed Martin, Spectrum Astro, NRL, LaRC, Raytheon, ITT and others

Flight Unit Configuration
The reusable logic core architecture in the Power PCI provides for future enhancements as well as future product variations.
Power PCI ASIC specifications

**Specifications**

<table>
<thead>
<tr>
<th>Specification</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Clock Speed</strong></td>
<td>33 MHz</td>
</tr>
<tr>
<td><strong>Process Technology</strong></td>
<td>0.50 μm Leff CMOS, 5 levels of metal</td>
</tr>
<tr>
<td><strong>Die Size</strong></td>
<td>12.7 mm. by 12.7 mm.</td>
</tr>
<tr>
<td><strong>Cells / Gates / Latches</strong></td>
<td>926K / 700K / 26K</td>
</tr>
<tr>
<td><strong>PCI Peak Bandwidth</strong></td>
<td>130 MB/s write, 90 MB/s read</td>
</tr>
<tr>
<td><strong>Signal I/O</strong></td>
<td>456 (+ test)</td>
</tr>
<tr>
<td><strong>Power Supply</strong></td>
<td>3.3 V ± / - 10% core and I/O</td>
</tr>
<tr>
<td><strong>Power Dissipation</strong></td>
<td>1.5 W</td>
</tr>
<tr>
<td><strong>Temperature Range</strong></td>
<td>-55°C to +125°C</td>
</tr>
<tr>
<td><strong>Packaging</strong></td>
<td>32.5 mm. By 32.5 mm. By 6.22 mm. 624 pin Column Grid Array (CGA) with flip-chip C4 mount</td>
</tr>
<tr>
<td><strong>Radiation Hardness</strong></td>
<td>Total Ionizing Dose: &gt;1Mrad (Si) SEU: &lt;1E-10 upsets / bit-day (W.C. 90% GEO) Latchup: Immune</td>
</tr>
<tr>
<td><strong>Mass</strong></td>
<td>14.5 grams</td>
</tr>
</tbody>
</table>
SDRAM Packaging

SDRAM (16M x 4) → Staktek will stack in 2-high 16M x 8 SDRAM Stack

Test and burn-in of Stacks at BAE SYSTEMS Manassas

Stacks packaged on double-sided module

Component Test → Assembly

16M x 16 → Mil-Screen → Module Test
Design Status

- **Power PCI design, fabrication and testing completed**
  - Initial Power PCI Design completed and delivered to customers 1Q2001
  - 2nd version (minor backend changes) completed and delivered to customers on boards 4Q2001
  - Flight part screening complete and parts in stock

- **Board design completed and tested**
  - First SFC (Engineering Model) delivered to JPL in December 2000
  - Qualification Testing completed in September 2001
  - Six SFC Engineering units retrofitted with 2nd version Power PCI delivered to JPL in December 2001-January 2002

- **Flight Model deliveries scheduled for Late March/Early April 2002**

- **Work underway on Enhanced SFC**
  - 66MHz Enhanced Power PCI ASIC release to manufacturing expected in June 2002 (6 months ahead of schedule)
  - Enhanced SFC deliveries planned for December 2002-January 2003 (6 months ahead of schedule)
RAD750™ development software and RAD6000™ migration

Many RAD750 operating systems and compilers are available, and software already written for the RAD6000 is easily migrated to the RAD750.
RAD750™ software development environment

Software Development System
- Pentium personal computer
- Windows NT Operating System
- Ethernet connection to RAD750
- Corellis JTAG interface
- RAD750 or COTS PowerPC Board

WindRiver VxWorks OS
- High performance multi-tasking kernel
- Networking capability
- Device independent I/O
- Dynamic load of user programs
- Highly configurable execution environment
- “Tornado” Software development and debug tools

BAE SYSTEMS Supplied Software
Board Support Package (BSP)
- VxWorks compatible
I/O device drivers
Start-Up ROM (SUROM)
- System “Reset handler”
- On-board diagnostics
  - CPU and Power PC1 self-test
  - Memory test
- Bootstrap image load into RAM
- Test and initialize board hardware
- Fault recovery during restart

Green Hill Multi and GNU Tools
- Optimized C, C++, Ada compilers
- Source level debugger
- Mixed language integration
- Version control system
- Program builder
- Editor

A complete environment, based on our RAD6000 experience, eases RAD750 software development
Processor Roadmap 2001-2005

Processor:
- July 2002: RAD750 (133 MHz)
- Jan 2003: Possibly Funded
- July 2004: Currently Unfunded
- Jan 2005:

ASICs:
- July 2002:
- Jan 2003:
- July 2004:
- Jan 2005:

Memory:
- July 2002: C-RAM memory devices
- Jan 2003: 64K C-RAM test site
- July 2004:
- Jan 2005:

Legend:
- In Production
- In Hardware
- In Development
- Planned
- Possibly Funded
- Currently Unfunded

2/13/02
Enhanced Power PCI - Under Development

- Larger Instr. cache
- Mult. and Shift Instr.
- Branch prediction
- Execution under LD & ST instructions
- Allow reg writes while disabled
- Increase to 24 GPR's

- Reduced Latency
- PCI-Mem, Mem-PCI and PCI-PCI Transfers
- Temp. Data Storage for I/O and EMC
- Reduced Latency • 256M SDRAM

Enhanced Bridge
- Development underway under JPL funding
- Migration to R-25
  - 3.3V I/O Operation
  - 2.5V Core
- 66 MHz I/F Operation
  - Oscillator
  - 6xx Bus
  - Memory bus
- Errata Fixes
- Performance Enhancements
- Pin Compatible with Current Design

Legend:
- Unchanged
- Enhanced
- New

The Power PCI / 66 adds on-board DMA and scratchpad memory in addition to improved performance in many existing functions
L2 Cache Design Approach

- Proof of Concept
  - Use L2 Tag as Baseline SRAM Core
  - Simulate L2 Cache HLM with 750 HLM
  - Translate into Logic and Optimize
  - Architectural Tradeoffs, Circuit Design and Simulation
  - Chip Layout
  - Parasitic Extraction and Design Verification (LVS&DRC)
  - Postprocessing, Masks, and Fab
  - Initial Electrical Test

- Characterization & Radiation Testing
  - Electrical Characterization
  - SEU Test
  - Total Dose Test

- Release to Production
  - Production Design Enhancements
  - Production Test Program
  - 24 Month Overall Schedule

2/13/02
RAD750 L2 Cache CGA MCM

- **42.5 mm CGA Module Contains:**
  - 1 RAD750
  - 2 L2 Cache Memory (1MB total)
  - RAD750 package capacitors

- **CGA Design Features**
  - Pin for Pin with existing RAD750 package
  - Proven Design and Process
  - Builds on current X2000 CGA family
    - 25mm CGA used for RAD750
    - 32mm CGA used for Power PCI

- **Task Elements**
  - Development & Implementation (Leverage L2 Tag design)
  - Test and Screen
  - Qualification & Board Evaluation

Leveraging the dedicated L2 cache port on the RAD750 with radiation hardened memory chips will further extend the processor’s performance.
RAD750 with L2 Cache 3U Board

- Multi-chip package approach with the RAD750 and two L2 cache chips placed in a 42mm ceramic column grid array package.
- Printed wiring board stack-up, wire size and spacing rules will be the same as those used on X2000 SFC design.
- No buried or blind vias.
- Oscillator moved to back side of board.
- EEPROM parts rearranged on board.

The MCM will fit on a CompactPCI 3U board, allowing "drop-in" upgrades.
Memory options becoming limited

<table>
<thead>
<tr>
<th></th>
<th>Speed</th>
<th>Power</th>
<th>Cost</th>
<th>Cycle Life</th>
<th>Non-Volatile</th>
</tr>
</thead>
<tbody>
<tr>
<td>SRAM</td>
<td>Very High</td>
<td>High</td>
<td>High</td>
<td>Very High</td>
<td>No</td>
</tr>
<tr>
<td>DRAM</td>
<td>High</td>
<td>Low</td>
<td>Very Low</td>
<td>Very High</td>
<td>No</td>
</tr>
<tr>
<td>FLASH</td>
<td>Low</td>
<td>Very Low</td>
<td>Low</td>
<td>Low</td>
<td>Yes</td>
</tr>
<tr>
<td>OUM</td>
<td>High</td>
<td>Low</td>
<td>Very Low</td>
<td>High</td>
<td>Yes</td>
</tr>
</tbody>
</table>

- DRAM (SDRAM) - Volatile, significant power, Low radiation tolerance-susceptible to stuck bits
- SRAM - Lower density, high power, Volatile
- Flash - Limited cycle life, low speed

- **Ovonic Unified Memory (Chalcogenide) offers a solution - high speed, low power, high cycle life, non-volatile and radiation hardened to substrate limit**
Chalcogenide-Based Non-Volatile Memory Technology

- **Chalcogenides:**
  - alloys with at least one Group VI element that can exist in either of two stable states

  **Amorphous State**
  - Low reflectance & conductance

  **Polycrystalline State**
  - High reflectance & conductance

- **To change states:**
  - to set (amorphize), melt alloy and remove heat
  - to reset (crystallize), raise to a lower temperature and then remove heat

- **To Read:**
  - apply low voltage. Electric current determined by resistance of memory element
Current Status

• **Phase 0A Complete**
  - Memory cell demonstrated with good uniformity, endurance, write/read power

• **Phase 0B Started**
  - Design and fabricate test chips which:
    - Integrate memory cell with CMOS transistors
      - Target device sizes support 16Mb arrays in 0.5 micron CMOS
    - Demonstrate write & read peripheral circuitry
  - Test chips focused on integrating all elements by end of Phase 0B (64kb arrays)

• **Recent Progress**
  - 5x reduction in write current (now ~1.0mA)
  - CMOS test chip released to fabrication, results by Q1 2002
  - Array test chip in detailed designed, release projected Feb. 2002
4M/16M Chalcogenide NVRAM

- First product driven by market needs
- Built in 0.25 micron CMOS Manassas foundry
- 3.3V / 2.5V power supply
- Cycle time: \( \leq 50 \text{ns} \)
- Write cycle endurance: \( > 10^{10} \)
- Read cycle endurance: unlimited
- Power:
  - Operate \( \leq 10 \text{ mW/MHz} \)
  - Standby \( \leq 50 \mu \text{W} \)
Supporting Charts
SFC Qualification Test Flow - Completed
## SFC Vibration Levels

<table>
<thead>
<tr>
<th>Frequency (Hz)</th>
<th>Design/Qual, PF Test</th>
<th>FA Test</th>
</tr>
</thead>
<tbody>
<tr>
<td>20-50</td>
<td>+9dB/Oct.</td>
<td>+9dB/Oct</td>
</tr>
<tr>
<td>50-250</td>
<td>0.20 g²/Hz</td>
<td>0.10 g²/Hz</td>
</tr>
<tr>
<td>350-1000</td>
<td>0.10 g²/Hz</td>
<td>.05 g²/Hz</td>
</tr>
<tr>
<td>Overall</td>
<td>12.3 grms</td>
<td>8.7 grms</td>
</tr>
</tbody>
</table>

Duration: 3 minutes in each of 3 orthogonal axes

**Random Vibration Requirements**

<table>
<thead>
<tr>
<th>Frequency (Hz)</th>
<th>Design/Qual, PF Test</th>
<th>FA Test</th>
</tr>
</thead>
<tbody>
<tr>
<td>20</td>
<td>1.29 g²/Hz</td>
<td>0.647 g²/Hz</td>
</tr>
<tr>
<td>50-500</td>
<td>20.0 g²/Hz</td>
<td>10.0 g²/Hz</td>
</tr>
<tr>
<td>600-1000</td>
<td>10.0 g²/Hz</td>
<td>5.01 g²/Hz</td>
</tr>
<tr>
<td>2000</td>
<td>0.630 g²/Hz</td>
<td>0.316 g²/Hz</td>
</tr>
</tbody>
</table>

**Random Vibration Response Limits**
Pyroshock Qualification Levels

Pyroshock Design and Test Requirements
Use of RAD750™ vs. redundant commercial processors in space

**Software effort and overhead**
- **Effort**
  - Must code "upset checking" routine as well as split application code to allow for regular checking
  - Must code recovery routine
- **Overhead**
  - Regular output to voter chip interrupts functional processing
  - Check pointing is required more often
  - Performance loss of 50% or more is typical

**SEU / SET susceptibility**
- **Upset mechanisms**
  - Dynamic logic, found in all areas of commercial design
  - Storage nodes, RAMs and registers
  - Transient (SET) propagation through combinational logic to storage nodes
- **Flux rate**
  - SER at 90% W.C. GEO causes 1-2 upsets/hr
  - Proton projection at LEO causes 0.3-0.7 upsets/hr
  - Solar flares cause 0.1-20 upsets/sec
- **Recovery**
  - TMR recovery will typically require several minutes
  - Upsets may not be detected in

**Product cost**
- **Component costs**
  - Rad-hard voting chip has high recurring cost in addition to NRE
  - Commercial CPUs will have cost advantage
- **Software costs**
  - NRE for development of checking and recovery routines
- **Board costs**
  - More complex board design with lead time vs. a standard rad-hard product

Commercial processors, even with redundancy, have issues and exposures that far outweigh their benefits when compared to the RAD750 solution
Error detection and fault management features

Fault Tolerance Mechanisms:

- Embedded Micro Controller
  - Constant check on static configuration registers
  - On-chip parity check
  - Interface error check on Data and Address busses
  - Error logs
  - Critical registers are TRM in addition to SEL hardened
  - "1 Hot" state machines with checking
  - PCI Ready Parity

- PCI Data & Address parity
  - PCI protocol check
  - System watchdog time
  - Built In Self Test (BIST)
  - JTAG
    - Handshake error
    - Instruction parity
    - Access control
  - Error thresholding
    - Critical
    - Functional
  - Internal address checks

The RAD750 is supplemented by the Power PCI to comprehensively address system level fault management
"The work was performed for the Jet Propulsion Laboratory, California Institute of Technology, sponsored by the National Aeronautics and Space Administration.

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