X2000 Command and Data Handling System Development

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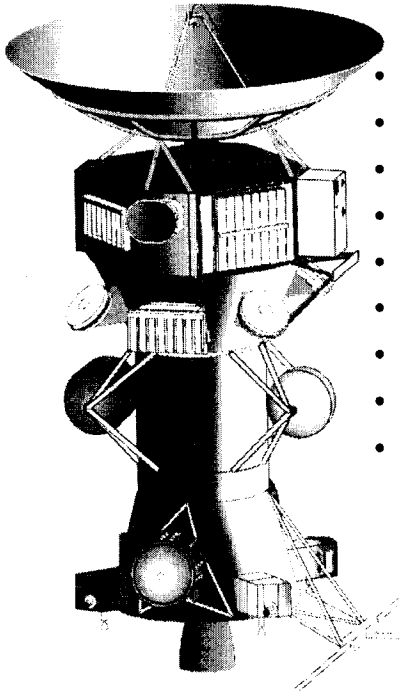
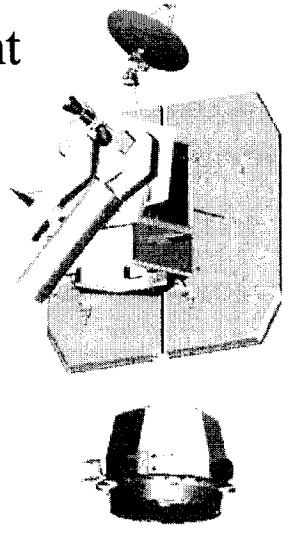
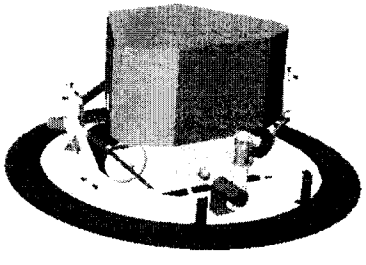
Agenda

Command and Data Handling System Development



- 10:00 C&DH Overview
- 10:01 System Flight Computer
- 10:03 System I/O Slice
- 10:13 Non-Volatile Memory Slice
- 10:23 System Interface Assembly
- 10:33 Temperature Remote I/O and Assembly
- 10:40 Advanced Packaging
- 10:50 Software
- 10:55 Integration & Test





X2000 Avionics Hardware Overview

PowerPC 750
- Radiation hardened version of commercial G3 processor
- IBM foundry

CPCI Bridge
- Interface between processor and CPCI bus
- BAE & IBM foundry

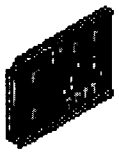
Digital I/O ASIC
- Bridge between 1394/I²C and CPCI bus
- 1394 link layer
- Foundry: Honeywell

Mixed Signal I/O ASIC
- Physical layer for 1394
- I²C driver circuits
- Foundry: Honeywell SSEC, Plymouth MI

Memory Control ASIC
- Interface memory and CPCI bus
- Includes error correction circuit
- Foundry: Honeywell SSEC, Plymouth MI

System Interface ASIC
- Interface between CPCI bus and high speed serial I/O for science and telecom
- Foundry: Honeywell SSEC, Plymouth MI

Temperature Remote I/O ASIC
- Includes 16 analog inputs for telemetry
- I²C interface
- Foundry: Honeywell SSEC, Plymouth MI



SFC - System Flight Computer
- PowerPC 750Compact PCI based
- 128 Mbytes DRAM; 256Kbytes EEPROM
- Baseline 240 MIPs; variable speed
- Contractor: BAE Systems, Manasas, Va.

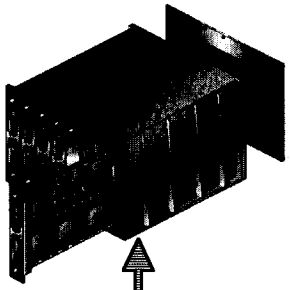
SIO - System Input/Output
- PCI/1394/I²C Bridge; 2 UARTs
- Includes node reset control; general fault protection logic; discretes
- Assembly developed at JPL

NVM - Non Volatile Memory
- 2 Gbit/slice Flash Memory
- Includes power management control and erase/write cycle tally
- Contractor: SEAKR Engineering, Littleton Co.

SIA - System Interface Assembly
- Includes 1553, SPI and high speed serial interfaces
- Assembly developed at JPL

TAS - TRIO Assembly Slice
- Temperature and analog collection
- 6 Temperature Remote I/O (TRIO) ASICs split between 2 I²C buses
- 96 telemetry channels; 10 bit A/D
- Contractor: Johns Hopkins University/Applied Physics Laboratory

compactPCI Chassis
- Commercial standard, first space application
- Developed at JPL



compactPCI Backplane
- Developed at JPL

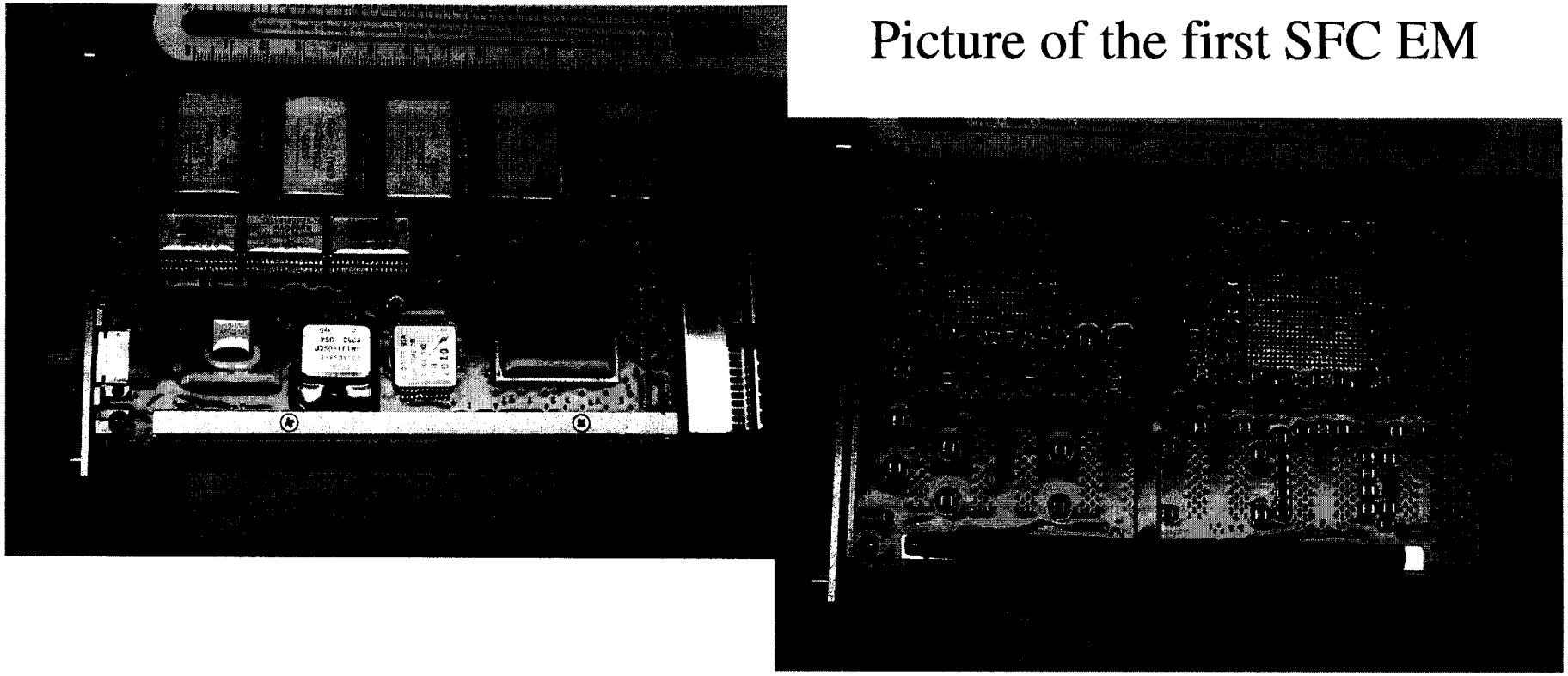
CDH ASIC Technology
- Radiation hardened, high density, digital and mixed signal ASICs
- ASICs complete FY 2002

Slice Technology
- 3U CPCI boards
- EM 's complete FY 2001, 2002
- FM's complete FY 2003

CPCI Chassis
- Complete Dual-String CDH in one 16 slot chassis
- One quarter mass and volume of Cassini CDS
- FM's complete FY 2004

System Flight Computer (SFC)

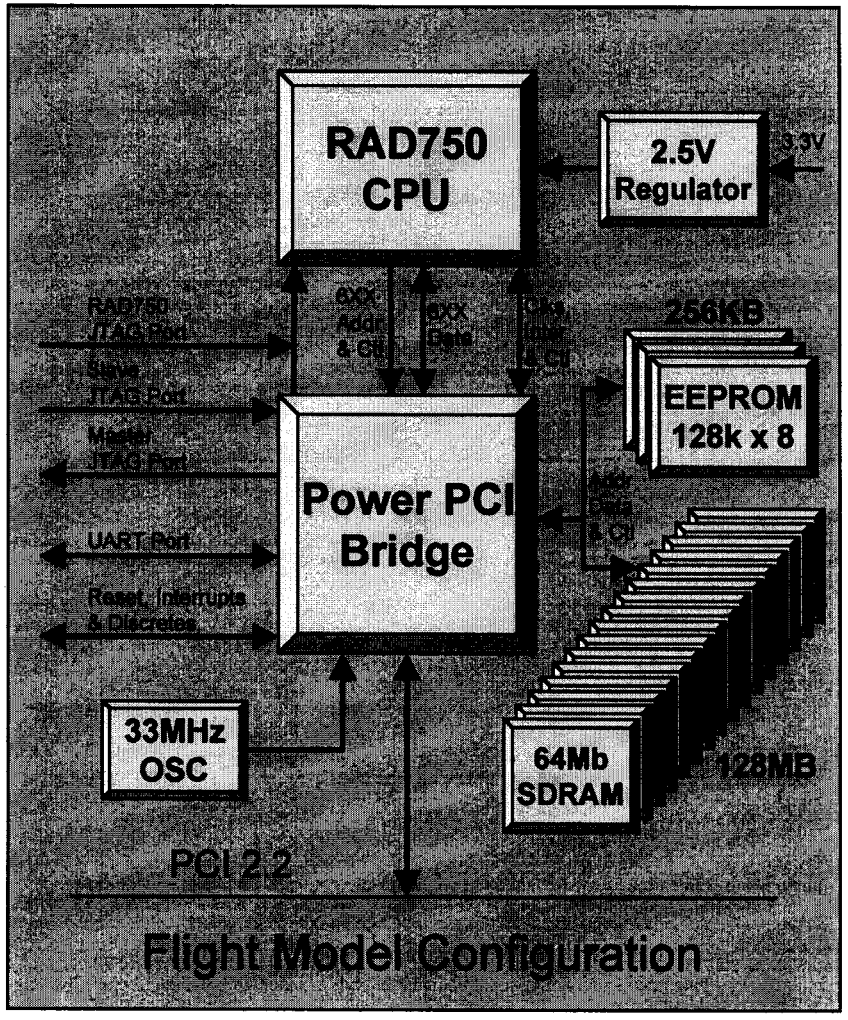
Picture of the first SFC EM

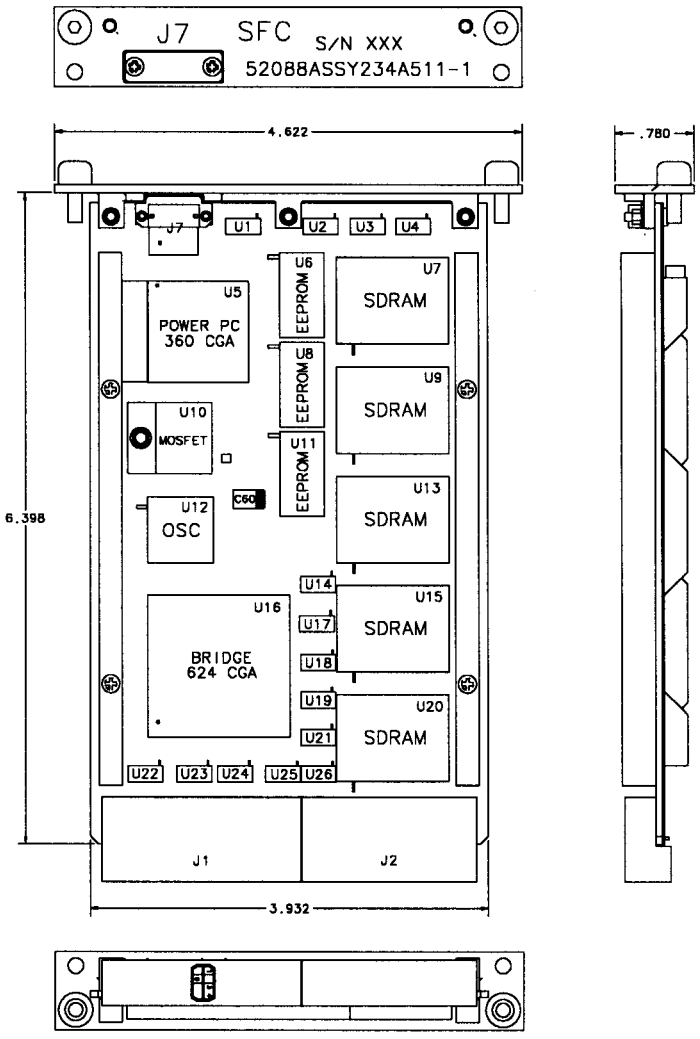


Following information provided by: Dwight Geer

Dwight.A.Geer@jpl.nasa.gov

System Flight Computer Block Diagram





Key Requirements: Baseline SFC

- SPEC95 performance benchmarks
  - 6.5 SPECint95, 3.9 SPECfp95 and 240 Dhrystone 2.1 MIPS
  - Performance degradation < 20% while PCI DMA activity is at 66 MB/s
- Power conservation modes controllable by software
- 32 bit 33 MHz CompactPCI Bus Specification
- 128 MBytes main memory
- 256 KBytes SUROM (Startup ROM)
- EDAC mechanism for all memory
- JTAG and built-in self-test (BIST) capability
- Double-Sided CompactPCI 3U Card
- Software includes:
  - Test routines to support BIST functions executed out of SUROM or RAM
  - BSP (Board Support Package) interface functions and SFC configurable hardware drivers
  - SUROM software to initialize the SFC to a known operational state

Key Requirements: Enhanced SFC

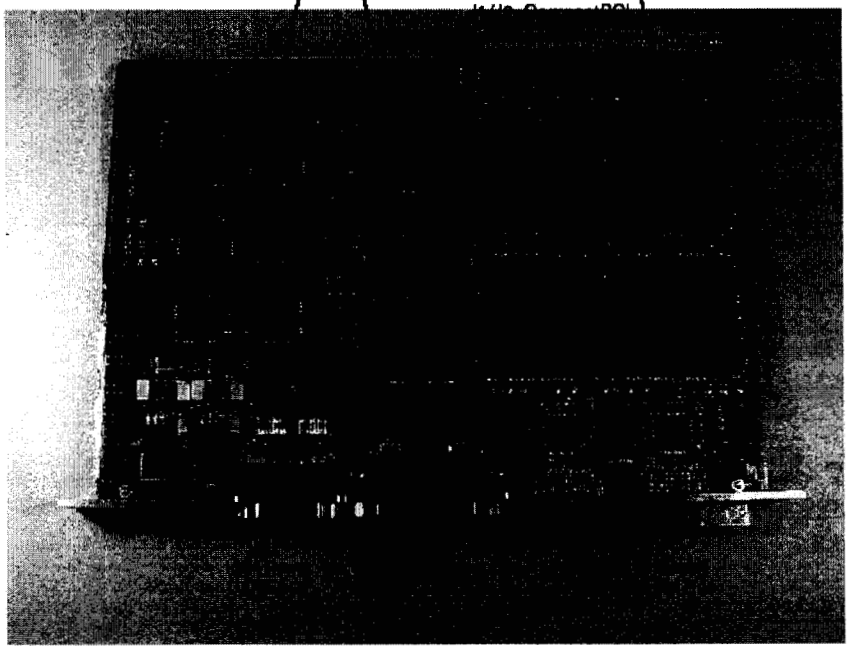
- Power PCI internal operation at 66 MHz (baseline is 33 MHz)
  - Reduces memory latency for cache miss
- DMA Controller with the following features:
  - Executes a linked list of DMA commands in RAM.
  - Performs transfers in all combinations of PCI and RAM access (RAM → PCI, PCI → RAM, PCI → PCI, RAM → RAM)
  - Generates CPU interrupts on the occurrence of certain events
    - Example: command completion, command list completion and error
    - Interrupts are maskable (defaults to masked)
- Increased size of Scratch Pad memory
  - Reduces CPU latency by prefetching PCI data into this RAM.
  - Reduce memory bus contention by allowing EMC code to be executed from this RAM

System I/O (SIO)

PROMs
- Contains DIO Hardware Design
- Loaded into FPGAs when Power is Applied
- Socketed to Allow Design Upgrades

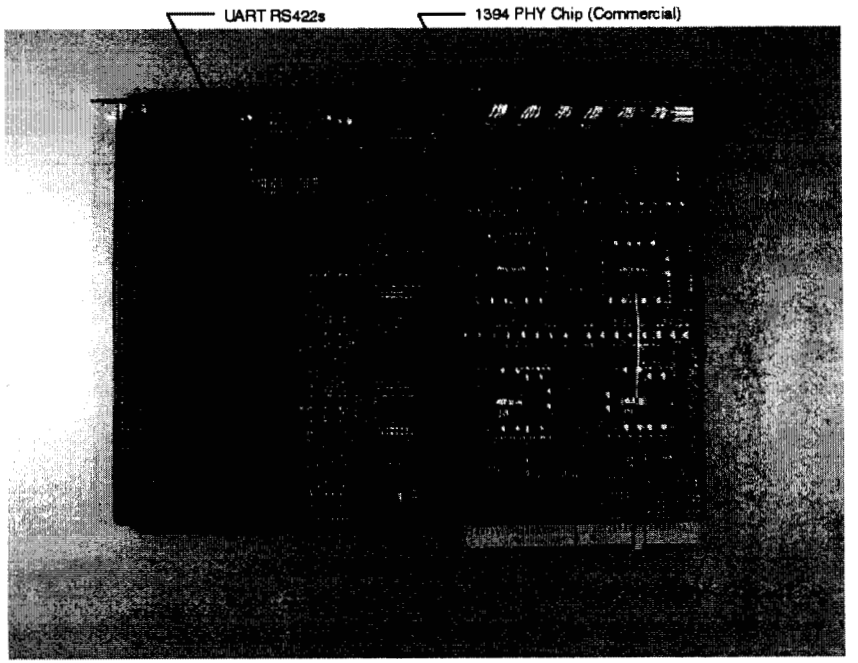
Dual Port Status RAM
- Part No. IDT 70V3579S
- 1394 FIFO

XILINX XCV800 FPGAs
- Two FPGAs Equivalent to a DIO ASIC
- Two DIO Equivalent ASICs on PT-SIO



Front

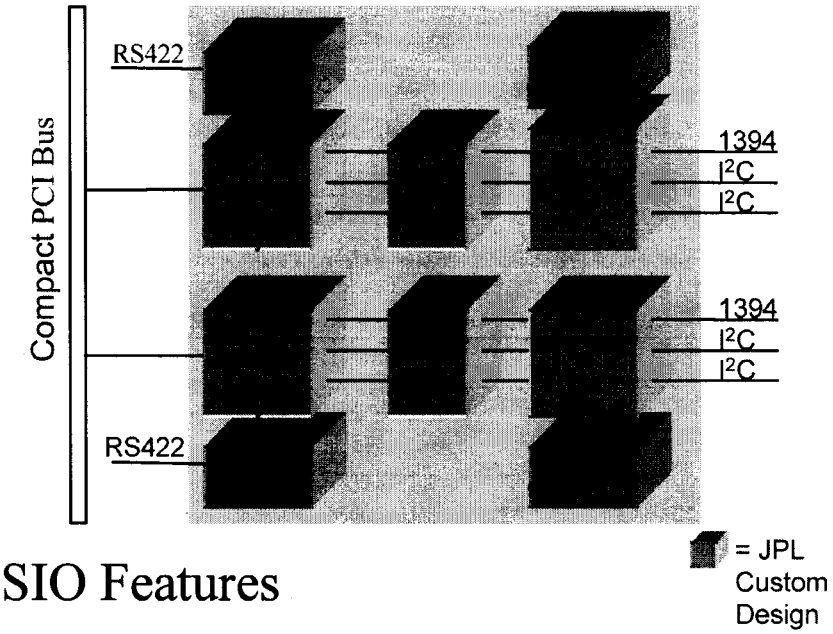
Back

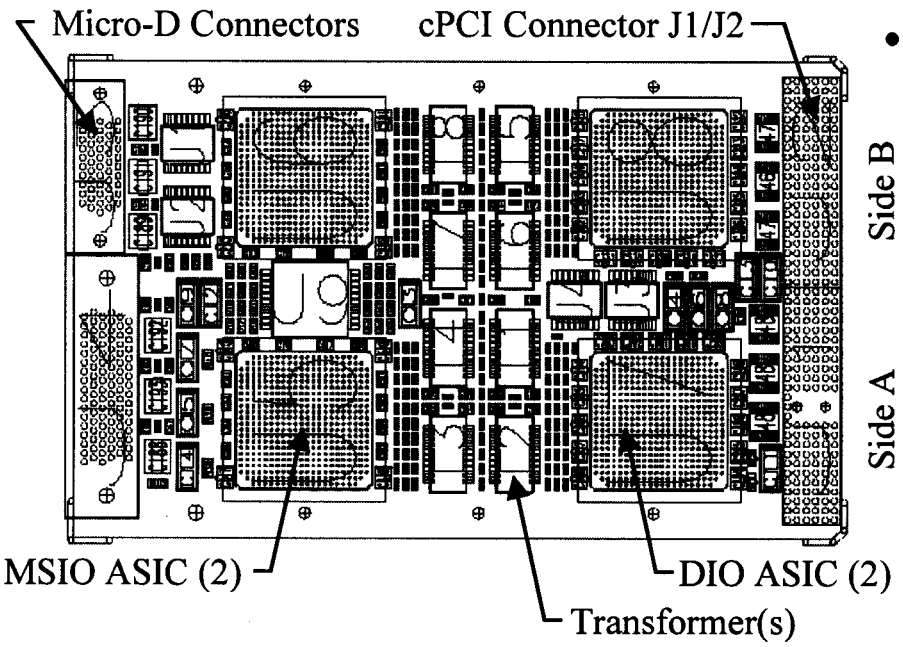


Following information provided by: Genji Arakaki
Genji.A.Arakaki@jpl.nasa.gov

SIO Description

- SIO Acts as the System Interface to Seven Separate X2000/EO Buses
  - Compact PCI bus (PICMG 2.0 R2.1)
  - IEEE 1394a Bus - 100 Mbps (2 per Slice)
  - I^2C Bus (4 per Slice)
  - Miscellaneous I/O
    - UART (4)
    - Discretes

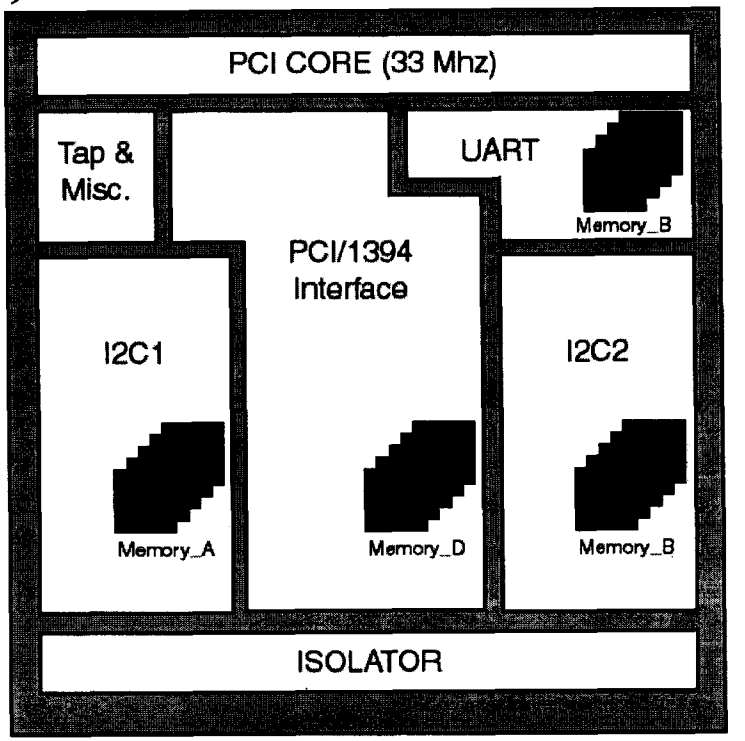




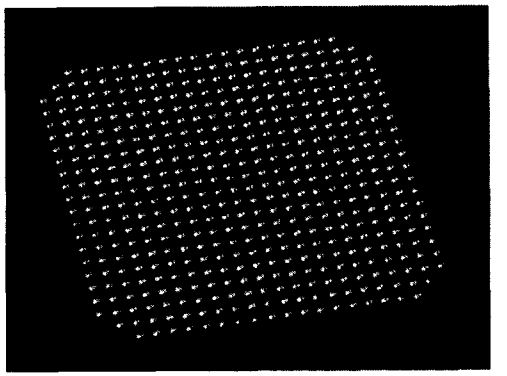
- SIO Features
  - Double-Sided 3U Compact PCI Card
  - 1 Mrad Radiation Hardened
  - Custom ASIC, Honeywell HX3000 for DIO
  - Custom Mixed Signal ASIC, Honeywell HX2000r for MSIO
  - Transformer Isolation between DIO and MSIO
  - Power: 11.3 Watts Est. Max.
  - Mass: .5 Kg Est.

Digital I/O (DIO) ASIC

- Functions
  - CompactPCI Interface (33 Mhz)
  - Link & Transaction Layer of 1394 (100 Mbps)
  - I^2C Bus Controller (Hi-Rel, Fault Tolerant)
  - 16550 UART
  - Custom Logic
  - Built-in Self Test
- Design
  - JPL (Specification, I^2C High-Rel Controller, Custom Logic, Integration, Simulation and Analysis
  - Innovative Semiconductor, Inc. Intellectual Property (1394 Link and Transaction)
  - Mentor Graphics (PCI, UART, I^2C IP)
- Honeywell HX3800 ASIC
  - .35 uM, SOI (Silicon-on-Insulator)
  - 1 MRad Hardened
  - Drop-in Memory
  - Est. 700 K Gates
  - Package: 472 Pin Dimpled BGA (Ceramic)



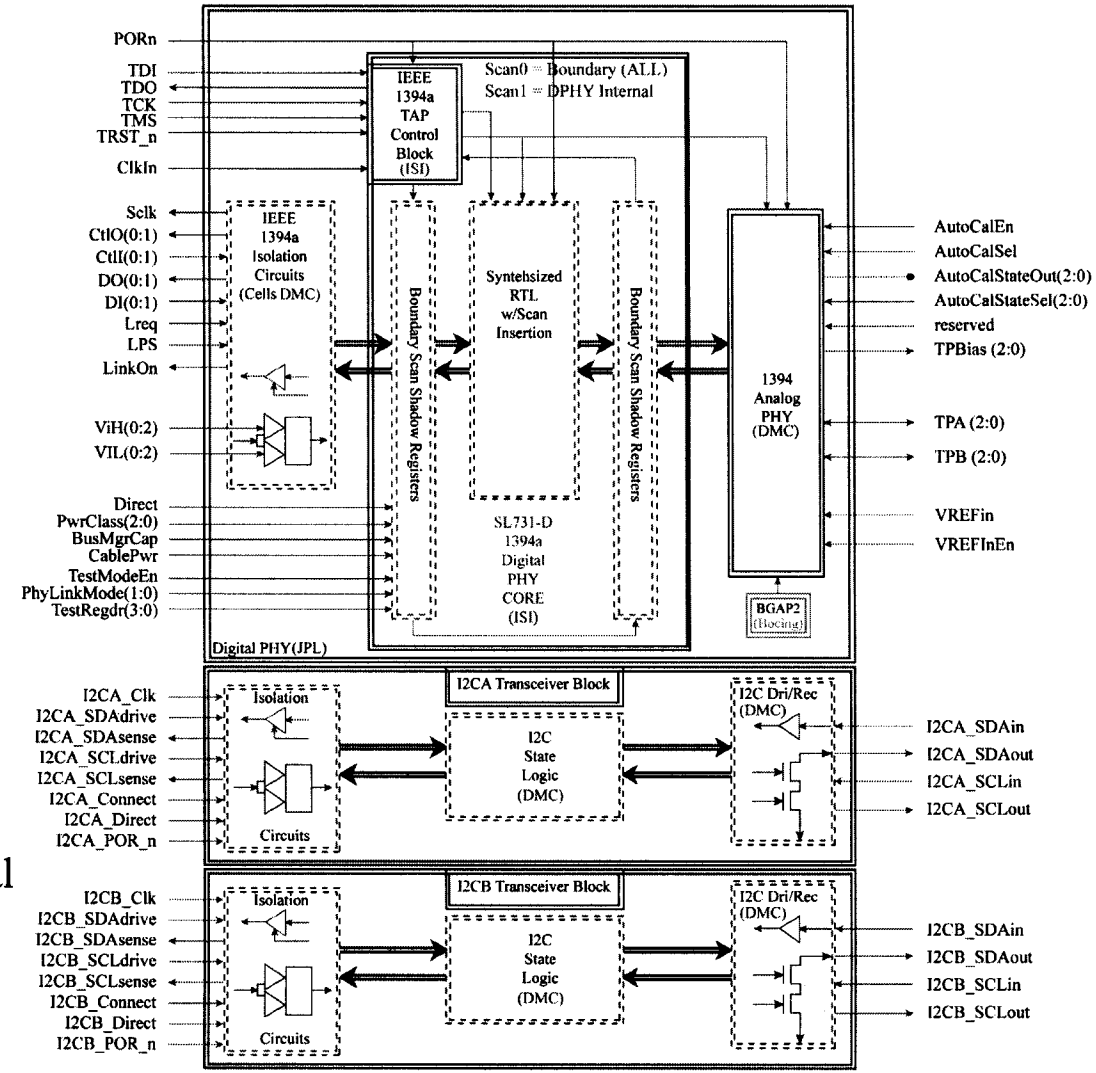
Floorplan: DIO



BGA Package
Size: 29 x 29 mm
(1.14 x 1.14 in)
472 Pins

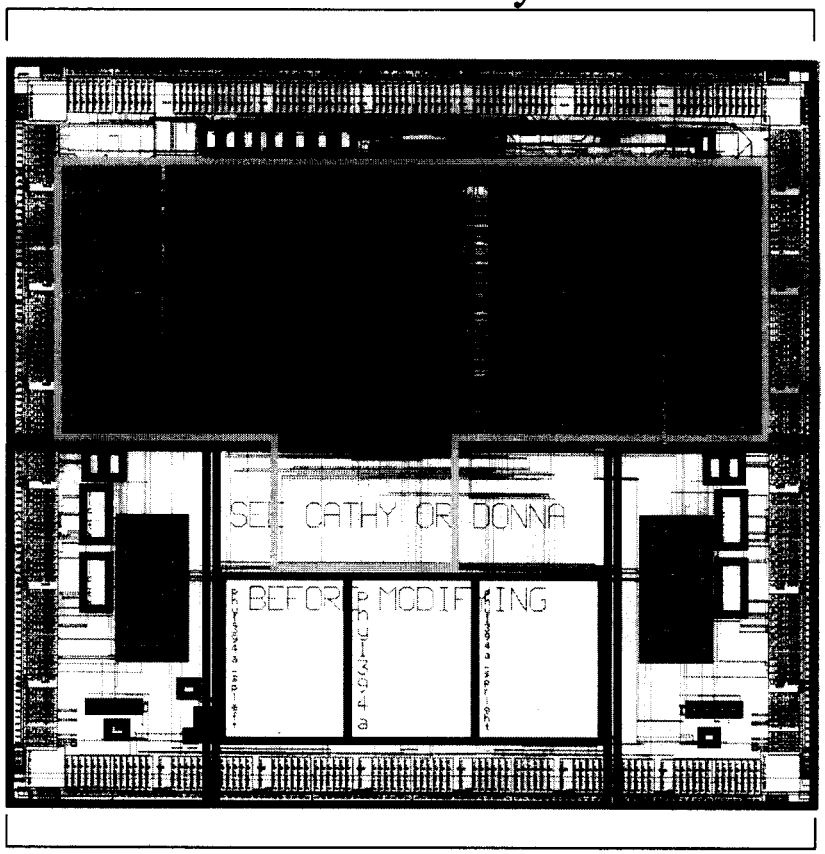
Mixed Signal I/O (MSIO) ASIC

- Functions
  - 1394 S100 Physical (PHY) Layer
    - Compliant to IEEE-1394a
  - Two (2) I^2C Physical Interfaces
    - Compliant with Philips Standard
    - Fault Protection features
- Highlights
  - Three Separate Power Domains (1394. I^2C (2))
  - I^2C Fail Silent
  - Slew Rate Limited I2C Drivers
  - High Current (30 mA) I2C Drivers
- Design
  - Innovative Semiconductor, Inc. IP (Digital 1394 Phy Block)
  - Boeing (Voltage Reference)
  - DigitalMediaCom (Analog Physical Layer, I^2C Blocks)
  - JPL In-house Specification, Integration, Simulation and Analysis



Mixed Signal I/O (MSIO) ASIC (con't)

To Isolated Link/Phy Interface



To 1394 Cable Termination

- I2C
- 1394
- Gate Array (Digital)
- Custom Analog Cells

- Fabrication
  - Honeywell HX2160r ASIC
    - .7 uM SOI CMOS
    - 1 MRad Hardened
    - 100 Mhz Rated (Maximum)
  - Package: 472 Pin Dimpled BGA (Ceramic)
- Characteristics
  - Power: .97 Watts Worst Case
  - 47K Internal Cell Site Count
  - 40% Placement Utilization

Actual Size
(12.15 x 13.55 mm)

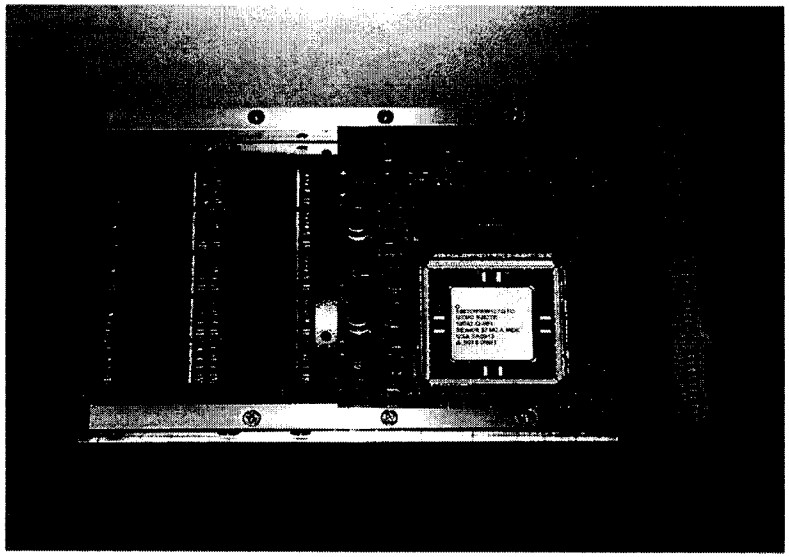
Differences between Prototype and Engineering Model

- Six Prototype-SIOs (FPGA based DIO) in Functional Testing and Integration
  - Key DIO Design Problems have been Resolved
- MSIO CDR Completed October, 2001
  - Chip Worst Case Analysis (WCA) Submitted and Reviewed
- MSIO Fabrication (Underlayers) Started in October, 2001
- Flight SIO Layout In-Process

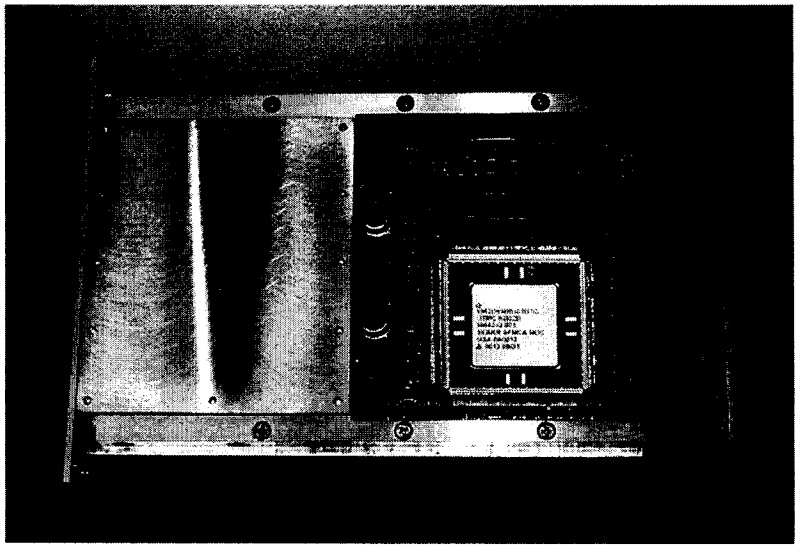
Remaining Milestones	Date
DIO PDR	2/15/02
DIO CDR	5/3/02
MSIO POD Delivery from Honeywell	7/29/02
DIO POD Delivery from Honeywell	10/7/02
SIO Slice CDR	7/26/02
SIO EM001 Delivery to Hardware Integration	10/28/02
SIO FM001 Delivery to Hardware Integration	9/26/03

Non-Volatile Memory (NVM)

NVM Engineering Model Board



without Clamshell



with Clamshell

Following information provided by: Karl Strauss

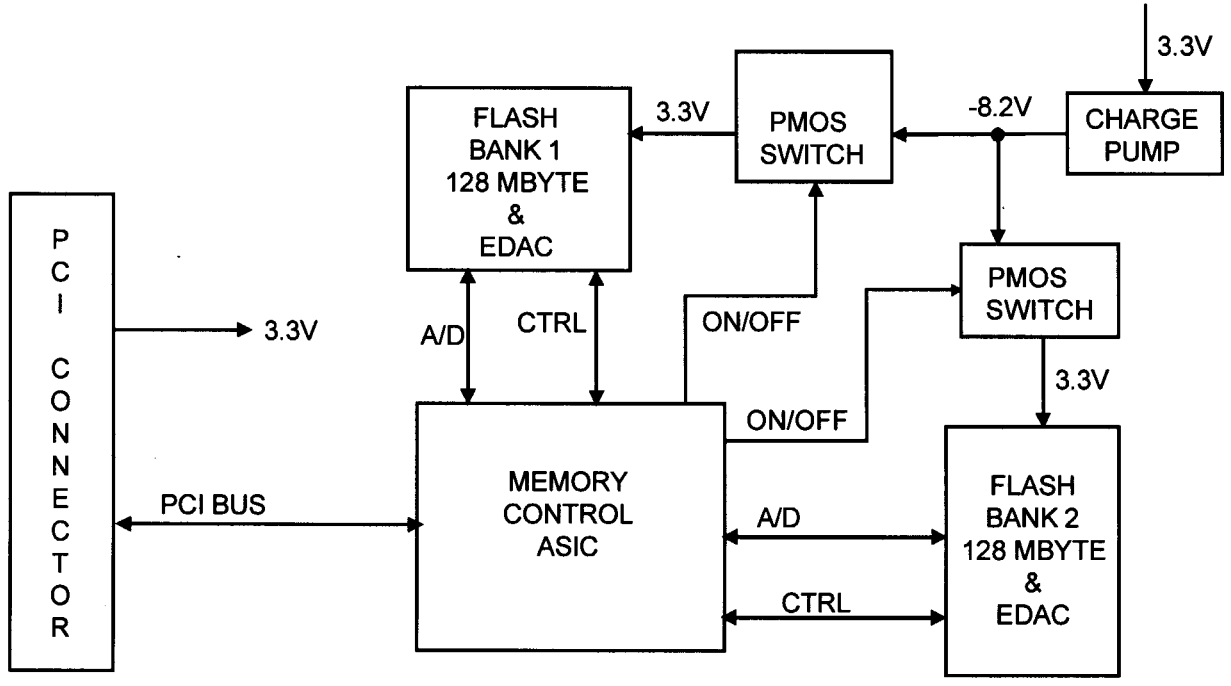
Karl.F.Strauss @jpl.nasa.gov

Description of the Nonvolatile Memory (NVM)

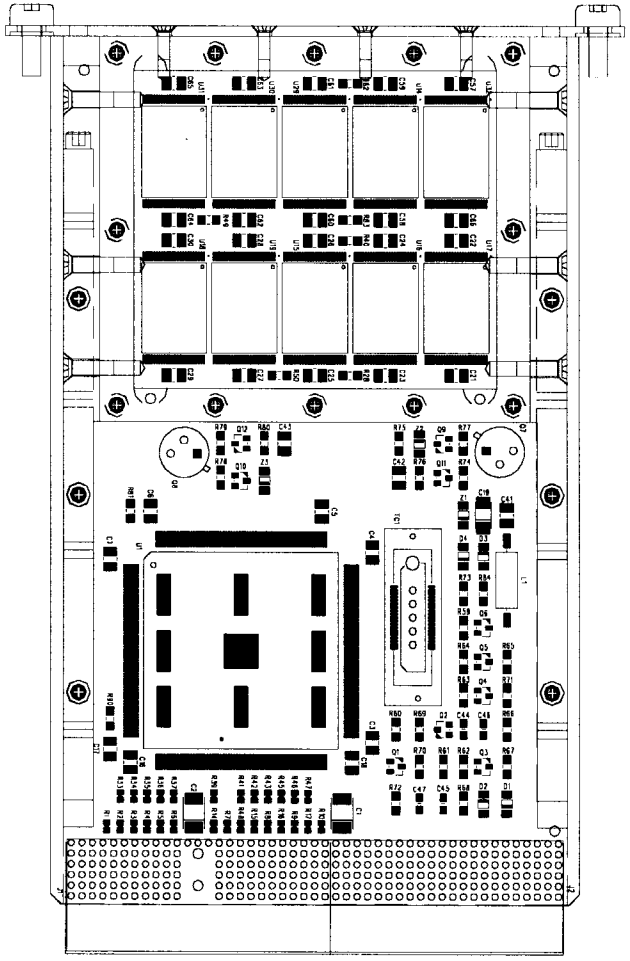
- Self-Contained 3U PCI format, Medium Capacity slice designed for Non-Volatile storage of Flight Software, Science Data, and State Machine information
- 2 Gb of Write Cycle Limited Non-Volatile Memory
  - Easily expandable to 8x capacity
  - Low Power: ~2W @ 3.3V
  - Mass: 1661 grams with Clamshell, 340 grams without
- Applicable to Many Diverse Applications
  - Designed to Operate in High Radiation Environment

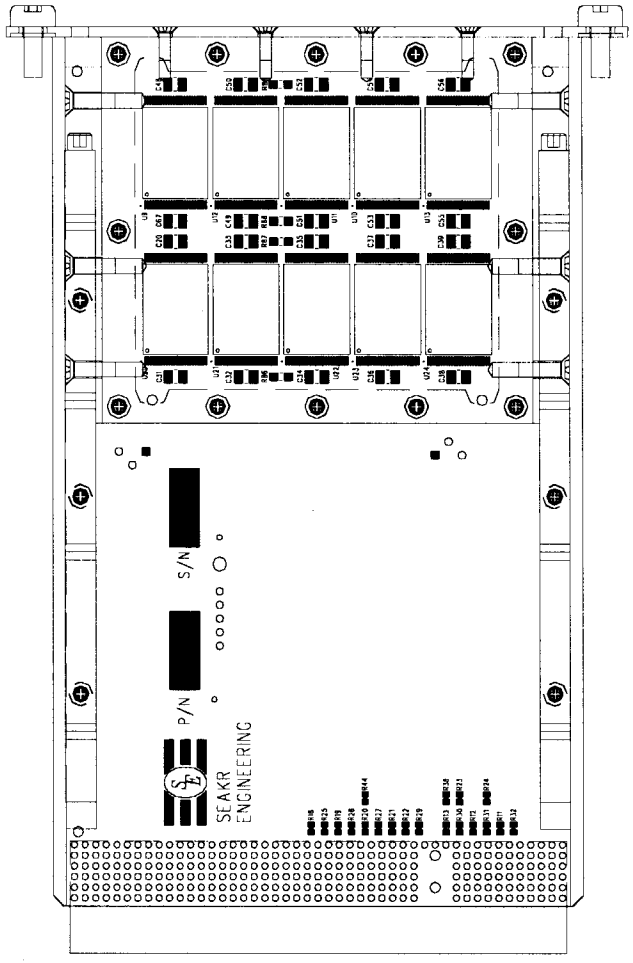
NVM – Block Diagram

- Memory Elements: 20 Samsung 128 Mb Flash
  - Organized into 2 Independent banks with Individual power control to each bank
    - Drop-in Substitution of higher density Flash parts permits immediate expansion to 4Gb. Card can go to 16Gb with stacked Flash devices
  - ASIC: Honeywell HX2160
    - Contains Reed-Solomon EDAC, allows loss of entire chip with no loss of data



NVM - Layout





Contract Information & Status

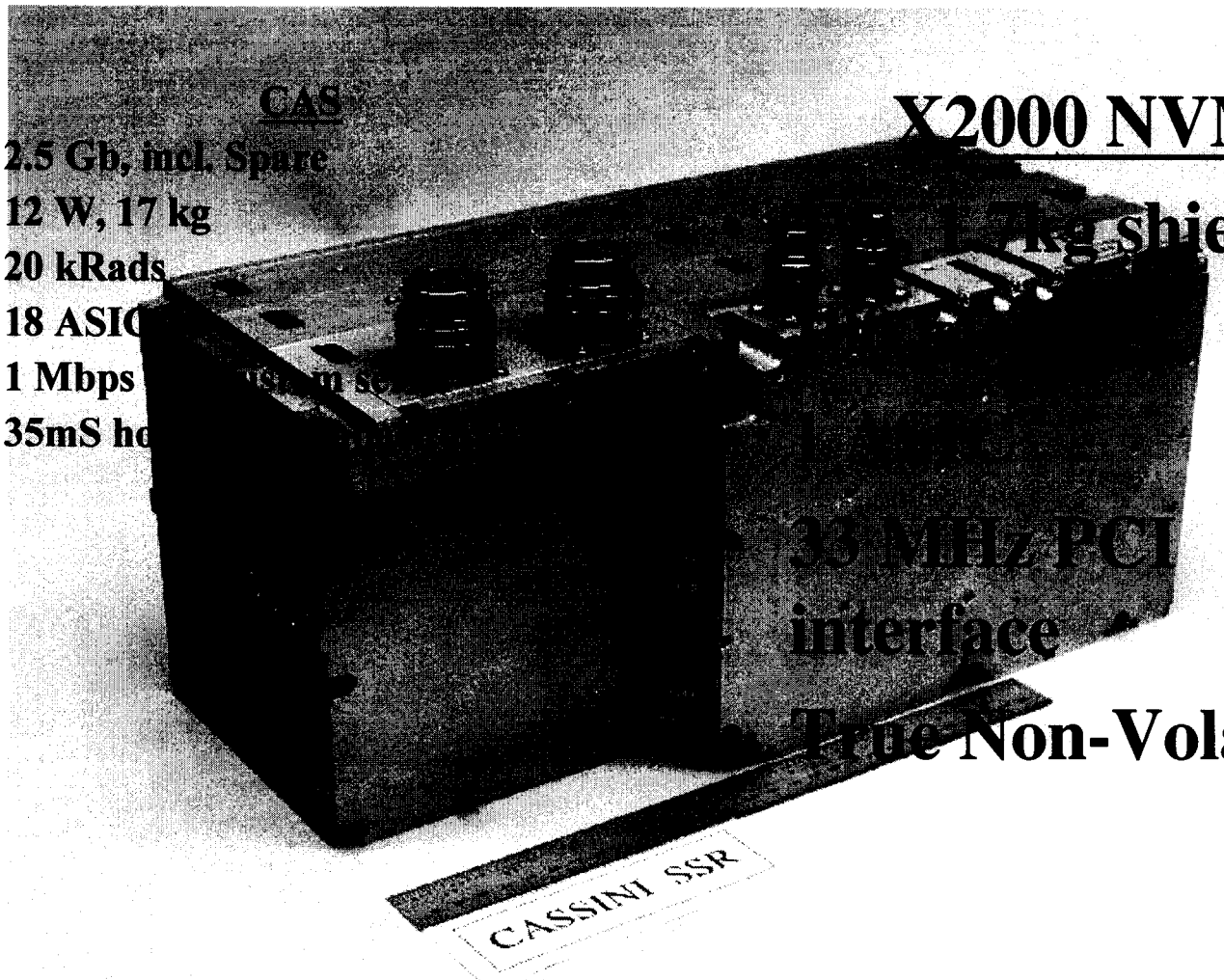
- Designed & Developed by SEAKR Engineering, Denver
- 10 Prototype units delivered to JPL
- 10 EM-grade units delivered to Deep Impact
- 14 FM-grade units on schedule for delivery next month
- Qual Test Complete
- Flight Units in post-manufacture test
  - First delivery in 3 weeks

Data Storage Technologies

A Small Historical Perspective

Item	MGN	CAS	MPF	X2000
Cap.	1.8Gb	2.5Gb	2Mb	2Gb
Media	Tape	DRAM	EPROM	Flash
Qty	1/3 Mile	640	80	20
Pwr	35W, 28V	12W, 28V	7W, 5,12V	3W, 3.3V
Mass	22kg	17kg	4kg	1.7kg
Size	16x12x8	16x8x7	6U VME (2 cards)	3U PCI
VOLATILE	N	Y	N	N

Data Storage Technologies



CAS

- 2.5 Gb, incl. Spare
- 12 W, 17 kg
- 20 kRads
- 18 ASIC
- 1 Mbps
- 35mS h

X2000 NVM

- 1.7kg shielded
- 33 MHz PCI interface
- True Non-Volatility

NVM Customers

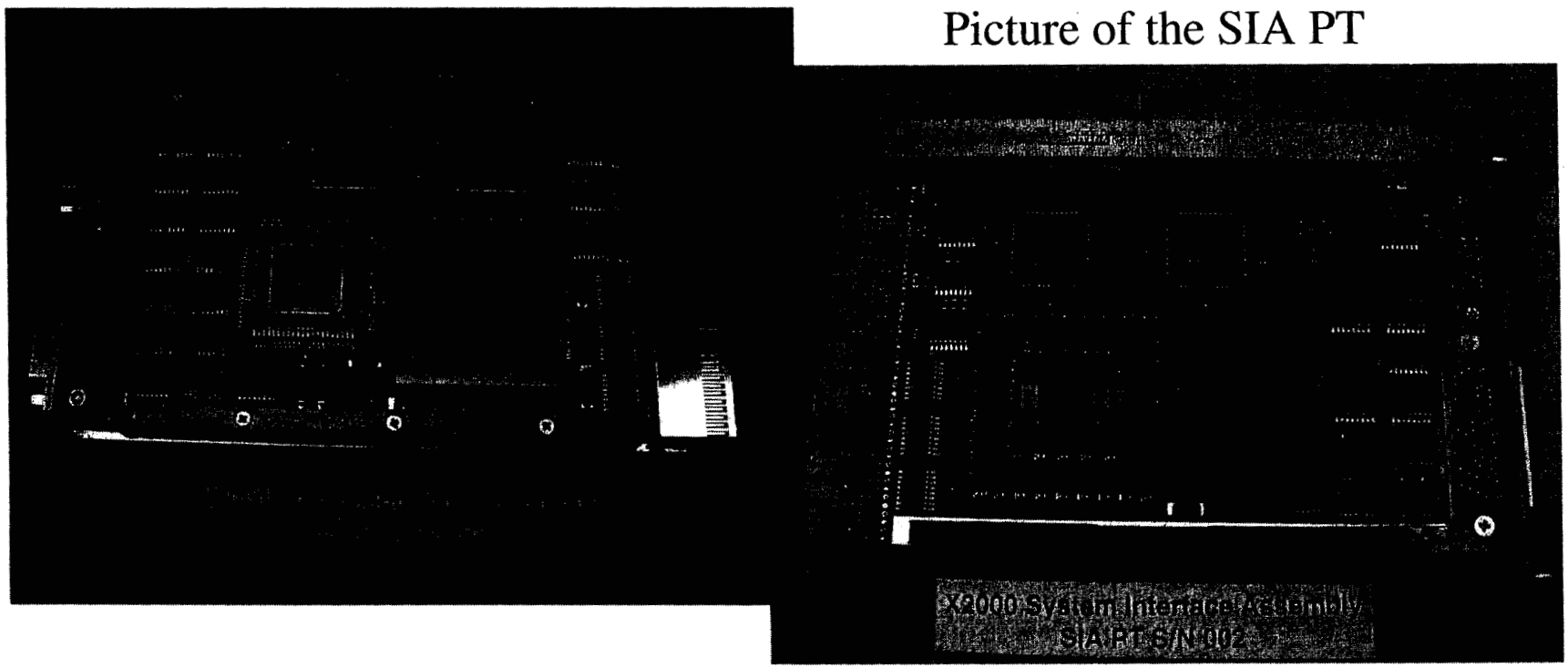
- Deep Impact: Using 5 slices per string
- Mars '05
- Other SEAKR customers

Adjunct Support

- JPL now sponsors the IEEE Non-Volatile Memory Technology Symposium
  - See http://nvm.jpl.nasa.gov

System Interface Assembly (SIA)

Picture of the SIA PT



Following information provided by: Dwight Geer

Dwight.A.Geer@jpl.nasa.gov

SIA Description

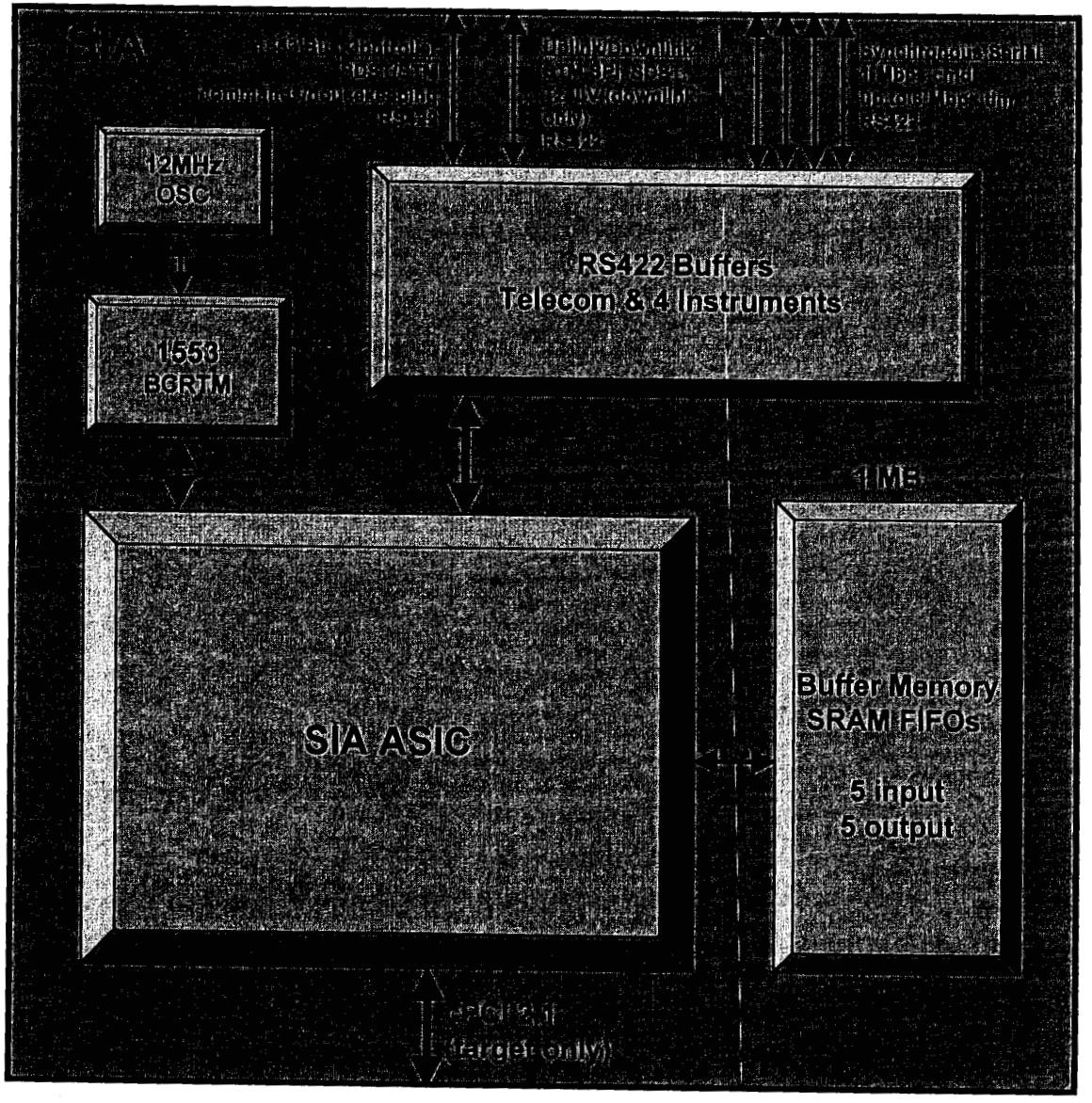
- The SIA provides the PCI bridge function to:
  - Four sensors
  - Two Telecommunication Subsystems
    - SDSTs (Small Deep Space Transponder) OR
    - STMs (Spacecraft Transponding Modem).
- PCI Target: 32 bit 33 MHz CompactPCI Bus Specification, PCIMG 2.0 R2.1
  - 1 PCI interrupt (INTA): all interrupts sources are maskable
- SIA clock: 32 bits and 1 μsec resolution (read/write)
- Buffer memory: 1 Mbyte
  - Configurable by software for each interface
    - Configurable Pointers: Top, Bottom, Watermark
    - Interrupts: Stale-Timer and "frame done"
  - Memory Arbiter – A Fair Round-Robin arbiter
- Double-Sided CompactPCI 3U card
  - Mass estimate: 0.5Kg
  - Power Estimate:

	Idle	Typ	Max	
• PT:		3.2W	6.5W	7.1W
• EM/FM:	3.5W	5.5W	6.2W	

SIA Description, cont

- Spacecraft Transponding Modem (STM) interface:
  - Redundant 1553 interface for engineering data, status and control
  - Redundant Serial Peripheral Interface (SPI)
    - Issues instantaneous serial telemetry output data rate of 4.1 Mbps to the STM
    - Uplink rate on SPI command interface is 2.0 Mbps
- Small Deep Space Transponder (SDST) interface:
  - Redundant 1553 interfaces for engineering and status and data
  - Redundant serial interfaces (one each for command and telemetry) to each transponder
    - Downlink encoding: no encoding, the Reed Solomon Encoder or the Turbo Encoder
    - Downlink telemetry rates: 5 bps and 250 kbps
      (actual maximum rate could be higher to support test activity)
    - Uplink Hardware Commands: 8 discrete outputs settable
      (One output is an active low pulsed signal used as a hardware decoded reset)
    - Direct Access port: supports command data rate up to 250 kbps
- High speed synchronous serial interfaces (4 input and 4 output)
  - Command interface: 1 Mbps instantaneous serial link data transfers per channel
  - Telemetry interface: up to 6Mbps instantaneous serial link data transfers per channel
  - Instrument interfaces can be reset independently of all other interfaces
- Tz (Time Zero) Umbilical Support Interface

SIA Block Diagram



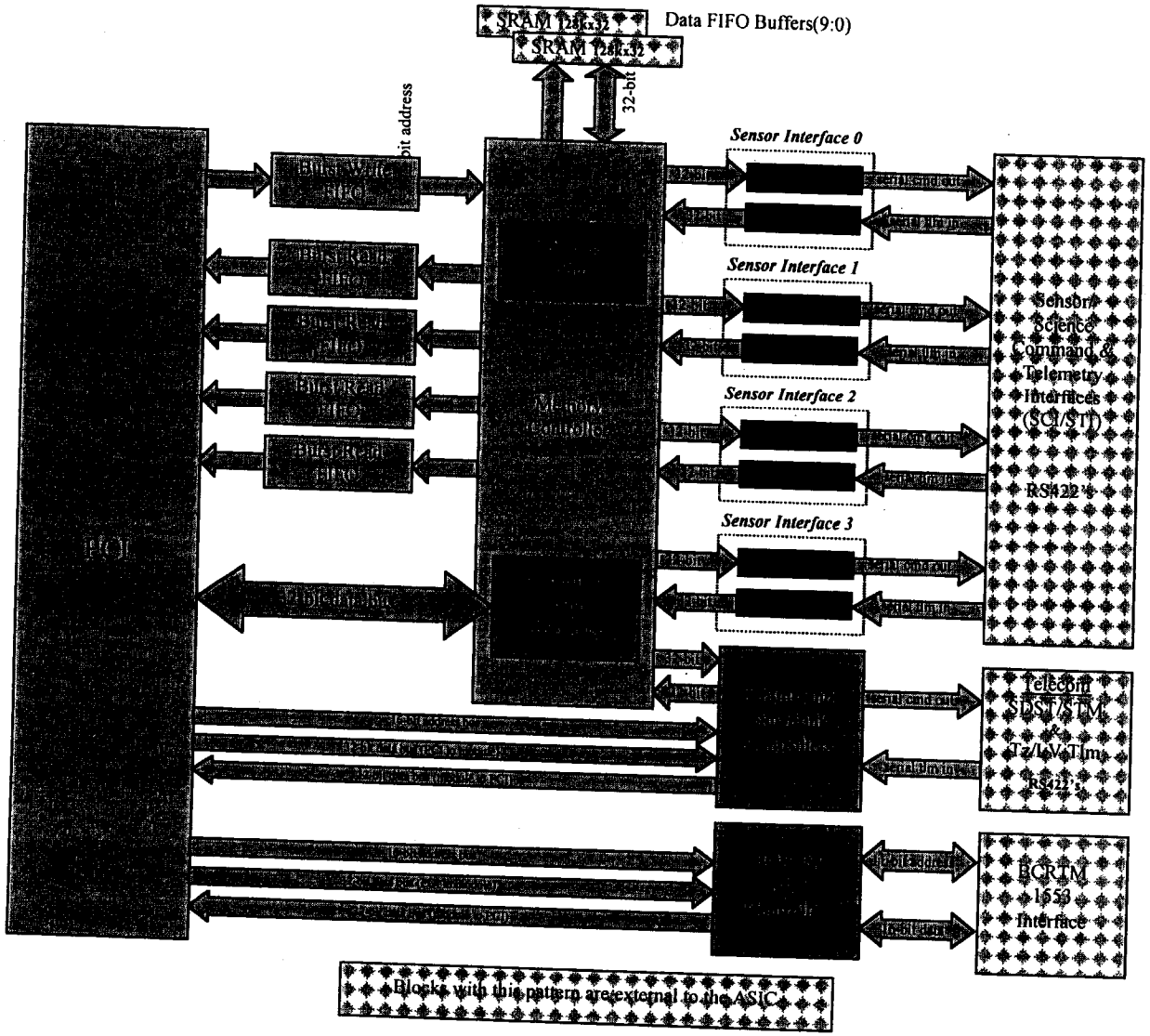
The System Interface Assembly development is in-house (JPL)

- Prototype SIA (PT) – based on Xilinx Virtex 1000e 560 pin Ball Grid Array FPGA
- Engineering Model (EM) – baseline replaces FPGA with Honeywell HX3800 ASIC
- Flight Model (FM)

System Interface Assembly components

- Double-sided Compact PCI card
- Radhard SIA ASIC
- Radhard UTMC BCRTM ASIC
- Radhard BAE SYSTEMS 128Kx32 SRAM Modules
- Radhard Intersil RS422 Driver/Receivers
- Radhard QTECH 12MHz Oscillator

SIA ASIC Description



SIA ASIC Description - Backup

- The SIA ASIC provides most of the functionality of the SIA card.
  - The EM/FM SIA ASIC operates on 3.3 volts

<u>The ASIC major blocks</u>

- PCI Target Core
  - 33 MHz, 32-bit operations
  - 1 PCI Interrupt
- PCI Rate Buffer Core
  - 1 write (35 x 8 words) and 4 read (32 x 8 words) FIFOs
- Memory FIFO Control Core
  - Configures 1 Mbyte SRAM partitioned into 10 buffers
    - This memory is used as buffer memory between PCI system card and serial interface peripherals. It can be partitioned up to 10 individual buffers, i.e. configurable to optimize a target system whether it uses 1 or all 10 of the buffers.
  - Watermarks, Stale-Timer and "frame done" interrupts provide software flexibility
  - Memory Arbiter – A Fair Round-Robin arbiter

SIA ASIC Description – Backup, cont

- Uplink Core
  - Configurable to support SDST or STM redundant Uplink Command bit serial interfaces
  - SDST Mode:
    - Hardware Command Decoder
    - Provides pulsed decode capability to enable spacecraft reset independent of software
    - 7 level discrete general-purpose hardware decoded commands
    - Performs error checking and bit stream polarity resolution
  - STM Mode:
    - Uplink Command Serial Peripheral Interface (SPI)
- Downlink Core
  - Configurable to support SDST or STM redundant Downlink Telemetry bit serial interfaces
  - SDST Mode:
    - Configurable to support 3 encoding modes: Reed-Solomon, Turbo or no encoding
    - Configurable to provide Pseudo-Randomization of the data
  - STM Mode:
    - Downlink Telemetry Serial Peripheral Interface (SPI)

Note: Either STM or SDST style interfaces may be selected by software (triplicate voted in hardware)

SIA ASIC Description – Backup, cont

- UTMC BCRTM 1553 ASIC Controller Core
  - Typically used as Bus controller to command and retrieve housekeeping data to/from SDST/STM
  - The BCRTM Controller Core, controlling the UTMC ASIC, can be used as a general purpose Bus Controller or Remote Terminal for many other applications
  - Timed command capability allowing 1 μs resolution command issuance
  - Direct Access tap (intended for RS422 buffers) provides for the 1553 users to monitor 1553 traffic during integration and for closed loop testing support
- Four high-speed synchronous serial command interface Cores
  - SIA → sensor/instrument interfaces typically used to command a sensor or instrument
  - 1 Mbps serial interface
  - Timed command capability allowing 1 μs resolution command issuance
  - Three wire hardware interface (clock, data, frame)
- Four high speed synchronous serial telemetry interface Cores
  - Sensor/instrument → SIA interfaces typically used to collect sensor or science data
  - SIA supports interface rates to 6 Mbps
  - Three wire hardware interface (clock, data, frame)

SIA ASIC Description – Backup, cont

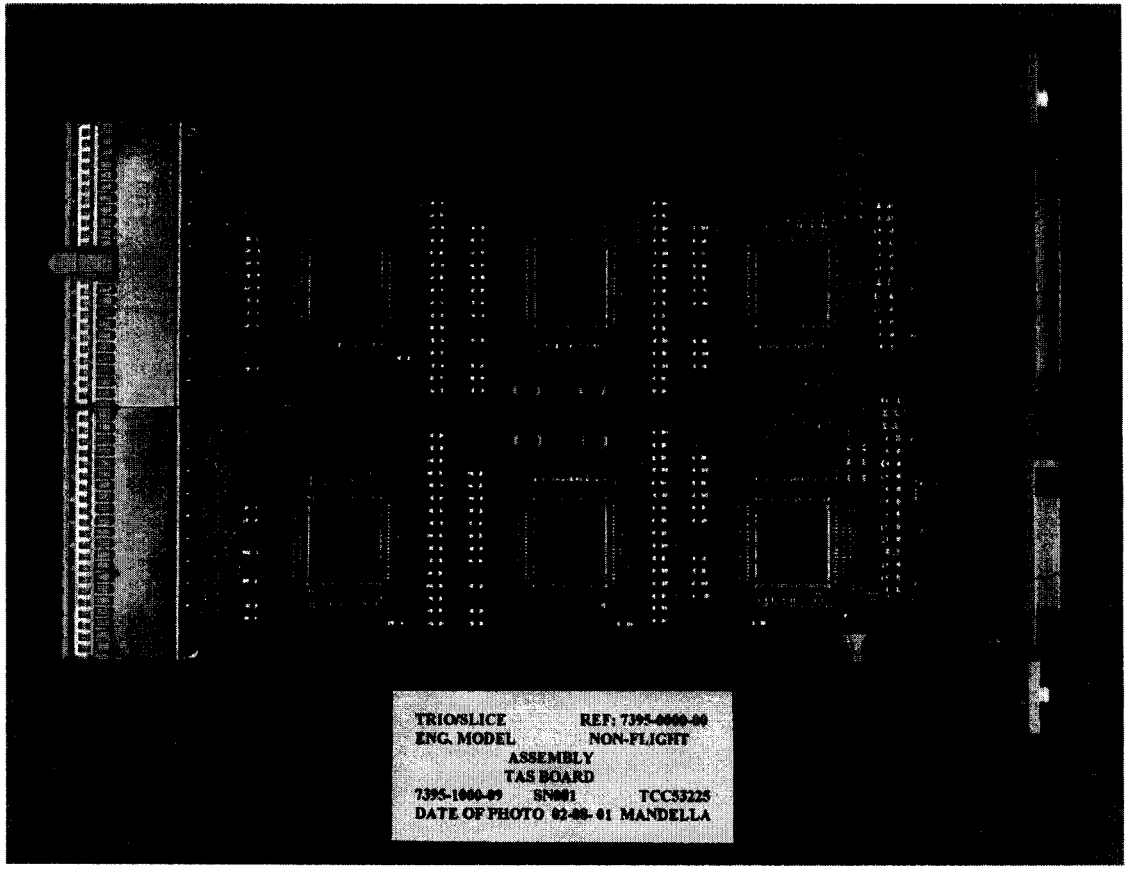
- Time Zero (Tz) Umbilical Support Functions
  - Tz Uplink
    - Uplink commands may be directed toward SIA HCD or may be rerouted to STM
  - Tz Echo Command Monitor
    - Provides method to monitor the spacecraft command source whether it is Tz, SDST or STM
  - Tz Downlink
    - Serial data and clock interface which forwards STM produced telemetry data (if STM mode selected) or SIA encoded telemetry (if SDST mode selected)
- Targeted to a radiation hardened ASIC Foundry.

SIA Current Status

All 6 Prototypes are in the lab

- SIA ASIC PDR – August 2002
- SIA ASIC CDR – November 2002
- SIA ASIC Tape Out – December 2002
- Board CDR – February 2003
- First SIA EM (POD ASIC) – August 2003
- First SIA EM (EM ASIC) – October 2003
- EM QUAL Complete – December 2003
- First SIA FM – December 2003

Temperature Remote Input Output (TRIO)



Following information provided by: Karl Strauss

Karl.F.Strauss @jpl.nasa.gov

TRIO Chip & TRIO Assembly Slice (TAS)

- TRIO (Temperature Remote Input Output)
  - A Very Low Power Multi-input Rad Hard A-D
- TAS (TRIO Assembly Slice)
  - Contains 6 TRIO chips + Rad Hard Voltage References
    - 2 sets of 3 units on separate power & ground planes
    - Design robust to 1 MRad

Contract Implementation

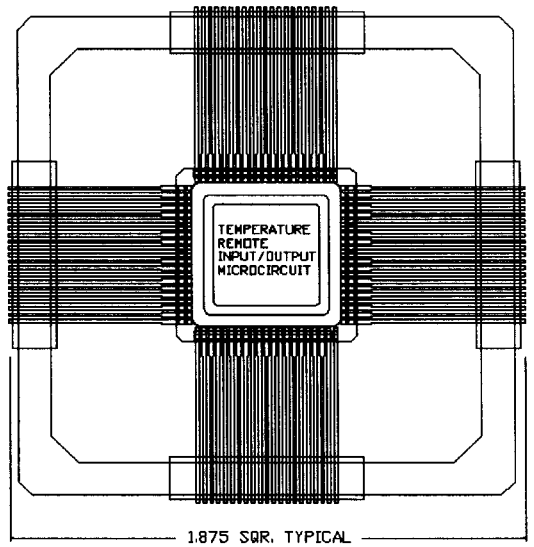
- TRIO developed & acquired under contract from Applied Physics Laboratory Johns Hopkins University, Laurel, Maryland

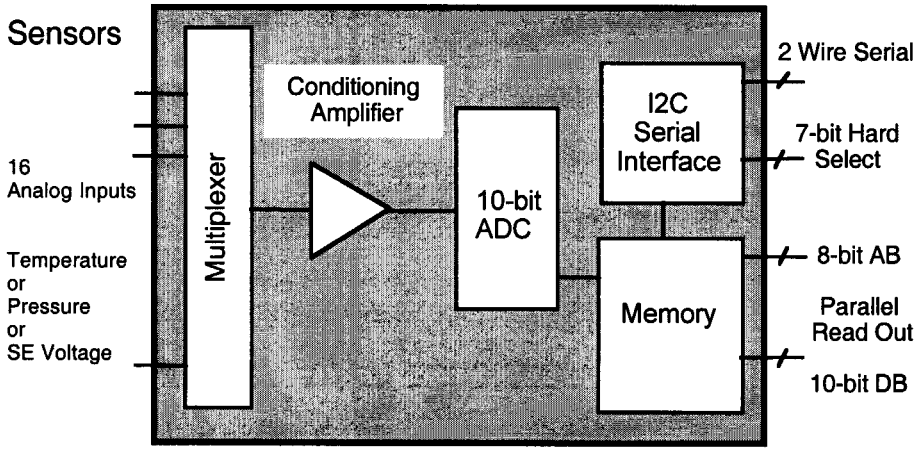
- The TRIO chip is an upgrade to the "TRIO-A" chip designed by APL and being used in several APL-run Space Missions

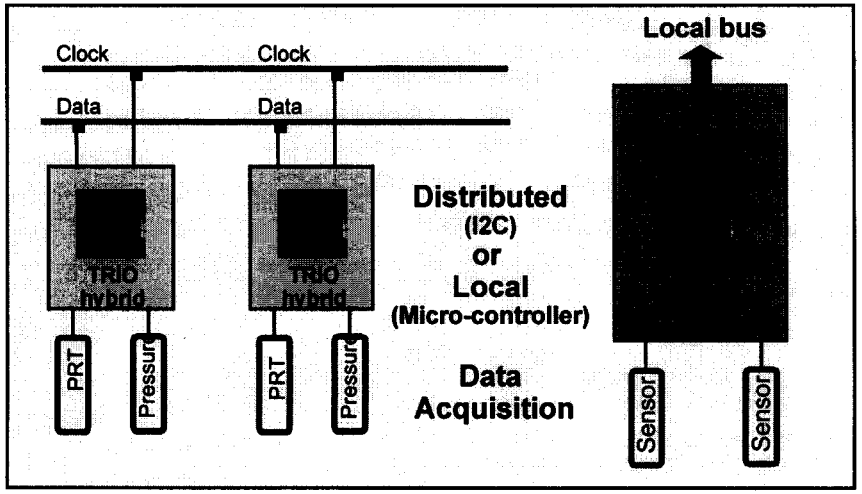
TRIO Chip Summary

Specifications:

- •16 analog inputs extendable to 32 with external MUX
- •Temperature mode with platinum resistance thermometers
- •Voltage mode with single ended voltage transducers
- •Programmable front-end delay up to 5msecs
- •10-bit successive approx. ADC settable up to 20KSamples/sec
- •Built-in voltage reference
- •32 10-bit memory locations
- •Standard parallel interface with 10-bit DB and 8-bit AB
- •Standard I2C serial interface with 7-bit hard address select
- •Built-in protection circuit in the serial interface
- •Fixed mode and scanning mode of operation
- •Configuration for 10-bit DAC
- •3-6V PS operation; power dissipation < 10mW @3.3V
- •Technology: Bulk CMOS 0.8u, Class S 4 Meg Rad

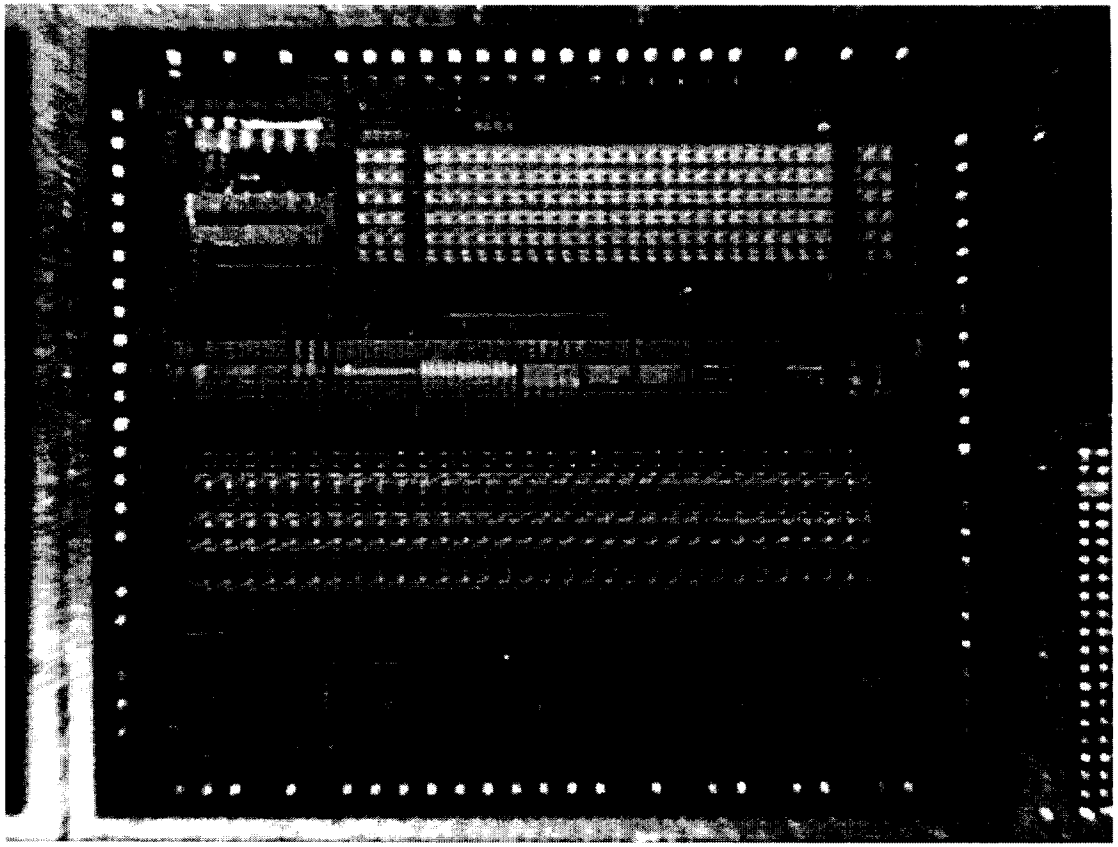






TRIO Status

TRIO die microphotograph



Status

TRIO fabrication complete

- Honeywell RICMOS IV
- Honeywell has closed production of RICMOS IV line
  - TRIO design rules compatible with Sandia fab

EM units on schedule, deliver 7/15

FM units on schedule, deliver 8/7

Mechanical Design and Development

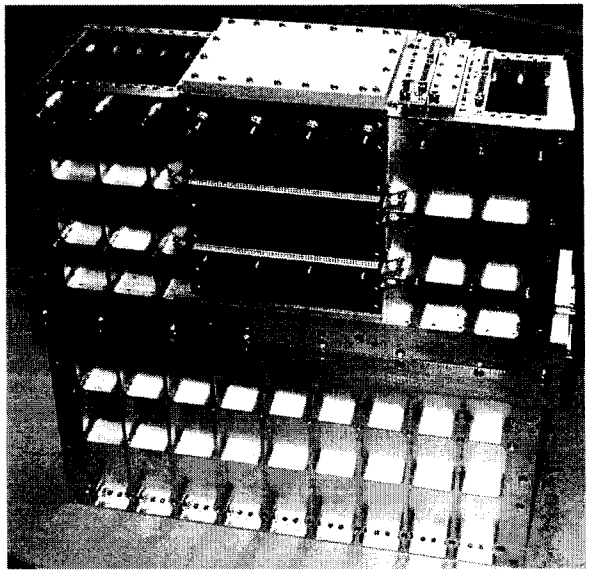
Following information provided by: Charlie Kaczinski
Charles.J.Kaczinski@jpl.nasa.gov

Requirements/Goals

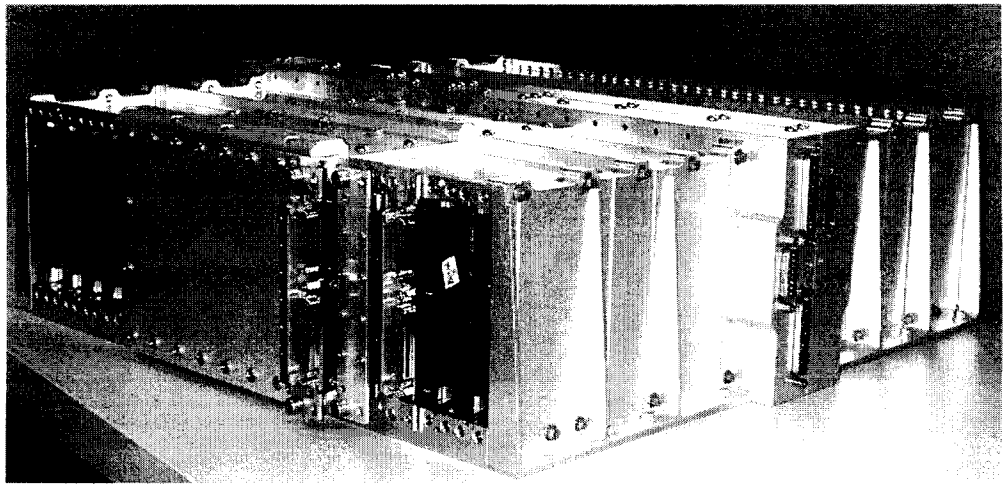
- Major Requirements
  - Mass - Targeting 100 Kg for Avionics system with radiation shielding
  - 10 Mrad behind 1mm [40 mil] spacecraft structure with 1.5 RDM radiation shielding.
  - 0.2 g^2/Hz vibration at slice and at the interface of the panel and chassis.
  - 2000g Pyro shock at the interface of the panel and chassis.
  - -55°C to +70°C operation at slice interface.
  - Any X2000 slice must be able to insert into a standard compact PCI chassis.
  - Must be able to remove any slice without affecting other slices.
  - Must handle up to 12 Watts heat dissipation on any given Slice.
- Goals have been established such as:
  - Industry available connectors, cables and breakout boxes.
  - Standard mounting hardware.
  - Power dissipation handling capability independent of card position in chassis.
  - Backplane removal without affecting other cards or backplanes.
  - Fit 16 Power Switches on a Slice.
  - Slice to Slice interconnect through backplanes.
  - Key Slice by Slice Type.

Current Europa Baseline Chassis

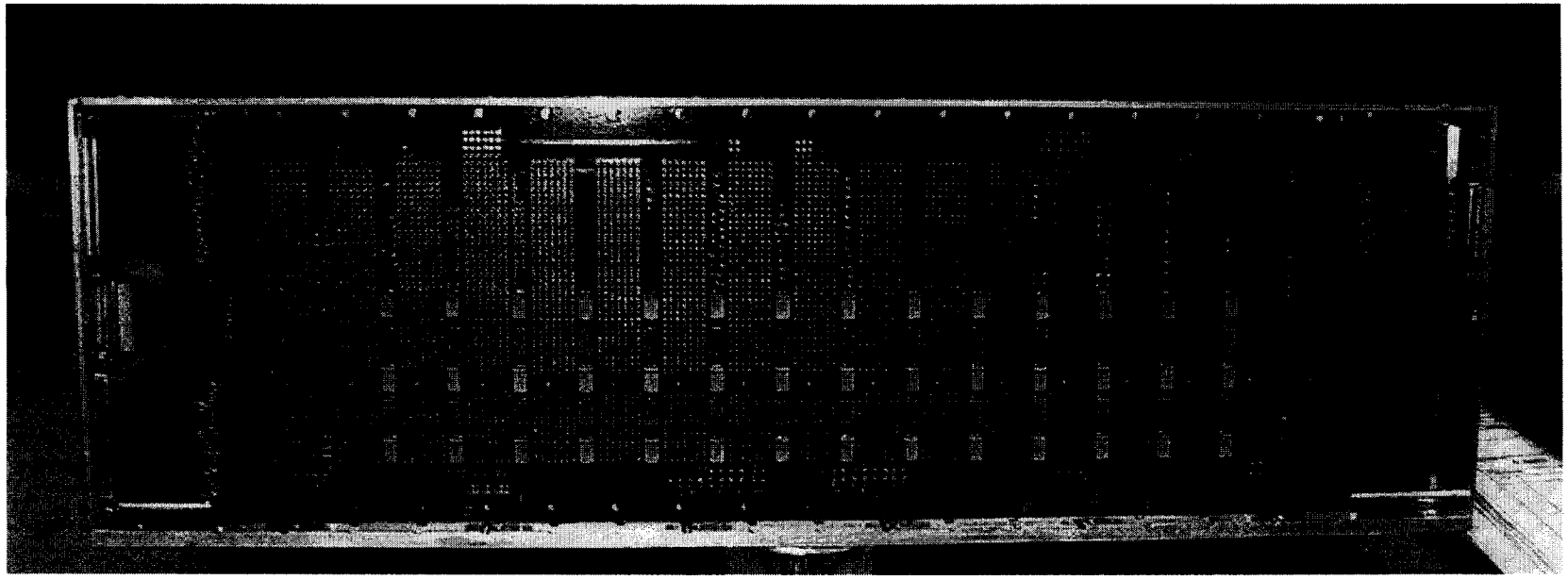
- Each Chassis mounted on separate spacecraft panel.
- Size Constraint, including cables:
  - 575mm [22.64"] to 620mm[24.41"] wide
  - 600 mm [23.62"]high
  - 152 mm [5.98"] deep.
- Chassis
  - Two rows of cards
  - Multiple Backplanes
    - Connected using Flex Cable(s)
- Internal Access Cabling
  - Backplanes
  - Multiple Front Panel Connectors.
- External Access Cabling
  - Multiple Side Panel Connectors.



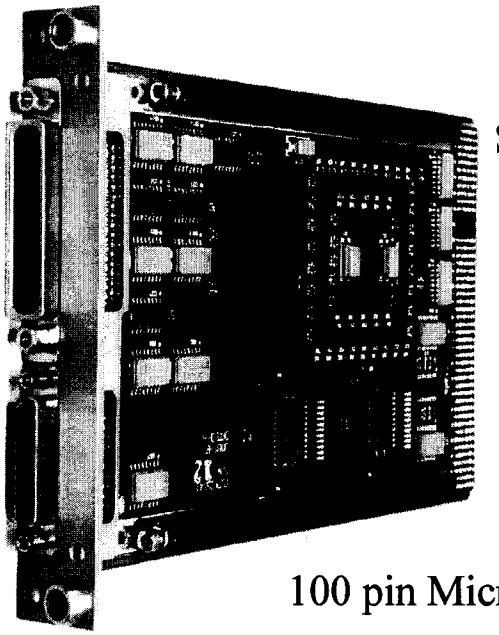
C&DH Chassis

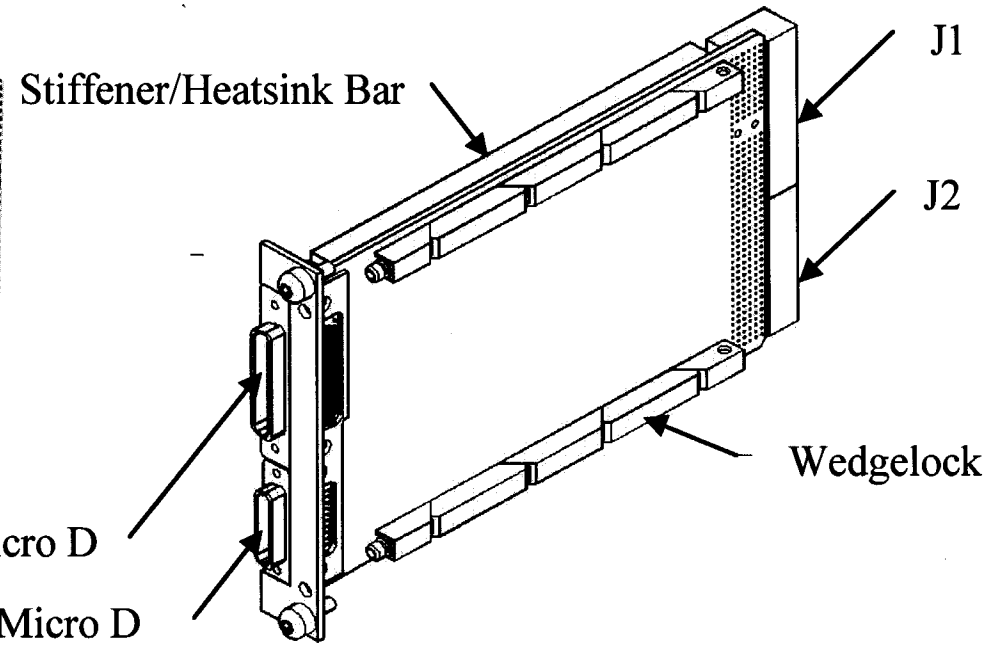


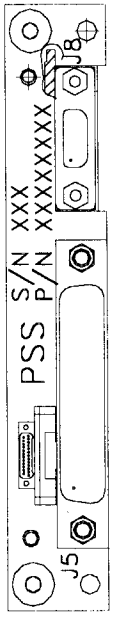
CDH BackPlane in EM Chassis



X-2000 CPCI Slice Configuration



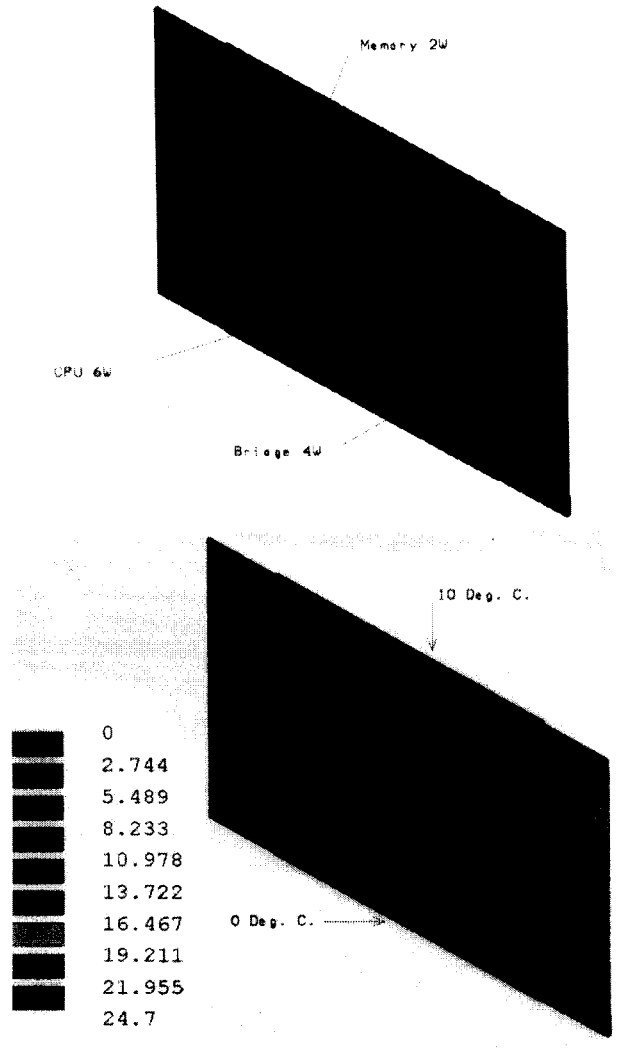




- **Circuit Areas:**
  - **-81.2 mm by 133 mm (~16.75 in_) on each side**
- **Component Height**
  - **-10.0mm (0.393 in) high on one side**
  - **-6.0mm (0.236 in) high on the other side**
- **Board Thickness of 2.0 ± .2 mm (~0.080±.008 in)**

Generic Slice Thermal Analysis

- Assumptions:
- Printed Wiring Board
  - 2mm [.080"] polyimide-glass PWB
  - Three copper planes, 0.0625mm [.0025"] thick
- Wedgelocks
  - Thermal resistance of 2.5 °C / Watt /inch
- Thermal Constraints
  - Upper rail is 10 °C higher than lower rail
  - Total maximum power Dissipation for System Flight Computer is 12 Watts (worst case card).
- Results:
  - Maximum temperature rise of approximately 25 °C referenced to the CPCI chassis lower rails.
  - Acceptable component temperatures were within reach (Tj= ~113°C; PowerPC Package: 2.2°C/Watt), given specific attention to PWB layout and mounting of hot parts.
  - Individual vendors responsible for detailed analysis.

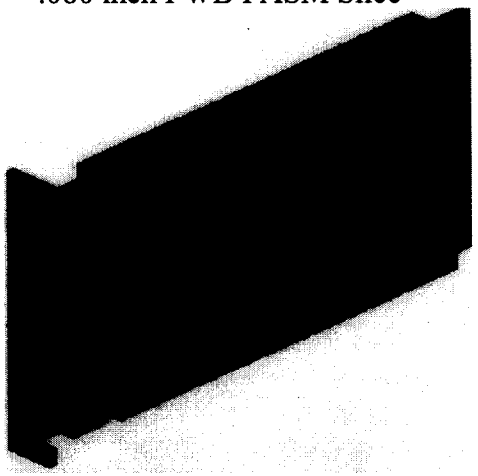


Generic Slice Structural Analysis

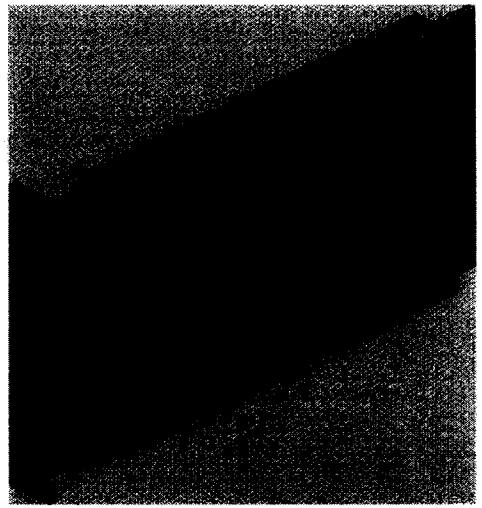
Assumptions:

- Printed Wiring Board
  - Board Thickness 2.0 mm [.080"],
  - Flexural modulus 20.67 x 106 KPa[3 x 106 psi],
  - Specific weight 2.8 g/cm^3 [0.1 lb/in_].
  - Additional component weight totaling 190g.
- Constraints:
  - Power Spectrum Density (PSD) Of 0.2 g^2/Hz.
  - Q=15
  - Wedgelocks between Fixed and Simply Supported.
  - Front Panel Fixed.
  - CPCI Connectors Simply Supported.
- Results
  - 3-sigma deflections of 0.25mm [.010"] acceptable per Steinberg requirements.
  - Natural Frequency of 350 Hz.
  - Individual vendors responsible for detailed analysis.

.080 inch PWB PASM Slice

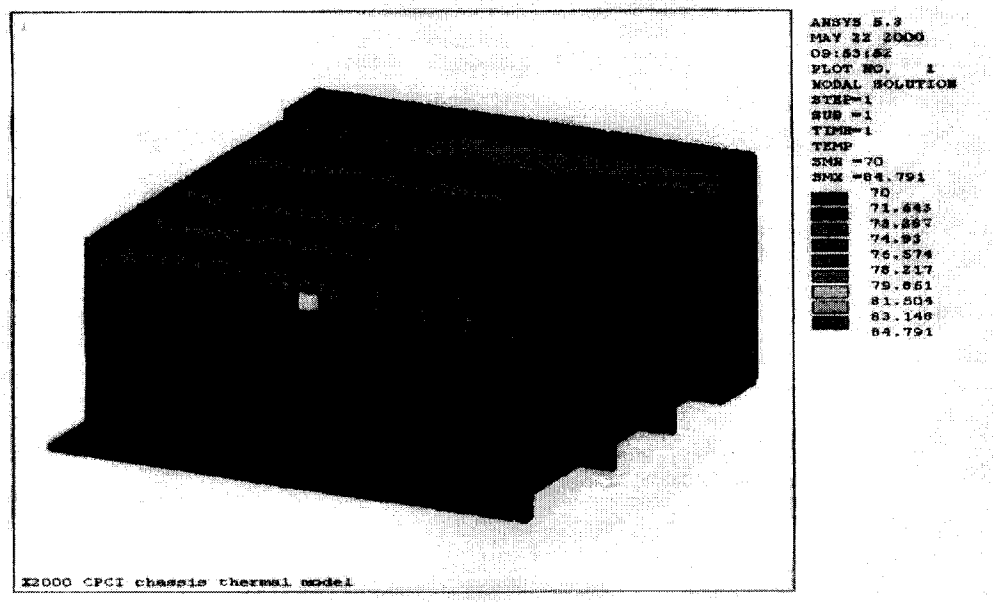


Exaggerated for Clarity



EM Chassis Thermal Analysis

Slice	Watts
1. PCAS	14W
2. TIF	3W
3. SIA	6W
4. SIA	6W
5. SIO	12W
6. Vault material	
7. NVM	3W
8. NVM	3W
9. SFC	15W



Model Detail:

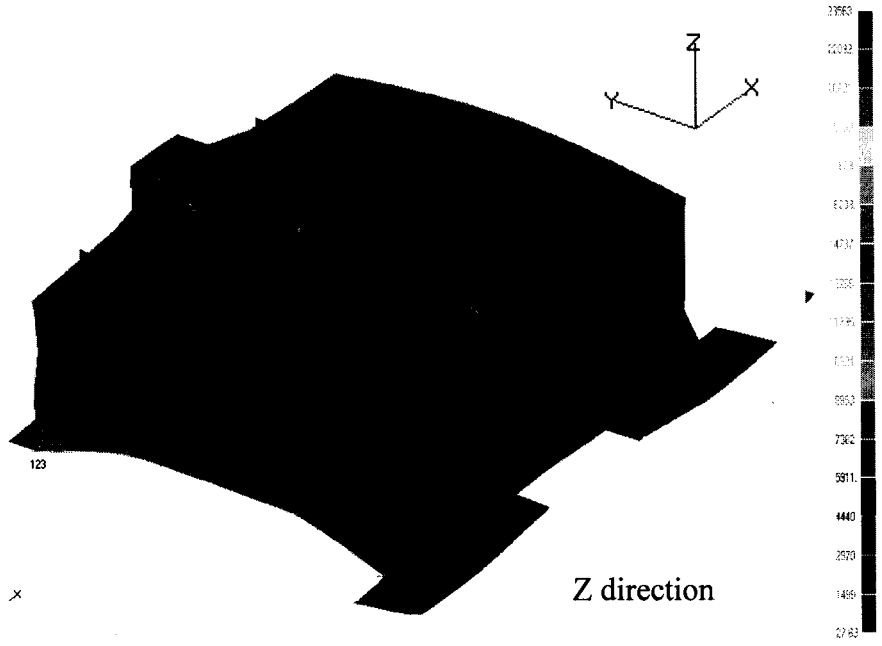
- Heat loads spread over each PWB.
- Total power dissipation of 62 W.
- PWBs conduct heat to chassis through wedgelock thermal resistance 2.5 °C / Watt / inch.
- Chassis conducts to shear plate through several bolted joints, thermal resistance of 1°C / Watt each joint.

Results:

- PWB mounting rails temperature: bottom rails are 75 °C maximum, upper rails are 85 °C maximum, with the assumption of that steady-state temperature for chassis and spacecraft panel interface is 70 °C . This includes RTV used as a thermally conductive agent.

EM Chassis Structural Analysis

Mode	Frequencies	Deflections	Directions
1	125 Hz	0.475mm [0.0187"]	Y
2	146 Hz	0.348mm [0.0137"]	Z
3	177 Hz	0.237mm [0.00934"]	X



Z direction

- Model Details:
- Mass of total model is 49.43 kg (109 pounds)
- Constraints at four corners.
- Loads are Based on Mass Acceleration Curve (MAC) = 18.0 G's
  - Factor of safety of 1.25 for yield.
  - Factor of safety of 1.40 for ultimate.
- Results look at ultimate load of 30 G's:
- Highest stress occurred near attach point and was 184,886 KPa [26,834 psi].
- Corresponding Margin of Safety is +1.38.

Connector Validation Status

- Dynamic Tests: shock (2000g), vibration (.2g^2/Hz), and severe vibration (.4g^2/Hz).
  - Completed showing acceptable results.
  - Report released to the IFDP library.
- Thermal Soak Test: 3000 hours at 125°C
  - 1100 hours complete. Memo written
  - 3000 hours complete. Preliminary results show no problem.
  - Test report to be written.
- Thermal Cycling Test: 200 cycles, -55°C to 125°C
  - Complete except for 1394 connector which needs to be retested.
  - Test report released.
- Current Rating Tests:
  - Completed current rating in air.
  - Current rating transient completed.
  - Current rating in vacuum underway.
  - Results show the CPCI connectors from two manufacturers met the required current carrying capability.
  - Test report released.
  - Results questioned – test being redone with improved design of test setup.

Miscellaneous Status

- Documentation/Drawings:
  - Released 10 Slice MICD's.
  - Released CDH/ACS EM detail chassis drawings.
  - Validation Chassis: Fabrication and Assembly drawings released to PDMS.
- Prototype Hardware
  - Delivered 7 CDH commercial chassis with custom backplanes.
  - Delivered 4 Power commercial chassis with custom backplanes.
  - Delivered Rear I/O slices for TAS, TIF, SIO,SIA, SFC, PCA, PSS.
- Dimpled BGA Qualification
  - Dynamic levels of .2 and .4 G^2/Hz and 2000G shock after 10 cycles –55 to 100 °C.
  - 200 cycles –55 to 100 °C.
  - Results questioned – mass fell off during vibe resulting in intermittent on one of 4 BGA parts (one with dent).

Software Development

Following information provided by: Len Day
Len.Day@jpl.nasa.gov

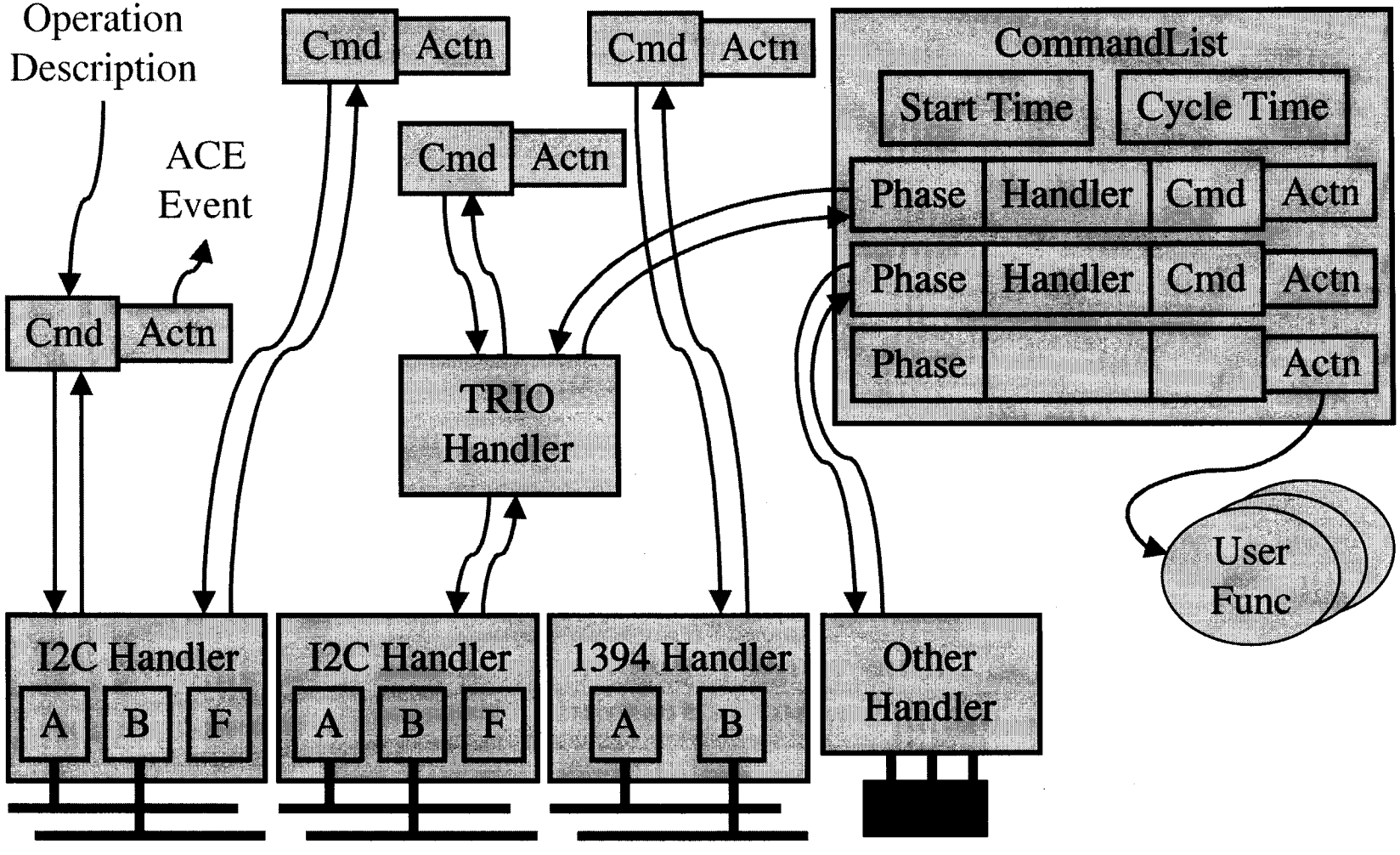
Software Charter

- Among other things the Operating System and Avionics Support team is chartered to:
  - Provide flight device drivers for all X2000 hardware
    - Device drivers to support general device capabilities and not to be mission-specific
  - Use these drivers to support the X2000 hardware integration and test
  - Provide test tool support for testing / exercising the X2000 software and hardware

Software Overview

- Abstract Device Model (ADM)
  - An object oriented framework containing the common code for implementing drivers such as I/O queuing, I/O completion notification, event reporting
  - Concrete instantiations of the ADM for each of the X2000 devices
- A complimentary implementation called "Command Lists" which enables repetitive execution and allows commands for various devices to be executed with specified temporal and other relationships
- A test tool called LLE (Low Level Exerciser) useful for both software and hardware test
- All software designed for portability, using the ACE (Adaptive Computing Environment) layer to insulate from the operating system

Abstract device model



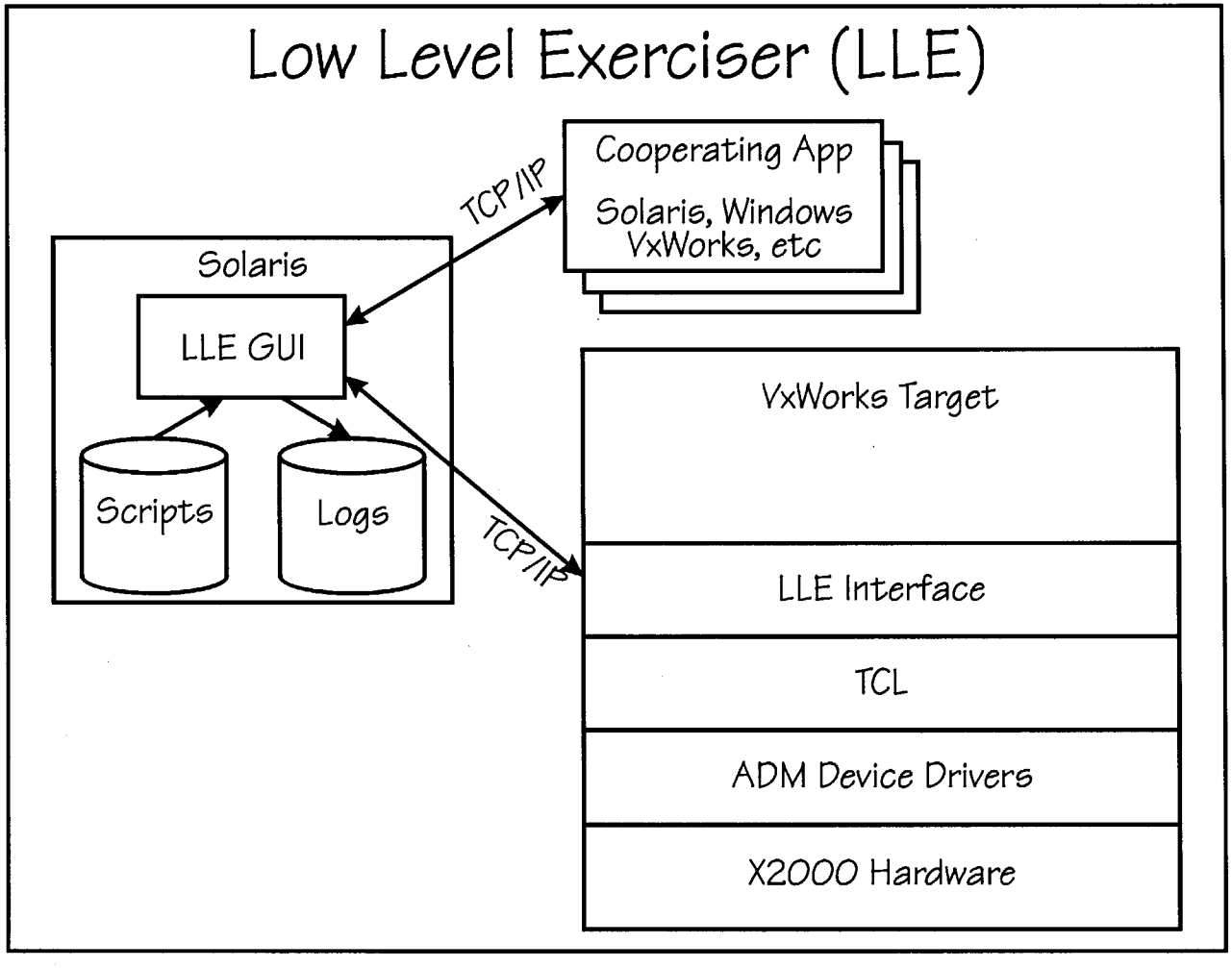
Device drivers

- DIO
  - 4 separate drivers, 1394, I2C, UART and "Custom logic" (timers, discretes)
- SIA
  - Incorporates instrument and telecom serial and 1553 interfaces
- NVM
  - Device driver currently implemented, filesystem implementation planned
- TRIO
- PSS

1394 Hardware Abstraction Layer (HAL)

- Provides access to all 1394 hardware features
- Separate piece of software from the ADM, etc
- Implemented mostly in C
  - C++ parts can be replaced by C code
- Less abstract than the ADM interface
  - ADM interface is implemented on top of the HAL
  - ADM Interface a higher-level view of the isochronous and asynchronous operations and contains address space management.

Test Tools


Low Level Exerciser (LLE)
Cooperating App
Solaris, Windows
VxWorks, etc
TCP/IP
Solaris
LLE GUI
Scripts
Logs
TCP/IP
VxWorks Target
LLE Interface
TCL
ADM Device Drivers
X2000 Hardware

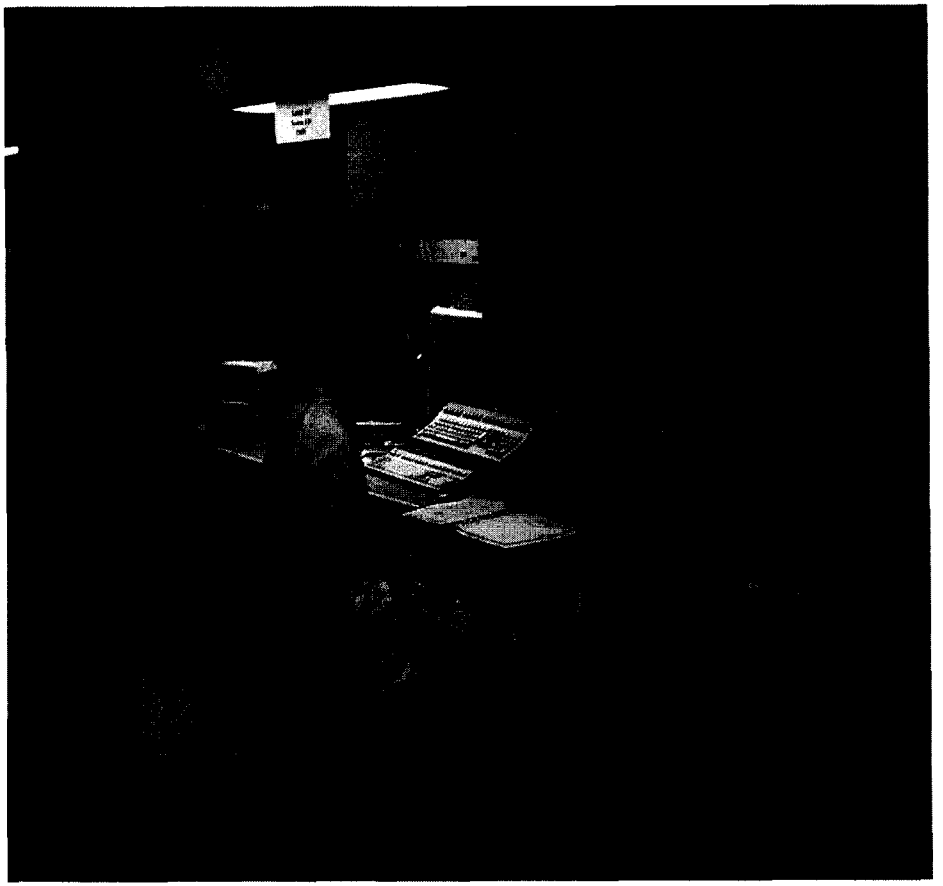
Test Tools, cont.

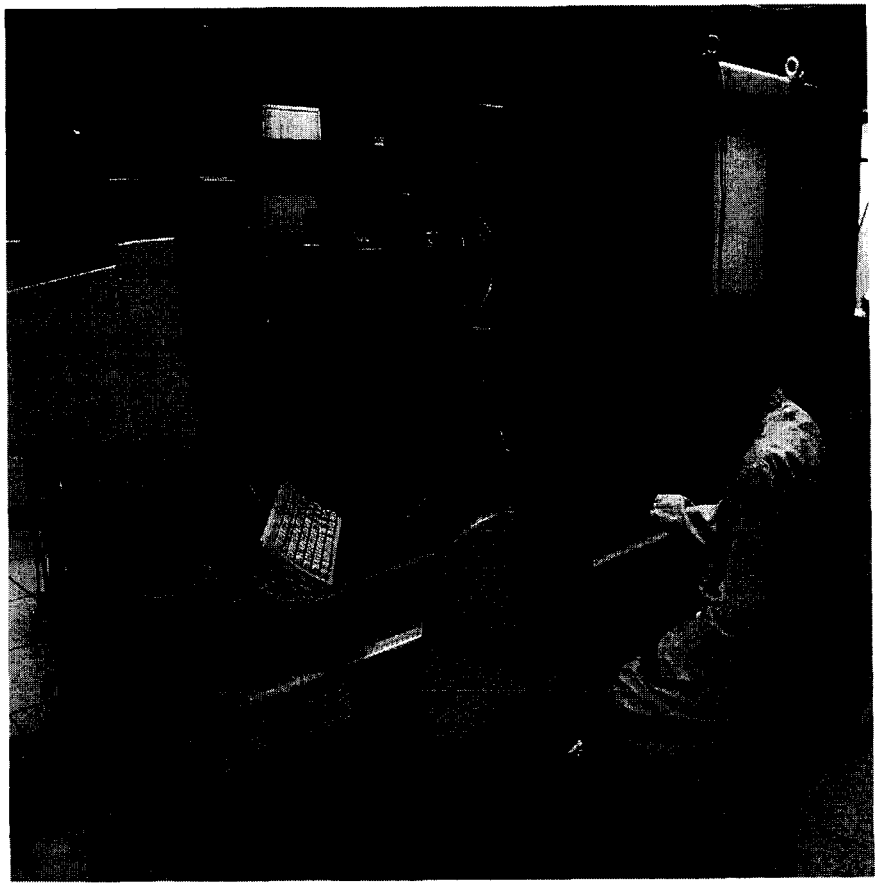
- LLE GUI implemented in TCL/TK
  - Provides command input, script input, timestamped logging to file and the screen
  - Provides interfaces to any number of external applications for transfer of commands and output with coordinated execution / unified log
  - Runs on Unix, Windows, should run on Mac (untested)
- Full software instrumentation / test hooks are provided in the drivers
  - ADM drivers register TCL commands to exercise I/O operations, build and maintain command lists, verify data and I/O status, etc. Commands generally exist to exercise all driver capability from TCL
  - Instrumentation is includable / excludable via #define

Development Status

- All device drivers are complete or are nearing completion
  - All of them run on the X2000 hardware
  - All except I2C and 1394 have been formally delivered. I2C and 1394 essentially done, awaiting resolution of a few questions
  - All drivers are being used on a daily basis to support hardware verification
- LLE is operational and being used extensively for hardware and software test

X2000 Hardware Verification





Following information provided by: Bonnie Theberge

Bonnie.C.Theberge@jpl.nasa.gov

Current Status

- Slice Verification
  - Performed acceptance tests on the following vendor slices
    - NVM, SFC, TAS
  - Performed functional verification of the following JPL-developed slices
    - SIO verification almost complete
      - Verified I2C, UART, Custom Logic, Discretes, PCI - 100%
      - 1394 verification in process - detailed backup material available
    - SIA verification in process
      - All functional interfaces have been verified
      - Detailed checkout in process

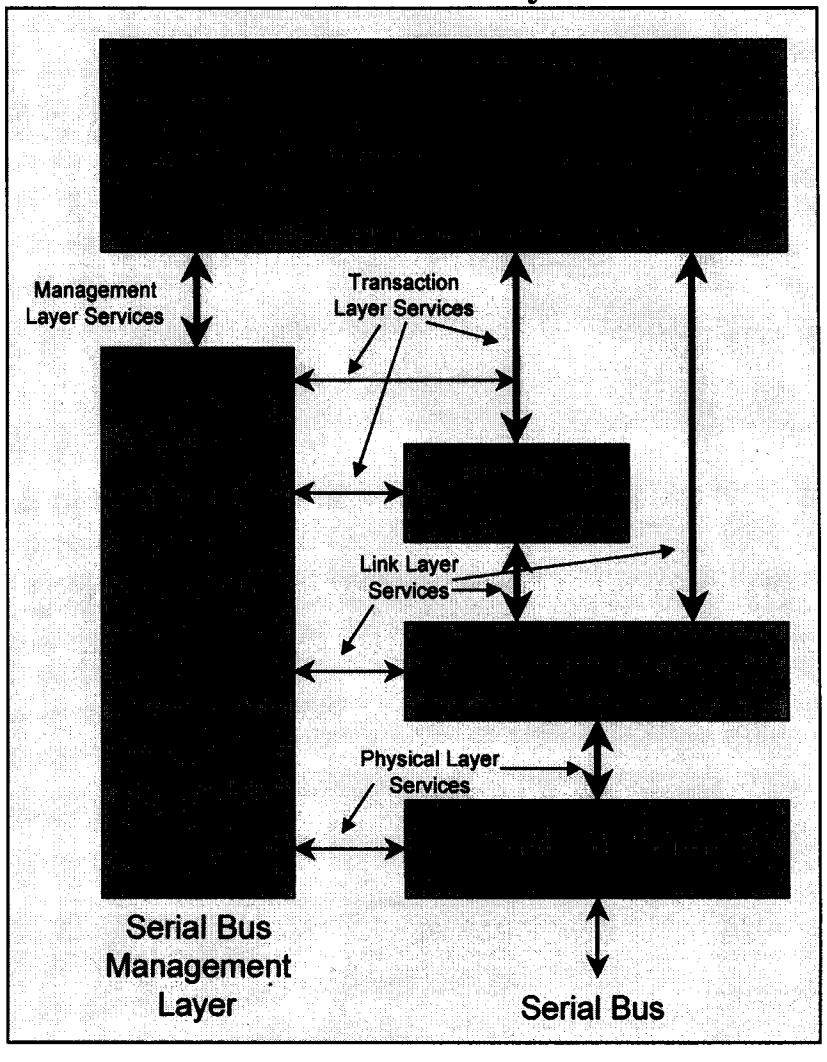
Current Status

- Integration Tests
  - SFC to SIO and SIA through EM backplane
  - SIO to TAS across I2C bus
- Testbed Development
  - Delivered STB-1 Phase 1 (9/00)
    - Single string CDH
    - Used for FSW Driver integration on hardware platform
  - Building up STB-1 Phase 2
    - Dual string CDH
    - Will be used for FSW performance tests
  - Engineering Model testbed STB-2 to be completed 11/02

STB = System Testbed

1394 Hardware and HAL Software

1394 Protocol Layers



- Hardware Abstraction Layer (HAL) software incorporated into flight software
  - HAL software modified for robust space application
  - Flight software being used to verify 1394 functionality and hardware performance
- 1394 Transaction layer being verified
  - Operational verification for nominal and error cases per vendor documentation and 1394 specification
- 1394 link layer being verified
  - Operational verification bits for nominal and error cases per vendor documentation and the 1394 specification
- 1394 Serial Bus layer being verified
  - Self ID and Tree ID process verified

1394 Bus Functionality Verification

- Asynchronous Transfers
  - Successful reads and writes of data payloads of up to 512 bytes in single cycle verified
- Isochronous Transfers
  - Successful transmissions of up to 1024 bytes in single cycle verified
- Asynchronous and Isochronous Transfers
  - Successful Asynchronous transfer with a payload of 512 bytes and Isochronous transfer with a payload of 1024 bytes in single cycle
- Illegal Transfers
  - Illegal transfers detected by hardware and software protection schemes
- DMA transfers to local memory via PCI Bus
  - Automatic DMA transfers of data and commands using PCI bus
- Memory protection
  - Software and hardware memory protection schemes proven and verified