



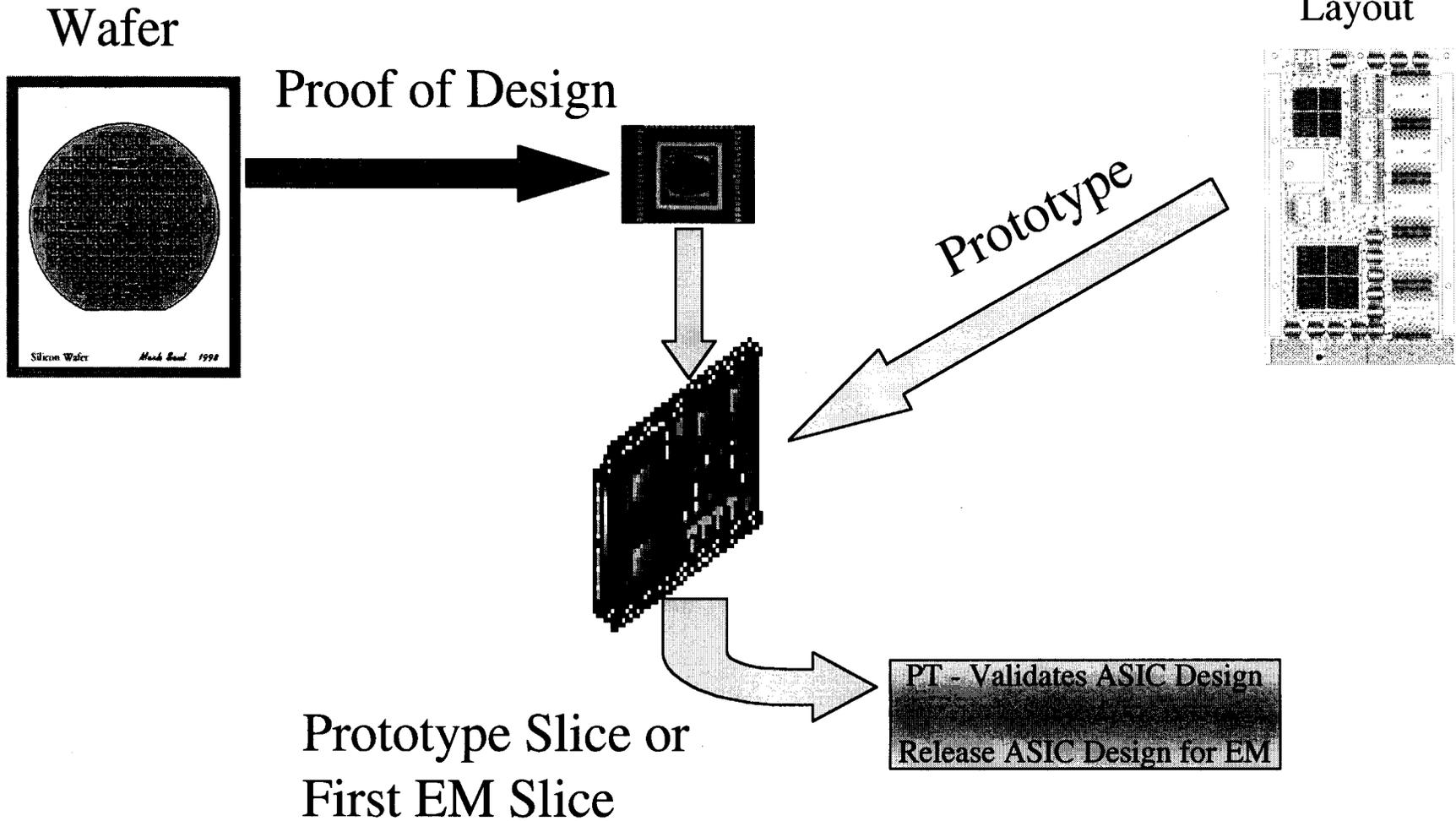
# X2000 Advanced Avionics Development

Randel Blue

February 13, 2002

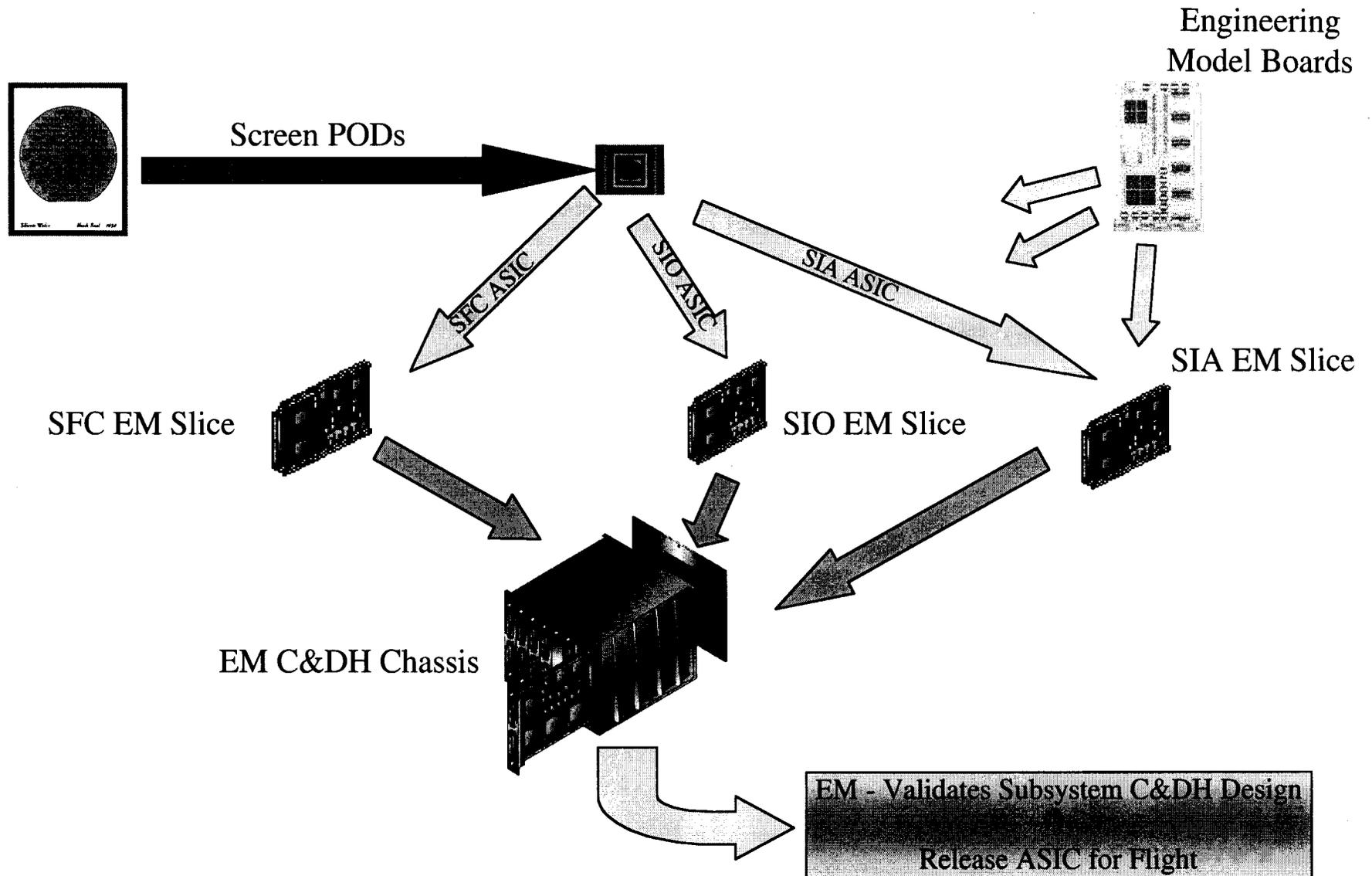


# X2000 CDH Development Phase I



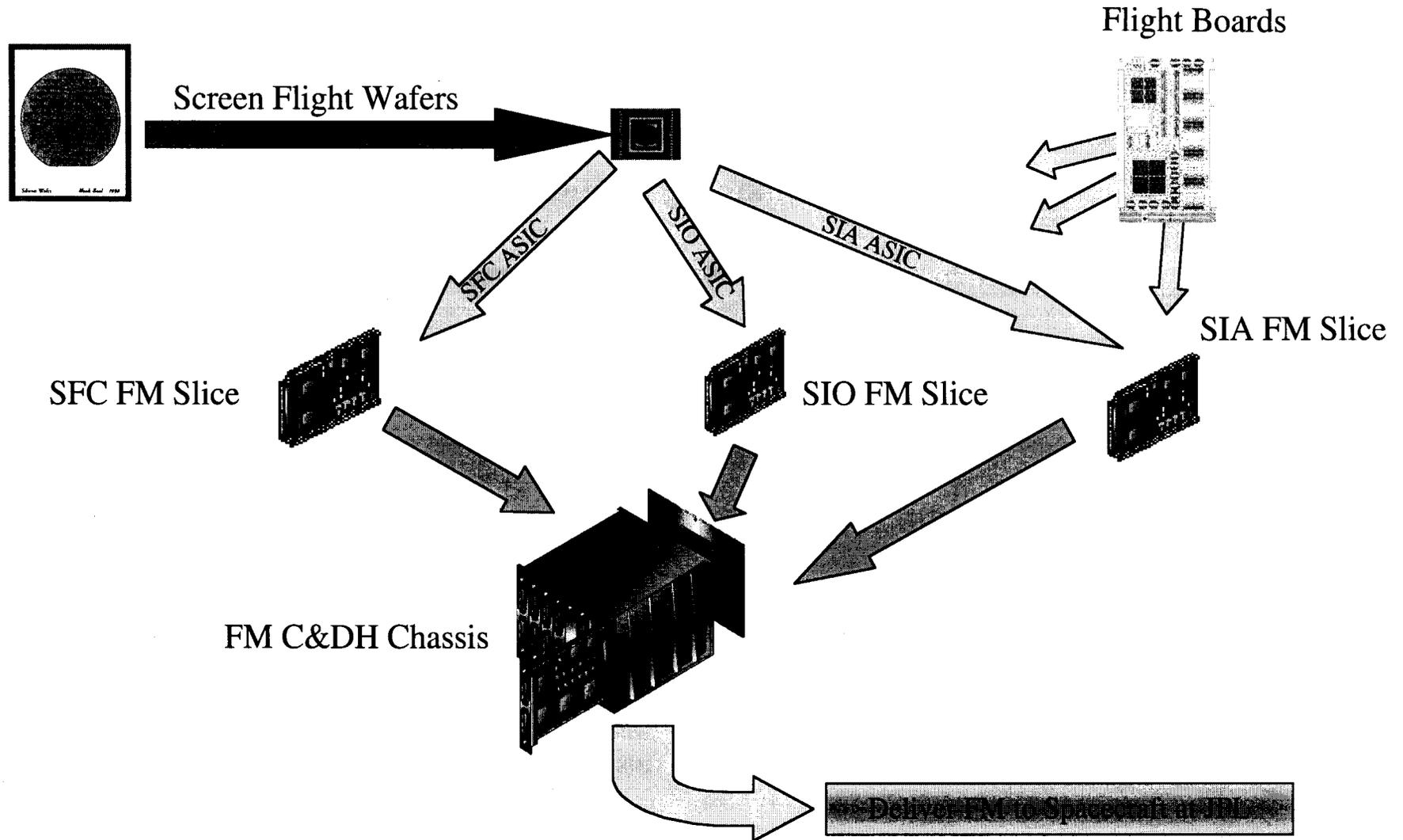


# X2000 CDH Development Phase II





# X2000 CDH Development Phase III



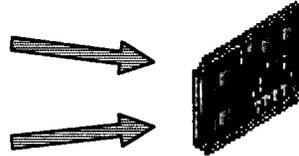


# X2000 Avionics Command & Data Handling Hardware



## PowerPC 750

- Radiation hardened version of G3 processor
- IBM foundry



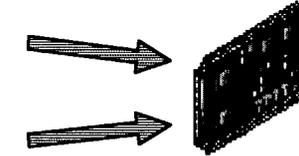
## CPCI Bridge

- Interface between processor and CPCI bus
- BAE & IBM foundry



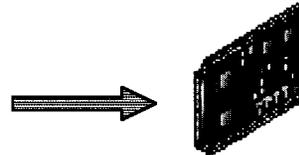
## Digital I/O ASIC

- Bridge between 1394/I<sup>2</sup>C and CPCI bus
- 1394 link layer
- Foundry: Honeywell SSEC, Plymouth MI



## Mixed Signal I/O ASIC

- Physical layer for 1394
- I<sup>2</sup>C driver circuits
- Foundry: Honeywell SSEC, Plymouth MI



## Memory Control ASIC

- Interface memory and CPCI bus
- Includes error correction circuit
- Foundry: Honeywell SSEC, Plymouth MI



## System Interface ASIC

- Interface between CPCI bus and high speed serial I/O for science and telecom
- Foundry: Honeywell SSEC, Plymouth MI



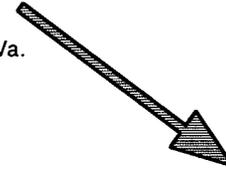
## Temperature Remote I/O ASIC

- Includes 16 analog inputs for telemetry
- I<sup>2</sup>C interface
- Foundry: Honeywell SSEC, Plymouth MI



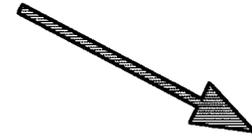
## SFC - System Flight Computer

- PowerPC 750 Compact PCI based
- 128 Mbytes DRAM; 256Kbytes EEPROM
- Baseline 240 MIPs; variable speed
- Contractor: BAE Systems, Manassas, Va.



## SIO - System Input/Output

- PCI/1394/I<sup>2</sup>C Bridge; 2 UARTs
- Includes node reset control; general fault protection logic; discretes
- Assembly developed at JPL



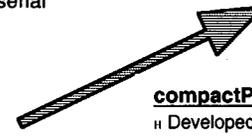
## NVM - Non Volatile Memory

- 2 Gbit/slice Flash Memory
- Includes power management control and erase/write cycle tally
- Contractor: SEAKR Engineering, Littleton Co.



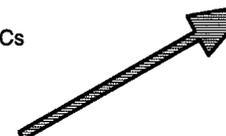
## SIA - System Interface Assembly

- Includes 1553, SPI and high speed serial interfaces
- Assembly developed at JPL



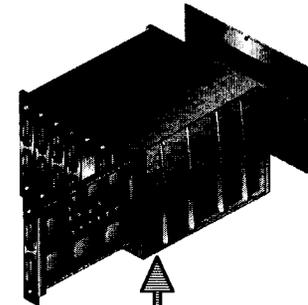
## TAS - TRIO Assembly Slice

- Temperature and analog collection
- 6 Temperature Remote I/O (TRIO) ASICs split between 2 I<sup>2</sup>C buses
- 96 telemetry channels; 10 bit A/D
- Contractor: Johns Hopkins University/Applied Physics Laboratory



## compactPCI Chassis

- Commercial standard, first space application
- Developed at JPL



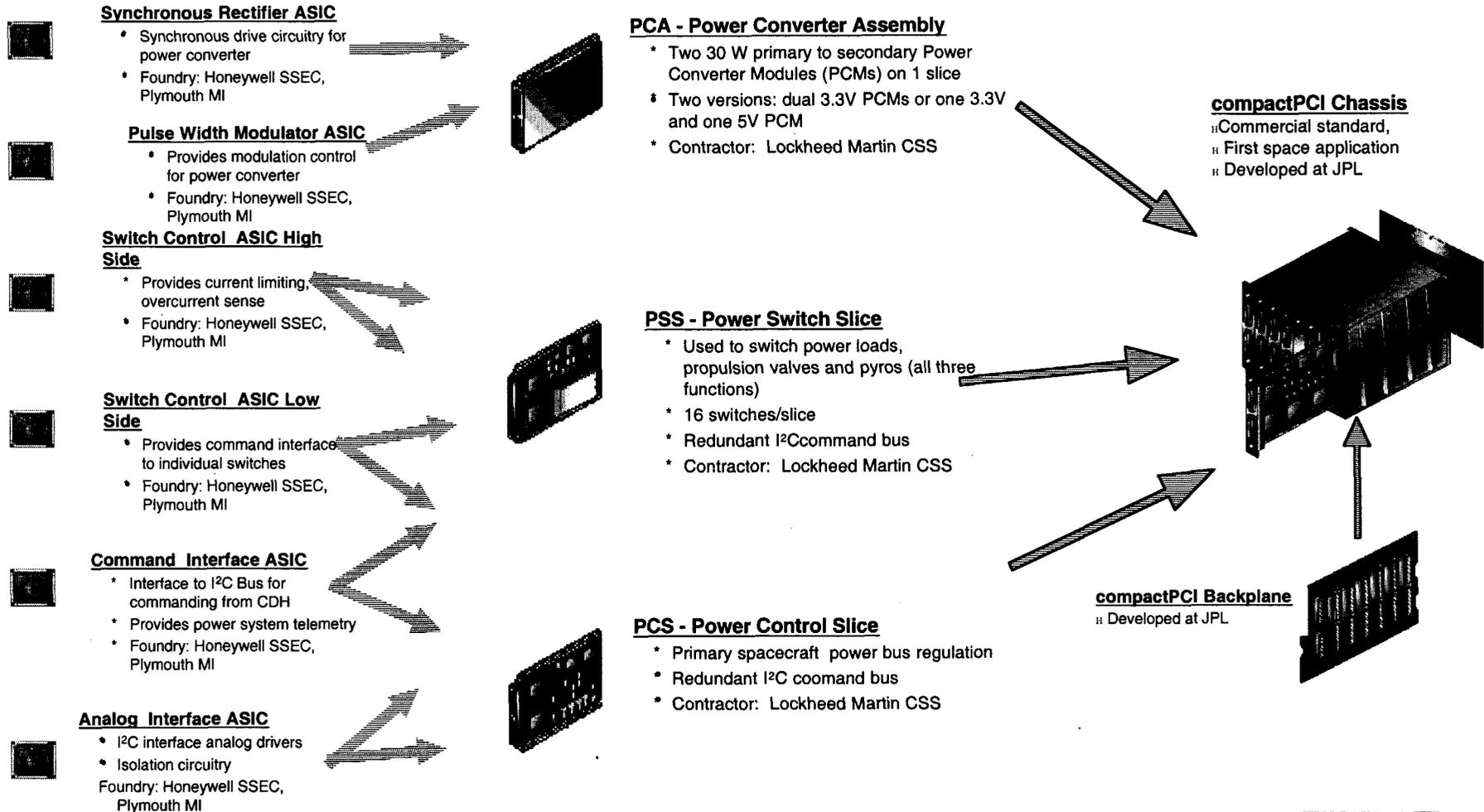
## compactPCI Backplane

- Developed at JPL

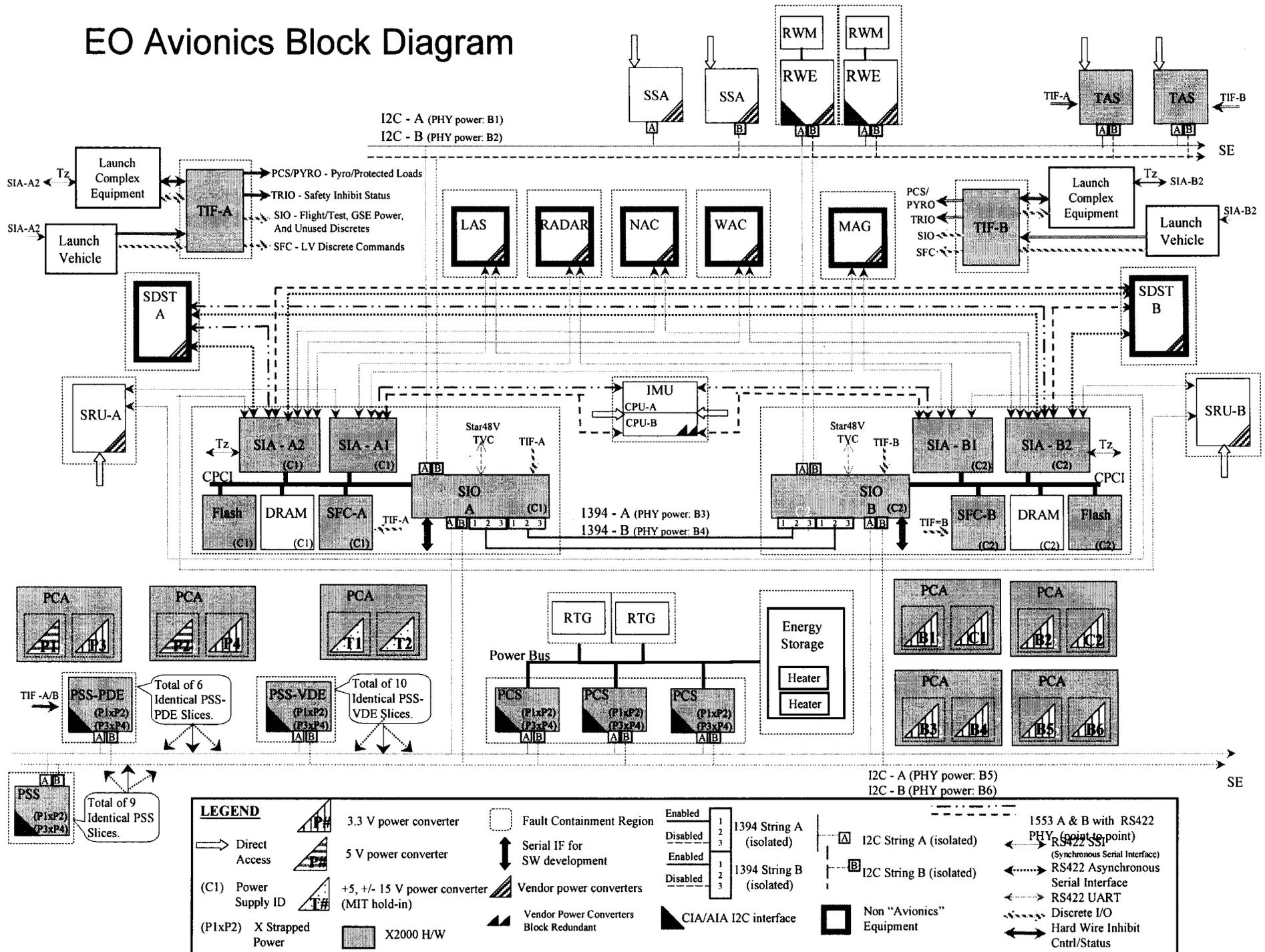




# Europa Orbiter/X2000 Avionics Power System Hardware



# EO Avionics Block Diagram





# X2000 Development Status and Plan

- **System Flight Computer**
- Successfully completed Qualification testing in September of 2001
- Engineering models have been delivered to JPL
- First delivery of X2000 SFC for flight to Deep Impact mission scheduled for April 3, 2002
- Contract to produce SFC with enhanced version of PCI bridge chip is continuing
  - Will provide on board DMA capability and faster internal clock rates
  - First enhanced SFC scheduled for delivery February, 2003
- **System Input/Output Assembly**
- Mixed Signal I/O ASIC in fab at Honeywell
  - Provides electrical isolation of physical layer of I2C and 1394 buses
  - Proof of design ASICs expected mid-July
- Digital I/O ASIC design is completing, fabrication start in May
  - Includes link layer of I2C and 1394
  - Connects PCI bus to I2C and 1394 serial buses



# X2000 Development Status and Plan

- **Non-Volatile Memory Slice**
- Successfully completed environmental qualification tests December 2001
- First five EM NVM slices delivered to Deep Impact October 2001; Five EMs to Europa January 2002
- First Deep Impact flight models scheduled for delivery March 19, 2002
  - Flight ASICS are in burn-in at Honeywell
- Characterization of flash memories for erratic programming phenomenon is continuing
  - Currently at ~70,000 erase/write cycles, very low incidence of erratic programming
  - Flight requirement is less than 10,000 cycles
- **System Interface Assembly**
- SIA board and ASIC development has been completed and verified
  - Stress testing is underway, expected completion Q2 FY02
- SIA has been integrated into test chassis with X2000 SFC
- SIA ASIC CDR planned for December 2002, first EM August 2003
  - Delay is due to funding profile constraints



# Command & Data Handling Subsystem ASICs



	ASIC	Function	Slice	Designed By	Proc By	Fab By	Fab Line Type	Gate Count	Pin Count	Status
1	Power PCI Bridge Chip	Bridge between the Compact PCI (cPCI) bus, memory (EEPROM, SDRAM) and the RAD750 processor. Includes UART and JTAG interfaces for software support and diagnostics.	SFC	BAE	BAE	BAE	Digital	700K	624	Fab run completed.
2	RAD750	Rad hard version of the PowerPC 750 processor.	SFC	BAE	BAE	BAE	Digital	10M Transistors	360	Fab run completed 5/01.
3	DIO (Digital I/O)	Bridge between the 1394/I <sup>2</sup> C buses and the cPCI bus. Implements the link layer of the 1394 bus, the two I <sup>2</sup> C bus controllers, and logic for fault tolerance enhancements. Includes a UART to support software development and discrete I/O signals for miscella	SIO	JPL + Mentor/ISI	JPL	Honeywell SSEC	Gate Array HX311G	170K gates + 250Kb RAM	220 Sig 100 Pwr	Design complete, synthesis inprocess , fab start 5/02
4	MSIO (Mixed Signal I/O)	Implements the physical layer of the 1394 bus and the drivers of the I <sup>2</sup> C buses.	SIO	SSEC/DMC + Mentor/ISI + JPL	JPL	Honeywell SSEC	Mixed Signal HX2300	50K gates + analog 1394 I/I	200 Sig 150 Pwr	In fab at Honeywell
5	SIA (System Interface ASIC)	Provides interface between the cPCI bus, the 1553 bus controller ASIC, buffer memory (SRAM), SDST (RS422) and 4 high speed serial interfaces (instruments/sensors).	SIA	JPL + Asgard ASIC	JPL	Honeywell SSEC	Digital HX311G			FPGA version in checkout.
6	Memory Controller ASIC	Interface between cPCI bus and memory (flash). Includes Reed Solomon EDAC and flash power control.	NVM	SEAKR	SEAKR	Honeywell SSEC	Digital HX2160	~70K		ASIC fabrication complete.
7	TRIO (Temperature Remote I/O)	Includes 16 analog inputs for temperature or voltage measurement, 10 bit ADC and I2C interface.	TAS	APL	APL	Honeywell SSEC	Custom RIMOS4	~46K	84	ASIC fabrication complete.

NOTES:  
 All ASICs are 1 Mrad except as noted  
 ASICs to be fabricated via the JPL Multifab Contract



# Power Subsystem ASICs



	ASIC	Function	Slice	Designed By	Proc By	Fab By	Fab Line Type	Gate Count	Pin Count	Status
1	SCAH (Switch Control ASIC High)	Provides the floating current limit, overcurrent trip and MOSFET drive function for the power switch inside the PASM.	PSS PCS	Boeing/JPL	JPL	Honeywell SSEC	Mixed HX2040	<10K	60	CDR on 5/15/02.
2	SCAL (Switch Control ASIC Low)	Provides the ground referenced command I/F and charge pump for the power switch inside the PASM.	PSS PCS	Boeing/JPL	JPL	Honeywell SSEC	Mixed HX2040	<10K	60	CDR on 5/15/02.
3	PWMA (Pulse-Width Modulator ASIC)	Provides pulse width modulation control for a dual forward topology on the primary side of the Power Converter Module (PCM).	PCA	Boeing	JPL	Honeywell SSEC	Mixed HX2080	<10K	128	Completed fabrication of the first pass on 12/15/00. The part is fully functional with the exception of the autozero amplifier. Part deleted from PCA design
4	SRCA (Synchronous Rectifier ASIC)	Provides synchronous rectifier drive and output voltage and current sense on the secondary side of the PCM.	PCA	Boeing	JPL	Honeywell SSEC	Mixed HX2040	<10K	60	Completed fabrication of the first pass on 12/15/00. The part is fully functional with the exception of a POR timing issue. Part deleted from PCA design
5	AIA (Analog Interface ASIC)	Provides the system I2C bus interface and chops the signal across transformers for isolated interface with the CIA.	PSS PCS	JPL + SSEC	JPL	Honeywell SSEC	Custom HX2040	~20K	33 Sig 20 Grd	CDR held January 2002.
6	CIA (Command Interface ASIC)	Provides local command and control for the PCS and PSS including A/D conversion.	PSS PCS	JPL + SSEC	JPL	Honeywell SSEC	Mixed HX2300	87K gates + 1Kb RAM + 64Kb ROM	184 Sig 50 Grd	CDR on 8/15/02.

**NOTES:**

All ASICs 1 Mrad unless otherwise noted

ASICs to be fabricated via the JPL Multifab Contract



# Command & Data Handling ASIC Status



#	ASIC	Slice	PDR	CDR	Mask Release	PODs	EMs	FMs	Comments
1a.	Power PCI Bridge Chip RIT A	SFC	●	●	●	●	●	N/A	RIT A is not planned to be used for flight
1b.	Power PCI Bridge Chip RIT B	SFC	-	-	●	●	▲	▲	
1c.	Power PCI Bridge Chip Enhanced Version	SFC			12/16/02	4/17/03	5/1/03	7/15/03	
2	RAD750	SFC	●	●	●	●	●	▲	
3	DIO (Digital I/O)	SIO	-	5/3/02	5/24/02	9/23/020	11/26/02	8/15/03	
4	MSIO (Mixed Signal I/O)	SIO	●	●	▲	7/16/02	8/20/02	8/1/03	PODs and EM delayed, not critical path
5	SIA (System Interface ASIC)	SIA	●	11/27/02	12/17/02	7/8/03	9/4/03	9/10/03	
6	Memory Controller ASIC	NVM	●	●	●	●	●	2/22/02	Flight ASICS delayed at foundry
7a.	TRIO - Rev. A (Temperature Remote I/O)	TAS	●	●	●	●	●	N/A	Rev. A is not planned to be used for flight
7b.	TRIO - Rev. B (Temperature Remote I/O)	TAS	-	-	●	N/A	●	●	ASIC fab complete, delays in packaging

**DEFINITIONS:**

Mask Release - start of fabrication at the foundry  
 PODs - Proof-of-Design parts  
 EMs - Engineering Model Parts  
 FMs - Flight Parts

SFC - System Flight Computer  
 SIO - System I/O  
 NVM - Non-Volatile Memory  
 TAS - TRIO Assembly Slice  
 SIA - System I/F Assembly



Completed this Quarter



# Power System ASIC Status

#	ASIC	Slice	PDR	CDR	Mask Release	PODs	EMs	FMs	Comments
1	SCAH (Switch Control ASIC High)	PSS PCS	●	● Delta 5/13/02	11/20/02	6/2/03	11/15/04	12/28/04	EM and FM dates extended due to PASM fab
2	SCAL (Switch Control ASIC Low)	PSS PCS	●	● Delta 5/13/02	11/20/02	6/2/03	11/15/04	12/28/04	EM and FM dates extended due to PASM fab
3	PWMA (Pulse-Width Modulator ASIC)	PCA	●	●	●	●			First pass completed Deleted from PCA design
4	SRCA (Synchronous Rectifier ASIC)	PCA	●	●	●	●			First pass completed Deleted from PCA design
5	AIA (Analog Interface ASIC)	PSS PCS	●	▲	11/20/02	6/13/03	2/15/05	10/3/05	
6	CIA (Command Interface ASIC)	PSS PCS	●	8/15/02	12/1/03	5/27/04	2/15/05	10/3/05	

**DEFINITIONS:**

Mask Release - start of fabrication at the foundry  
 PODs - Proof-of-Design parts  
 EMs - Engineering Model Parts  
 FMs - Flight Parts

PSS - Power Switch Slice  
 PCS - Power Control Slice  
 PCA - Power Converter Assembly

▲ Completed this month