X2000 Advanced Avionics Development

Randel Blue

February 13, 2002
X2000 CDH Development
Phase I

Proof of Design

Prototype Slice or First EM Slice

PT - Validates ASIC Design
Release ASIC Design for EM

3U Board Layout
X2000 CDH Development
Phase III

Screen Flight Wafers

SFC FM Slice

SFC ASIC

SD ASIC

SIO ASIC

SIA FM Slice

FM C&DH Chassis

Flight Boards

Delivered to spacecraft interface
X2000 Avionics
Command & Data Handling Hardware

PowerPC 750
* Radiation hardened version of G3 processor
* IBM foundry

CPCI Bridge
* Interface between processor and CPCI bus
* BAE & IBM foundry

Digital I/O ASIC
* Bridge between 1394/iPC and CPCI bus
* 1394 link layer
* Foundry: Honeywell SSEC, Plymouth MI

Mixed Signal I/O ASIC
* Physical layer for 1394
* PCI driver circuits
* Foundry: Honeywell SSEC, Plymouth MI

Memory Control ASIC
* Interface memory and CPCI bus
* Includes error correction circuit
* Foundry: Honeywell SSEC, Plymouth MI

System Interface ASIC
* Interface between CPCI bus and high speed serial I/O for science and telecom
* Foundry: Honeywell SSEC, Plymouth MI

Temperature Remote I/O ASIC
* Includes 16 analog inputs for telemetry
* PCI interface
* Foundry: Honeywell SSEC, Plymouth MI

SFC - System Flight Computer
* PowerPC 750 Compact PCI based
* 128 Mbytes DRAM; 256Kbytes EEPROM
* Baseline 240 MIPS; variable speed
* Contractor: BAE Systems, Manasas, Va.

SIO - System Input/Output
* PCI/1394/iPC Bridge; 2 UARTs
* Includes node reset control; general fault protection logic; discretes
* Assembly developed at JPL

NVM - Non Volatile Memory
* 2 Gbit/slice Flash Memory
* Includes power management control and erase/write cycle tally
* Contractor: SEAKR Engineering, Littleton Co.

SIA - System Interface Assembly
* Includes 1553, SPI and high speed serial interfaces
* Assembly developed at JPL

TAS - TRIO Assembly Slice
* Temperature and analog collection
* 6 Temperature Remote I/O (TRIO) ASiCs split between 2 iPC buses
* 96 telemetry channels; 10 bit A/D
* Contractor: Johns Hopkins University/Applied Physics Laboratory

compactPCI Chassis
= Commercial standard, first space application
= Developed at JPL

compactPCI Backplane
= Developed at JPL
Europa Orbiter/X2000 Avionics
Power System Hardware

**Synchronous Rectifier ASIC**
- Synchronous drive circuitry for power converter
- Foundry: Honeywell SSEC, Plymouth MI

**Pulse Width Modulator ASIC**
- Provides modulation control for power converter
- Foundry: Honeywell SSEC, Plymouth MI

**Switch Control ASIC High Side**
- Provides current limiting, overcurrent sense
- Foundry: Honeywell SSEC, Plymouth MI

**Switch Control ASIC Low Side**
- Provides command interface to individual switches
- Foundry: Honeywell SSEC, Plymouth MI

**Command Interface ASIC**
- Interface to PC Bus for commanding from CDH
- Provides power system telemetry
- Foundry: Honeywell SSEC, Plymouth MI

**Analog Interface ASIC**
- PC interface analog drivers
- Isolation circuitry
- Foundry: Honeywell SSEC, Plymouth MI

**PCA - Power Converter Assembly**
- Two 30 W primary to secondary Power Converter Modules (PCMs) on 1 slice
- Two versions: dual 3.3V PCMs or one 3.3V and one 5V PCM
- Contractor: Lockheed Martin CSS

**PSS - Power Switch Slice**
- Used to switch power loads, propulsion valves and pyros (all three functions)
- 16 switches/slice
- Redundant I2C command bus
- Contractor: Lockheed Martin CSS

**PCS - Power Control Slice**
- Primary spacecraft power bus regulation
- Redundant I2C command bus
- Contractor: Lockheed Martin CSS

**compactPCI Chassis**
- Commercial standard
- First space application
- Developed at JPL

**compactPCI Backplane**
- Developed at JPL

PCA - Power Converter Assembly
- Two 30 W primary to secondary Power Converter Modules (PCMs) on 1 slice
- Two versions: dual 3.3V PCMs or one 3.3V and one 5V PCM
- Contractor: Lockheed Martin CSS

**compactPCI Chassis**
- Commercial standard
- First space application
- Developed at JPL

**compactPCI Backplane**
- Developed at JPL
EO Avionics Block Diagram

Legend:
- Direct Access
- 3.3 V power converter
- 5 V power converter
- +5, +/-15 V power converter (MIT hold-in)
- Vendor power converters
- Fault Containment Region
- Serial I/F for SW development
- 1394 String A (isolated)
- 1394 String B (isolated)
- ISA/IAIA I2C interface
- Non "Avionics" Equipment
- 1553 A & B with RS422 PHY (point to point)
- Synchronous Serial Interface
- Asynchronous Serial Interface
- RS422 UART
- Hardwire inhibit
- Card/Status

Launch Complex Equipment

TIF-A

I2C - A (PHY power: B1)
I2C - B (PHY power: B2)

PCS/PYRO - Pyro/Protected Loads
TRIO - Safety Inhibit Status
SIO - Flight/Test, GSE Power, And Unused Discretes
SFC - LV Discrete Commands

LAS
RADAR
NAC
WAC
MAG

TIF-B

Launch Complex Equipment

SRU-A

SIA-A1

I2C - A (PHY power: B1)
I2C - B (PHY power: B2)

PCA

Total of 6 Identical PSS-PDE Slices.

RTG

Total of 10 Identical PSS-VDE Slices.

PCA

Power Bus

PCA

Total of 9 Identical PSS-PDE Slices.

PCA

3.3 V power converter

5 V power converter

+5, +/-15 V power converter (MIT hold-in)

Vendor power converters

Fault Containment Region

Serial I/F for SW development

1394 String A (isolated)

1394 String B (isolated)

ISA/IAIA I2C interface

Non "Avionics" Equipment

1553 A & B with RS422 PHY (point to point)

Synchronous Serial Interface

Asynchronous Serial Interface

RS422 UART

Hardwire inhibit

Card/Status
X2000 Development Status and Plan

- **System Flight Computer**
  - Successfully completed Qualification testing in September of 2001
  - Engineering models have been delivered to JPL
  - First delivery of X2000 SFC for flight to Deep Impact mission scheduled for April 3, 2002
  - Contract to produce SFC with enhanced version of PCI bridge chip is continuing
  - Will provide on board DMA capability and faster internal clock rates
  - First enhanced SFC scheduled for delivery February, 2003

- **System Input/Output Assembly**
  - Mixed Signal I/O ASIC in fab at Honeywell
  - Provides electrical isolation of physical layer of I2C and 1394 buses
  - Proof of design ASICs expected mid-July
  - Digital I/O ASIC design is completing, fabrication start in May
  - Includes link layer of I2C and 1394
  - Connects PCI bus to I2C and 1394 serial buses
X2000 Development Status and Plan

- **Non-Volatile Memory Slice**
  - Successfully completed environmental qualification tests December 2001
  - First five EM NVM slices delivered to Deep Impact October 2001; Five EMs to Europa January 2002
  - First Deep Impact flight models scheduled for delivery March 19, 2002
    - Flight ASICS are in burn-in at Honeywell
  - Characterization of flash memories for erratic programming phenomenon is continuing
    - Currently at ~70,000 erase/write cycles, very low incidence of erratic programming
    - Flight requirement is less than 10,000 cycles

- **System Interface Assembly**
  - SIA board and ASIC development has been completed and verified
    - Stress testing is underway, expected completion Q2 FY02
  - SIA has been integrated into test chassis with X2000 SFC
  - SIA ASIC CDR planned for December 2002, first EM August 2003
    - Delay is due to funding profile constraints
## Command & Data Handling Subsystem ASICs

<table>
<thead>
<tr>
<th>ASIC</th>
<th>Function</th>
<th>Slice</th>
<th>Designer By</th>
<th>Proc By</th>
<th>Fab By</th>
<th>Fab Line Type</th>
<th>Gate Count</th>
<th>Pin Count</th>
<th>Status</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Power PCI Bridge Chip</td>
<td>Bridge between the Compact PCI (cPCI) bus, memory (EEPROM, SDRAM) and the RAD750 processor. Includes UART and JTAG interfaces for software support and diagnostics.</td>
<td>SFC</td>
<td>BAE</td>
<td>BAE</td>
<td>Digital</td>
<td>700K</td>
<td>624</td>
<td>Fab run completed.</td>
</tr>
<tr>
<td>2</td>
<td>RAD750</td>
<td>Rad hard version of the PowerPC 750 processor.</td>
<td>SFC</td>
<td>BAE</td>
<td>BAE</td>
<td>Digital</td>
<td>10M Transistors</td>
<td>360</td>
<td>Fab run completed 5/01.</td>
</tr>
<tr>
<td>3</td>
<td>DIO (Digital I/O)</td>
<td>Bridge between the 1394/12C buses and the cPCI bus. Implements the link layer of the 1394 bus, the two 12C bus controllers, and logic for fault tolerance enhancements. Includes a UART to support software development and discrete I/O signals for miscellaneous.</td>
<td>SIO</td>
<td>JPL + Mentor/SI</td>
<td>JPL</td>
<td>Honeywell</td>
<td>SSEC</td>
<td>Gate Array HX311G</td>
<td>170K gates + 25K6 RAM</td>
</tr>
<tr>
<td>4</td>
<td>MSIO (Mixed Signal I/O)</td>
<td>Implements the physical layer of the 1394 bus and the drivers of the 12C buses.</td>
<td>SIO</td>
<td>SSEC/DMC + Mentor/SI + JPL</td>
<td>JPL</td>
<td>Honeywell</td>
<td>SSEC</td>
<td>Mixed Signal HX2300</td>
<td>50K gates + analog 1394 M</td>
</tr>
<tr>
<td>5</td>
<td>SIA (System Interface ASIC)</td>
<td>Provides interface between the cPCI bus, the 1553 bus controller ASIC, buffer memory (SRAM), SOST (RS422) and 4 high speed serial interfaces (instruments/sensors).</td>
<td>SIA</td>
<td>JPL + Asgard ASIC</td>
<td>JPL</td>
<td>Honeywell</td>
<td>SSEC</td>
<td>Digital HX311G</td>
<td>FPGA version in checkout.</td>
</tr>
<tr>
<td>5</td>
<td>Memory Controller ASIC</td>
<td>Interface between cPCI bus and memory (flash). Includes Reed Solomon EDAC and flash power control.</td>
<td>NVM</td>
<td>SEAKR</td>
<td>SEAKR</td>
<td>Honeywell</td>
<td>SSEC</td>
<td>Digital HX2160</td>
<td>-70K</td>
</tr>
<tr>
<td>7</td>
<td>TRIO (Temperature Remote I/O)</td>
<td>Includes 16 analog inputs for temperature or voltage measurement, 10 bit ADC and I2C interface.</td>
<td>TAS</td>
<td>APL</td>
<td>APL</td>
<td>Honeywell</td>
<td>SSEC</td>
<td>Custom RICMOS4</td>
<td>-46K</td>
</tr>
</tbody>
</table>

**NOTES:**
- All ASICs are 1 Mrad except as noted.
- ASICs to be fabricated via the JPL Multifab Contract.
# Power Subsystem ASICs

<table>
<thead>
<tr>
<th>ASIC</th>
<th>Function</th>
<th>Slice</th>
<th>Designed By</th>
<th>Proc By</th>
<th>Fab By</th>
<th>Fab Line Type</th>
<th>Gate Count</th>
<th>Pin Count</th>
<th>Status</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 SCAH (Switch Control ASIC High)</td>
<td>Provides the floating current limit, overcurrent trip and MOSFET drive function for the power switch inside the PASM.</td>
<td>PSS PCS</td>
<td>Boeing/JPL</td>
<td>JPL</td>
<td>Honeywell SSEC</td>
<td>Mixed HX2040</td>
<td>&lt;10K</td>
<td>60</td>
<td>CDR on 5/15/02.</td>
</tr>
<tr>
<td>2 SCAL (Switch Control ASIC Low)</td>
<td>Provides the ground referenced command VIF and charge pump for the power switch inside the PASM.</td>
<td>PSS PCS</td>
<td>Boeing/JPL</td>
<td>JPL</td>
<td>Honeywell SSEC</td>
<td>Mixed HX2040</td>
<td>&lt;10K</td>
<td>60</td>
<td>CDR on 5/15/02.</td>
</tr>
<tr>
<td>3 PWMA (Pulse-Width Modulator ASIC)</td>
<td>Provides pulse width modulation control for a dual forward topology on the primary side of the Power Converter Module (PCM).</td>
<td>PCA</td>
<td>Boeing</td>
<td>JPL</td>
<td>Honeywell SSEC</td>
<td>Mixed HX2060</td>
<td>&lt;10K</td>
<td>128</td>
<td>Completed fabrication of the first pass on 12/15/00. The part is fully functional with the exception of the autozero amplifier. Part deleted from PCA design</td>
</tr>
<tr>
<td>4 SRCA (Synchronous Rectifier ASIC)</td>
<td>Provides synchronous rectification drive and output voltage and current sense on the secondary side of the PCM.</td>
<td>PCA</td>
<td>Boeing</td>
<td>JPL</td>
<td>Honeywell SSEC</td>
<td>Mixed HX2040</td>
<td>&lt;10K</td>
<td>60</td>
<td>Completed fabrication of the first pass on 12/15/00. The part is fully functional with the exception of a POR timing issue. Part deleted from PCA design</td>
</tr>
<tr>
<td>5 AIA (Analog Interface ASIC)</td>
<td>Provides the system I2C bus interface and chops the signal across transformers for isolated interface with the CIA.</td>
<td>PSS PCS JPL + SSEC</td>
<td>JPL</td>
<td>Honeywell SSEC</td>
<td>Custom HX2040</td>
<td>~20K</td>
<td>33 Sig 20 Grd</td>
<td>CDR held January 2002.</td>
<td></td>
</tr>
<tr>
<td>6 CIA (Command Interface ASIC)</td>
<td>Provides local command and control for the PCS and PSS including A/D conversion.</td>
<td>PSS PCS JPL + SSEC</td>
<td>JPL</td>
<td>Honeywell SSEC</td>
<td>Mixed HX2300</td>
<td>~87K gates + 1Kb RAM + 64Kb ROM</td>
<td>184 Sig 50 Grd</td>
<td>CDR on 8/15/02.</td>
<td></td>
</tr>
</tbody>
</table>

**NOTES:**
- All ASICs 1 Mrad unless otherwise noted.
- ASICs to be fabricated via the JPL Multifab Contract.
**Command & Data Handling ASIC Status**

<table>
<thead>
<tr>
<th>#</th>
<th>ASIC</th>
<th>Slice</th>
<th>PDR</th>
<th>CDR</th>
<th>Mask Release</th>
<th>PODs</th>
<th>EMs</th>
<th>FMs</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>1a</td>
<td>Power PCI Bridge Chip RIT A</td>
<td>SFC</td>
<td>✗</td>
<td>✗</td>
<td>✗</td>
<td>✗</td>
<td>✗</td>
<td></td>
<td>RIT A is not planned to be used for flight</td>
</tr>
<tr>
<td>1b</td>
<td>Power PCI Bridge Chip RIT B</td>
<td>SFC</td>
<td>-</td>
<td>-</td>
<td>✗</td>
<td>✗</td>
<td>△</td>
<td>△</td>
<td></td>
</tr>
<tr>
<td>1c</td>
<td>Power PCI Bridge Chip</td>
<td>SFC</td>
<td></td>
<td></td>
<td>12/16/02</td>
<td>4/17/03</td>
<td>5/1/03</td>
<td>7/15/03</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Enhanced Version</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>RAD750</td>
<td>SFC</td>
<td>✗</td>
<td>✗</td>
<td>✗</td>
<td>✗</td>
<td>✗</td>
<td>△</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>DIO (Digital I/O)</td>
<td>SIO</td>
<td>-</td>
<td>5/3/02</td>
<td>5/24/02</td>
<td>9/23/02</td>
<td>11/26/02</td>
<td>8/15/03</td>
<td>PODs and EM delayed, not critical path</td>
</tr>
<tr>
<td>4</td>
<td>MSIO (Mixed Signal I/O)</td>
<td>SIO</td>
<td>✗</td>
<td>✗</td>
<td></td>
<td></td>
<td></td>
<td>△</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>SIA (System Interface ASIC)</td>
<td>SIA</td>
<td></td>
<td></td>
<td>11/27/02</td>
<td>12/17/02</td>
<td>7/8/03</td>
<td>9/4/03</td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>Memory Controller ASIC</td>
<td>NVM</td>
<td>✗</td>
<td>✗</td>
<td>✗</td>
<td>✗</td>
<td>✗</td>
<td></td>
<td>Flight ASICS delayed at foundry</td>
</tr>
<tr>
<td>7a</td>
<td>TRIO - Rev. A (Temperature</td>
<td>TAS</td>
<td>✗</td>
<td>✗</td>
<td>✗</td>
<td>✗</td>
<td></td>
<td></td>
<td>Rev. A is not planned to be used for flight</td>
</tr>
<tr>
<td></td>
<td>Remote I/O)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>7b</td>
<td>TRIO - Rev. B (Temperature</td>
<td>TAS</td>
<td>-</td>
<td>-</td>
<td></td>
<td>N/A</td>
<td></td>
<td></td>
<td>ASIC fab complete, delays in packaging</td>
</tr>
<tr>
<td></td>
<td>Remote I/O)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Definitions:**
- Mask Release: start of fabrication at the foundry
- PODs: Proof-of-Design parts
- EMs: Engineering Model Parts
- FMs: Flight Parts
- SFC: System Flight Computer
- SIO: System I/O
- NVM: Non-Volatile Memory
- TAS: TRIO Assembly Slice
- SIA: System I/F Assembly
- △: Completed this Quarter

2/13/02
## Power System ASIC Status

<table>
<thead>
<tr>
<th>#</th>
<th>ASIC</th>
<th>Slice</th>
<th>PDR</th>
<th>CDR</th>
<th>Mask Release</th>
<th>PODs</th>
<th>EMs</th>
<th>FMs</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>SCAH (Switch Control ASIC High)</td>
<td>PSS PCS</td>
<td>○</td>
<td>○</td>
<td>11/20/02</td>
<td>6/2/03</td>
<td>11/15/04</td>
<td>12/28/04</td>
<td>EM and FM dates extended due to PASM fab</td>
</tr>
<tr>
<td>2</td>
<td>SCAL (Switch Control ASIC Low)</td>
<td>PSS PCS</td>
<td>○</td>
<td>○</td>
<td>11/20/02</td>
<td>6/2/03</td>
<td>11/15/04</td>
<td>12/28/04</td>
<td>EM and FM dates extended due to PASM fab</td>
</tr>
<tr>
<td>3</td>
<td>PWMA (Pulse-Width Modulator ASIC)</td>
<td>PCA</td>
<td>○</td>
<td></td>
<td>11/20/02</td>
<td></td>
<td></td>
<td></td>
<td>First pass completed Deleted from PCA design</td>
</tr>
<tr>
<td>4</td>
<td>SRCA (Synchronous Rectifier ASIC)</td>
<td>PCA</td>
<td>○</td>
<td></td>
<td>11/20/02</td>
<td></td>
<td></td>
<td></td>
<td>First pass completed Deleted from PCA design</td>
</tr>
<tr>
<td>5</td>
<td>AIA (Analog Interface ASIC)</td>
<td>PSS PCS</td>
<td>○</td>
<td></td>
<td>11/20/02</td>
<td>6/13/03</td>
<td>2/15/05</td>
<td>10/3/05</td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>CIA (Command Interface ASIC)</td>
<td>PSS PCS</td>
<td>○</td>
<td>8/15/02</td>
<td>12/1/03</td>
<td>5/27/04</td>
<td>2/15/05</td>
<td>10/3/05</td>
<td></td>
</tr>
</tbody>
</table>

### DEFINITIONS:
- **Mask Release**: start of fabrication at the foundry
- **PODs**: Proof-of-Design parts
- **EMS**: Engineering Model Parts
- **FMs**: Flight Parts
- **PSS**: Power Switch Slice
- **PCS**: Power Control Slice
- **PCA**: Power Converter Assembly

△ Completed this month

2/13/02