

X2000 Power System Electronics Development

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Abstract—The Europa Orbiter mission, currently baselined for launch in March 2008, is intended to follow up on tantalizing results from the *Galileo* spacecraft, data from which suggests that there may be a global ocean underneath the jovian satellite Europa's water ice crust. If Europa has an ocean, its volume is likely to be greater than that of all Earth's oceans combined, even though Europa itself is only about the size of Earth's Moon. Scientific objectives for the mission are to ascertain whether or not Europa has a liquid water ocean, to characterize ice layers beneath the surface, and to find the most scientifically enticing landing sites for future missions.

Europa orbits in the heart of the jovian magnetosphere's trapped radiation belts, resulting in radiation doses many times those for which civilian spacecraft have been designed in the past. Total dose is projected to be 6-7 MRad [Si] behind 40 mils aluminum in the case of Europa Orbiter. In addition, Europa orbit is propulsively one of the most difficult destinations to reach in the Solar System, making mass a major driver of mission cost. The combination of high radiation and the need for low-mass and -power electronics led to the X2000 avionics development activity, which is now at the core of the Europa Orbiter project. Because X2000 equipment has been designed for scalability and modularity, other missions have adopted the flight computer, memory, and potentially other "slices" of X2000 hardware and accompanying software. At the heart of the X2000 development are 14 rad-hard, high performance ASICs, which may be utilized either on the avionics "slices" for which they are being designed, or separately if that is beneficial to a user.

The Europa mission provides a challenge in terms of extreme environmental requirements. The key driving requirements are the one mega-rad total ionizing dose and the fourteen-year life.

The X2000 Power System Electronics (PSE) must reduce its power, mass and volume envelope by incorporating new technology developed by industry partners. The combination of Multi-chip module (MCM) packaging, rad-hard mixed signal application-specific integrated circuits (ASICs) and next-generation-power devices increases the packaging density of the Power System Electronics.

The X2000 PSE has successfully completed a preliminary design review clarifying the requirements. Currently, there

are two ASICs that completed fabrication and two others in fabrication. We have de-scoped one technology due to cost and schedule risk.

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1. INTRODUCTION

Europa Orbiter Project

The **Europa Orbiter Project** is managed by JPL for NASA takes the prime initiative to deliver an orbiter to the Jupiter moon Europa. The Europa Project now manages the X2000 development, formerly managed by the Integrated First Delivery Project under the Deep Space System Technology Program.

The X2000 Avionics primary focus is on the delivery of a flight avionics package for the Europa Orbiter. The package will include a new and innovative distributed architecture in both hardware and software. The architecture must be capable of integrating different instruments, propulsion modules, power sources and telecommunication into a multiple mission platform.

The key requirements for EO are as follows:

- 1 Mega-Rad Total Ionizing Dose
- 14 year life
- Low Mass and Power

With all of the challenges in the Europa mission, a combination of new technology and innovative architecture is needed.

2. DEVELOPMENT APPROACH

The Power System Electronics (PSE) approach to meeting the needs of the customer is to combine a new architecture with the development of new technology. Program funding makes the overall cost a key driver in the development.

Based on JPL's experience in developing the Cassini power system, a combination of radiation hardened ASICs and

high density packaging can be implemented to increase the overall functionality, reduce mass and lower both development and recurring cost.

The Cassini Power System used the Solid State Power Switch (SSPS) which combined a radiation-hard digital ASIC with discrete analog and power components in a class K hybrid package). CTS Microelectronics produced the SSPS under contract from JPL.

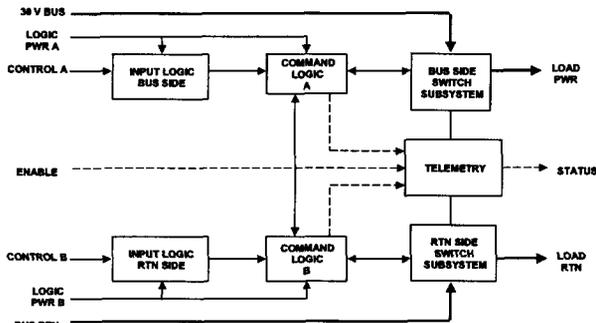


Figure 1 Cassini SSPS

The Cassini SSPS Hybrid contained the following components:

- 2 United Technologies Microelectronics Center gate arrays
- 35 active devices (IC dice)
- 26 chip resistors and capacitors
- 181 screened resistors
- 12 actively trimmed resistors
- 466 bond wires (396 are 1 mil gold)
- 72 pin package

Cassini also utilized a Honeywell (HR1060) one-mega-rad-hard gate array for the power distribution command interface. The power distribution contained a custom serial data bus on every board. The main command interface from the spacecraft was through a Remote Engineering Unit (REU) providing a 1553 data bus to the spacecraft and a parallel interface to the power subsystem.

Each development paid off for Cassini because the components were used on every power distribution board. The use of these custom components on every board reduced the number of piece parts and assembly time of each board. Cassini was able to provide more functionality in a smaller package by investing in Hybrids and gate arrays.

In a similar approach, the X2000 PSE will go one step beyond Cassini and implement mixed signal ASICs and MCMs.

Cassini was successful in using existing technology to provide modules; however, with today's technology there is room for improvement.

Other improvements over Cassini can be achieved by the use of a mixed signal ASIC technology. By selecting a technology that is compatible with the Command and Data Handling (C&DH) ASICs, the power system can use the same Intellectual Property (IP) for C&DH in the mixed signal ASICs in the power subsystem. This will provide a standard interface to each of the power system boards that is well supported by the system.

POWER SYSTEM GOALS

The following is a list of goals for the X2000 PSE, which relate directly to the goals of X2000 Program:

- Multiple-mission architecture
- Increased power management
- High end to end system efficiency

To meet the goal of a multiple-mission architecture, the power system electronics must be a modular and scaleable in design with standard interfaces.

The architecture of the power system needs to be partitioned in modules that can be changed depending on the mission requirements. Partitioning the design such that only a single module is affected by either different source, energy storage technology or unique load can reduce the cost of a multiple mission platform.

The power system architecture must utilize this philosophy without sacrificing the capability for design optimization. This requires a combination of MCM packaging with accessible surface mount packaging. With intelligent partitioning of the power system functions, a modular design can evolve with the capability for late changes and minor optimization.

Functions that are common throughout the power system like power switching, pulse width modulation and the command interface, can be incorporated in mixed signal ASICs or MCMs with little concern for future modification. These functions are core building blocks for the power system.

Another goal of the power system is to provide more power management capability enabling missions with very low power source capability. Power is a limited resource particularly for outer planet missions where generating power becomes more elusive.

More system observability and controllability in the form of telemetry and power switching enables the system to improve the management capability. By increasing the number of power switches and telemetry channels, the system has more options for accomplishing the mission requirements within the allocated power.

Improving the overall end-to-end system efficiency is always a goal for the power system. Many different types

of power converters in a system provide more risk in the system development when it comes to overall efficiency and system stability. Typically the different types of converters are under utilized and thus operate at the lower end of the efficiency curve.

A power converter development that meets the system-input-impedance, conducted-emissions requirements and provides a high efficiency over a wide load range reduces the risk and improves efficiency. A generic converter offering the most common output voltages is being developed using the latest technology. This converter allows users to take advantage of the latest technology while minimizing risk.

The users would have to use a generic capability power converter, but the payoff to system could be great. The power system deals with many of the same converters known to meet the input impedance and conducted emissions requirements. The key for this to be effective is that the converter needs a high efficiency over a wide load range and must come in a small package to make it attractive to the end user.

To be successful, X2000 will have to focus the NRE on a select few functional building blocks. The architecture needs to leverage building block approach and reduce the number of point designs to reduce the overall cost of the program.

X2000 PSE Objectives

The primary objectives for the X2000 PSE are as follows:

- Develop a one mega rad hard analog cell library
- Produce several mixed signal ASICs
- Fabricate a select number of power MCMs
- Deliver Compact PCI 3U Boards
- Deliver an integrated PSE subsystem

It is clear from the objectives that delivering a power subsystem are not enough. X2000 charter is to pave the way for future developments over several deliveries. The objectives reflect more than hardware delivery, rather a methodology for follow-on deliveries to use.

The development of a one-mega-rad-hard analog cell library provides a consistent path for future deliveries to use as a tool in developing ASICs. A good library can be used for the specification of different ASICs that are independent of the ASIC-fabrication foundry. The library can be maintained separately and targeted to different foundries as technology improves. This allows for the new foundries to be qualified with the library before the first specific ASIC design needs to be fabricated. Specific ASIC design can be passed from one delivery to the next with only a higher-level chip layout and simulation required.

The development of mixed signal ASICs for applications

repeated throughout the subsystem can provide consistency in performance over the environmental requirements. The performance of these functions can be proven and repeated reducing the number of piece parts in the system and lowering the risk in system integration. These ASICs are designed using the same analog cells and also share larger macro cells. The ASICs make it possible to meet the X2000 environmental requirements.

Just as the mixed signal ASICs are used, high density MCMs can be used to provide functional building blocks for the power subsystem. The MCM packaging approach enables the close packaging between the discrete power components and the ASICs. The power MCMs will provide the complex power circuits in a dense modular package. Most of the difficult design, layout, and analyses will be completed at the MCM level thus reducing the complexity on the circuit board.

The finished product will be power subsystem circuit boards that can be configured into a mission specific power system. The purpose of the circuit boards is to bridge the gap between the power electronics building blocks and the mission specific subsystem. By investing NRE in the MCMs, the circuit boards can be easily modified with little NRE to match the packaging concept of any mission. The circuit boards are a higher level building block that can be configured to meet the mission needs.

All of the objectives are determining deliveries to the X2000 program. These objectives are in place to build a foundation for power system development with the long-term goal of placing a system on a chip.

3. KEY TECHNOLOGY

Technology development has been very limited for many projects. The high non-recurring engineering (NRE) costs and schedule needed for technology development limit what many projects achieve. Additionally, the associated risk prevents many project managers from investing in new technology.

Fortunately, with the formation of CISM for technology development and the New Millennium Program (NMP) for flight validation, new projects can benefit with reduced risk while industry can demonstrate promising new technology.

The goal of CISM and the NMP Microelectronics Integrated Product Development Team (IPDT) is to develop and validate promising new technologies, modular building block designs, and standard interfaces. The IPDT has a number of members from industry, universities, laboratories and NASA with a common goal of producing a road map of technology needed for the next generation of spacecraft

JPL is partnering with key industry leaders to focus the technology development and provide an application for its use. The industry partners are Boeing's Solid State Electronics Development organization (SSED and Lockheed Martin Communications and Power Center (LM-CPC). This partnership has worked well in developing the Power Actuation and Switching Module (PASM: see figure2) for the Deep Space One (DS1) mission in the New Millennium Program.

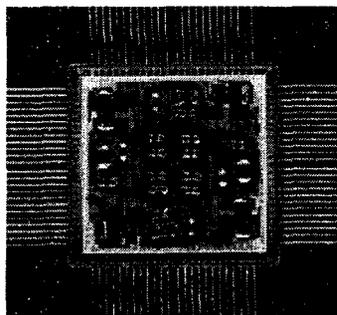


Figure 2 DS1 PASM

The PASM experiment has flight-validated two technologies for the power system electronics. The technologies are the high voltage mixed signal ASIC and Power High-Density Interconnect (PHDI) packaging.

The PASM has four power switches that are current controlled for soft start current limiting and tripping functions. It provides the same functionality as the SSPS in a much smaller package. The PHDI switch module was design by LM-CPC utilizing a General Electric (GE) technology. The PHDI packaging technology combines the mixed signal ASIC, power MOSFET and discrete components of four switches in a single package. The PHDI packaging technology enables high-density packaging for power applications.

Boeing designed the Switch Control ASIC (SCA) that provides the control functions for the power switch. The SCA was fabricated on the Harris Radiation Hardened SiGate (RSG) process. The SCA combined the functionality of the SSPS gate array and discrete analog components into a single component.

Other technologies were also used in the X2000 program. Boeing designed the Power Management ASIC and Advanced Instrument Controller for the NMP Deep Space 2 probe. LM-CPC developed the all PHDI Electronic Power Converter (see picture below).

All of these technologies were leveraged in some way in the X2000 PSE development.

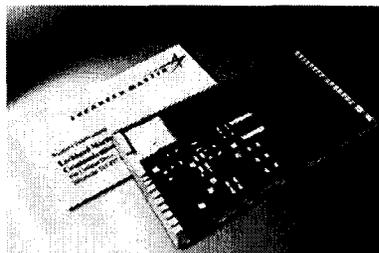


Figure 3 LM-CPC EPC

4. POWER SYSTEM ARCHITECTURE

The X2000 Power System Electronics (PSE) architecture (figure 3) is conceived to meet the goals of X2000. It is scalable and expandable for different mission power levels and redundancy requirements. It provides a high level of insight into the status of the power system and individual loads, and it uses the highest efficiency components available.

The X2000 IFDP power system is a direct energy transfer system with a battery-dominated bus. Alternate architectures can be achieved with the addition of a few more building blocks. These additional building blocks are not within the scope of the IFDP. The PSE slices can be used in alternate architectures if desired by the missions.

The power system architecture consists of unique functional slices which can be optimized for a specific power source, energy storage technology or load requirement. These slices are connected together via the power bus and the I2C data bus. Each slice has the same power and data interface.

The standard interface allows for missions to add slices as needed based on the power level and number of loads. The back plane configures the slices.

The packaging approach for the PSE is to use the Compact-PCI standard 3U card cage. All of the PSE slices will be double-sided 3U cards with average mass of 500g.

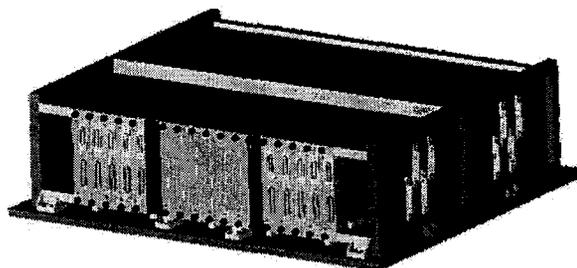


Figure 5 PSE Chassis

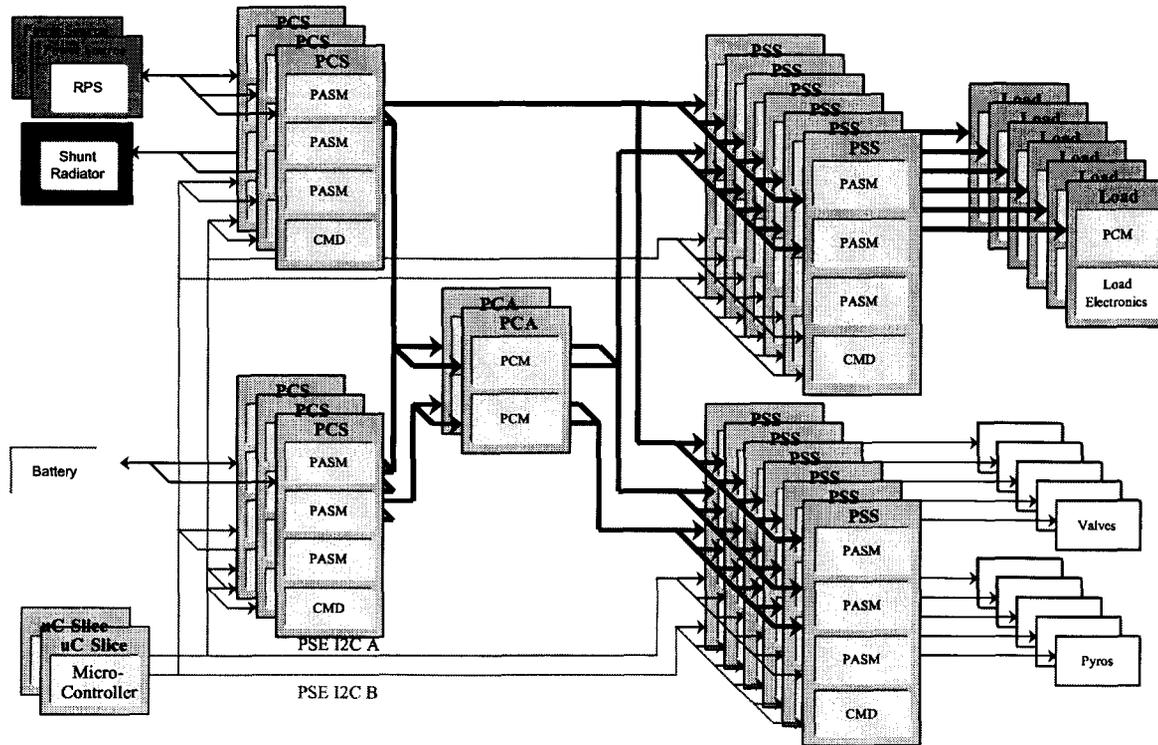


Figure 4 PSE Block Diagram

The cards will plug into a back plane that can be used to distribute the power bus and set the configuration of the circuit boards.

There are three types of slices:

- Power Control Slice (PCS)
- Power Converter Assembly (PCA)
- Power Switch Slice (PSS)

The following MCMs are used as the power electronic building blocks

- Power Actuation and Switching Module (PASM)
- Power Converter Module (PCM)

Each MCM contains mixed signal ASICs and discrete power components. Another functional building block is the command interface ASIC (CIA). The CIA is a mixed signal ASIC with some discrete component on the circuit board.

The following paragraphs are brief descriptions of the functionality of each slice. For a detailed description of each slice, refer to the Product Description Section.

Power Control Slice (PCS)

The PCS provides the main interface with the power source. The primary function is to regulate the power bus voltage and or battery charge current. It achieves regulation by digitally switching bus shunt loads to control the bus

voltage or battery current. The PCS will have programmable set points for both bus voltage and battery charge current. Power Control also provides all of the fault protection and telemetry for the power bus and battery. Single fault tolerance is obtained by majority voting three slices to provide that control function. The CIA provides the command and telemetry interface and control algorithms. The PASM provides the power switching.

The PCS, configured differently, also provides the main interface to the battery. The main function is to provide a battery cell bypass to prevent overcharging of the cell. The bypass cell voltage set point is programmable. Once again, single-fault tolerance is obtained by voting three slices. The CIA provides the command and telemetry interface and control algorithms, and the PASM provides the power switching.

Power Switch Slice (PSS)

The PSS provides the interface to all of the loads on the spacecraft. Each power switch can be commanded to drive a steady state or momentary/pulse load. Each switch can be configured in the high or low side, and series or parallel. No single failure shall cause more than one switch to be stuck ON. Telemetry is provided for each load. Every switch in the PASM provides controlled turn on and protects the power bus from load faults. The CIA provides

the command and telemetry interface. The PASM provides the power switching.

The PSS provides the power and command interface to the valves on the spacecraft. The CIA can synchronize and provide accurate timed commands. The same protection and telemetry is also provided per valve interface.

The PSS provides the interface to the pyro devices. The PSS provides an interface for safety inhibits, and has separate enable commands for groups of switches. Each switch provides current limiting to allow for simultaneous multiple events.

Power Converter Assembly (PCA)

The Power Converter Assembly (PCA) provides the housekeeping power for the power system. Each slice requires a redundant 3.3V and 5.0V housekeeping power. The 3.3V is for the digital logic, and the 5.0V is for the analog control functions. Power-cross-strapping is done internally on each slice. The PCA just contains one 3.3V PCM and one 5.0 PCM.

Each power system slice has the same standard I2C data bus interface which enables the spacecraft computer direct access to each module. This results in test and integration costs decrease due to having an industry standard interface combined with increased visibility into each module during system level testing.

The purpose of this architecture is to give the missions more flexibility to configure a power system that meets their requirements. The architecture provides all of the hooks needed for a robust configuration. The ultimate reliability of the subsystem depends greatly on the configuration of the slices. The architecture provides many options for redundancy and can be scaled based on the mission requirements. The Power System Electronics can be configured as a single string or 1 through N redundancy.

5. PRODUCT DESCRIPTION

The following subsections will elaborate in more detail on description in the previous section of the X2000 PSE products.

Rad-hard Analog Cell Library

Much of the PSE is based on the functionality provided in the analog ASIC cell library. The purpose of the library is to allow qualification of the cells to occur prior to the development of the ASIC.

The semiconductor process selected for the library is the Honeywell RiCMOS IV process. Honeywell has shown that they can achieve one mega-rad hard performance on this line. Other advantages to the line are that it is a proven digital process with a large library of digital cells and Intellectual Property.

Boeing is the industry partner who is developing this library. Many of the cells have been fabricated and tested verifying the post radiation models.

The complexity of the cells ranges from simple operational amplifiers and comparators to more complex macro cells such as an auto-zero amplifier or pulse width modulator. These cells make up the lowest level of building blocks for PSE.

Boeing has provided an innovative high voltage transistor on this low voltage process [1]. This development has been a key to enabling power control functions to be done on a low voltage mixed signal process. Altering the layout to increase the breakdown voltage and protecting the gate from the drain have increased the breakdown voltage. We are able to switch up to 30 volts with the N channel and 15 volts with the P channel.

Rad-hard Mixed Signal ASICs

The following rad-hard mixed signal ASICs are being developed:

- Pulse Width Modulator ASIC (PWMA)
- Synchronous Rectifier Controller ASIC (SRCA)
- Switch Control ASIC (SCA)
- Command Interface ASIC (CIA)

Each ASIC is based on the analog cell library and digital macro cells provided by C&DH.

The PWMA and SRCA are used in the power converter module. The PWMA is on the primary side of the isolated converter and provides the pulse width modulation and synchronous rectification driver functions. The SRCA is on the secondary side of the converter and provides the synchronous rectifier drivers.

The SCA is the most used part in the PSE with an estimated quantity of over one thousand for Europa. This is a perfect example of how an ASIC can be economical. The SCA provides all of the control functions for each switch in the PASM. The SCA provides the level shifting and charge pump for high side power switching.

The CIA provides the system interface for all of the boards.

The CIA is comprised of an integrated 8051 core, memory, ADC and a Philips I2C data bus interface. The CIA provides a single chip solution to the command interface that was handled by the REU on Cassini.

Power Converter Module (PCM)

The X2000 PCM design is a DC/DC converter that operates at high frequency (1Mhz) providing high efficiency and small volume (2.3" X 3.0" X 0.4").

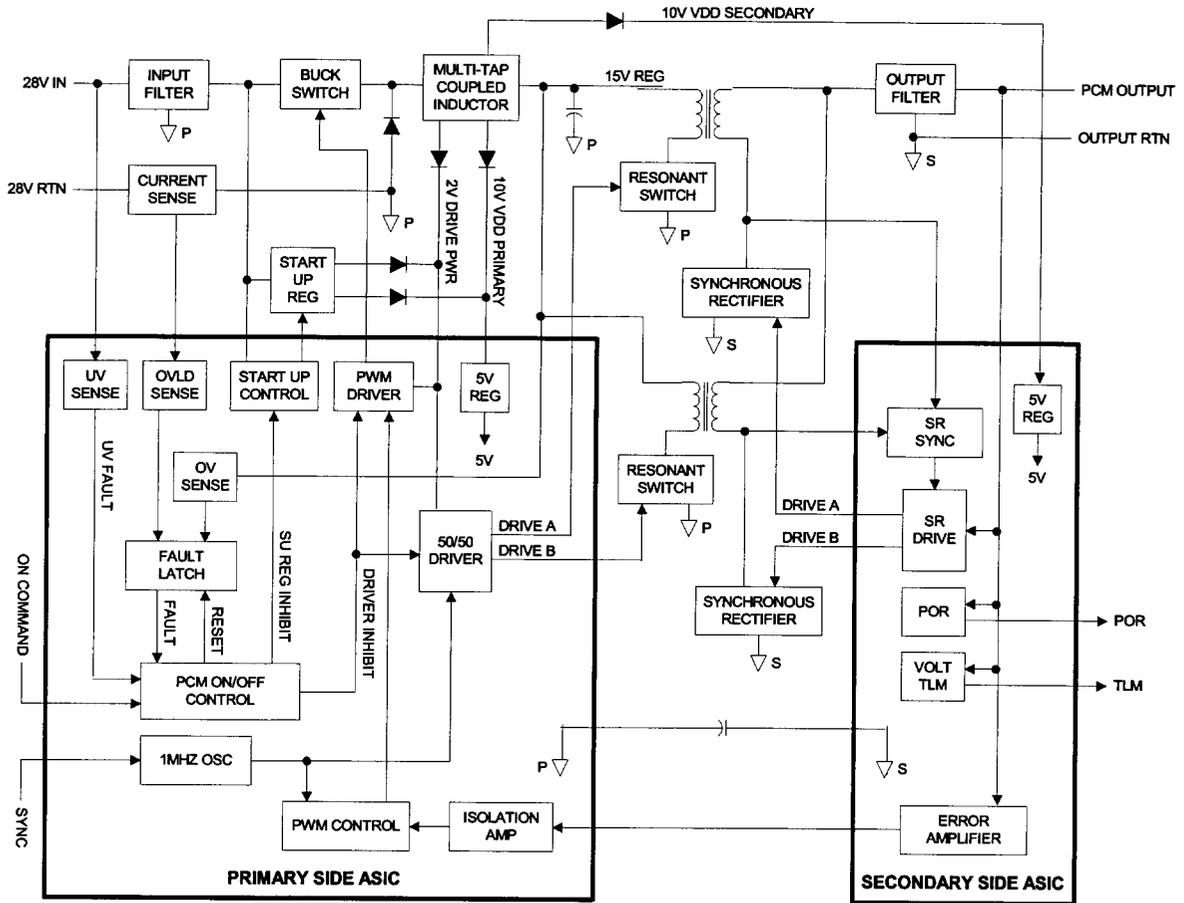


Figure 6 PCM Block Diagram

The PCM provides an output of either 3.3V or 5.0V at a power level of 30 watts. The input bus voltage is specified from 22 to 36 VDC. The converter provides output over-voltage and load short-circuit protection by latching off the converter.

The converter is designed to meet conducted and radiated susceptibility EMC requirements, including input power line transients. Isolation requirements are one meg at +/- 30 VDC, primary to secondary.

The topology is a dual resonant forward converter operated at a fixed switching frequency. Output voltage regulation is achieved by pre-regulating the dual-forward-converter primary voltage with a hard switched, Pulse Width Modulated, Buck Converter. The Resonant Forward Converter stages provide high efficiency by virtue of their zero voltage switching characteristics. The converters operate at 180 degrees out of phase to minimize input and output filtering. Output rectification losses in the high current low output voltage designs, are reduced by utilizing synchronous rectifiers. The resonant forward converter section is easily optimized because the input voltage is pre regulated. Thus, other output voltages can be easily

obtained by adjusting the main transformer turns ratio.

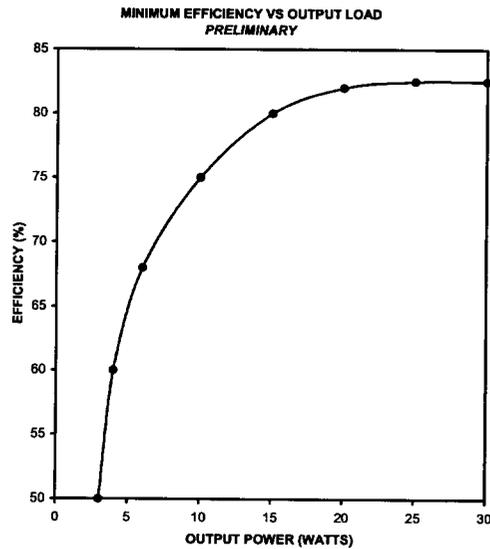


Figure 7 PCM Efficiency Curve

Efficiency is maximized by the use of Complementary Hetero-junction Field Effect Transistors (CHFET), developed by GE and Honeywell. The CHFET has the advantages of having low input capacitance and a low input drive voltage. Both of these parameters reduce the power necessary to switch at the 1 Mhz switching frequency. In addition, the CHFET structure does not contain a parasitic Source/ Drain body diode, which makes them ideal for a synchronous rectifier. There is no danger of a body diode conducting avoiding reverse recovery issues.

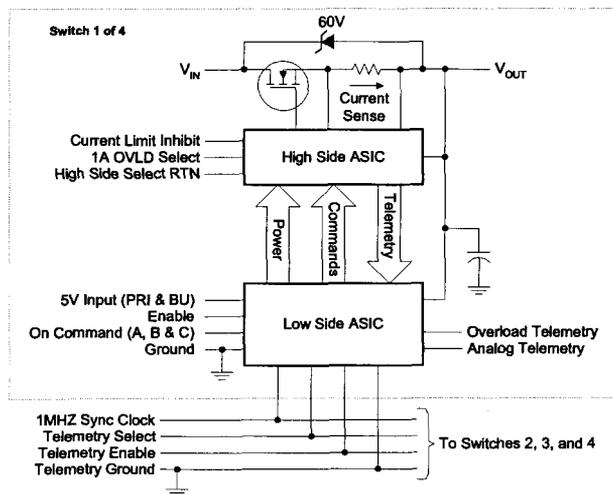


Figure 8 PASM Block Diagram

Power Actuation and Switching Module (PASM)

The second generation PASM is very similar to the DS1 version. It provides basically the same functionality but with a 1 mega-rad-hard rating. The PASM contains two independent solid state power switches in a single package. The following is a list of switch parameters for the PASM.

Overload Trip Current	1 A., 3 A (selectable)
Overload Trip Delay	20 ms
Current Limit	2 A, 5 A (selectable)
di/dt	180 A/S
Voltage Telemetry	0.075 V/V
Current Telemetry	1 V/A
On resistance	60 mOhms
Input Voltage Range	0 – 40 V

Some changes have been made to make it more compatible with the X2000 products. The SCA is on the Honeywell RiCMOS IV, therefore the PASM is now one-mega-rad hard. Another change is that the package has changed to fit three PASM's on a side within a Compact PCI 3U card.

Power Control Slice (PCS)

The PCS is configured as a set of generic power switches (PASM) driven by an 8051 micro-controller (CIA). In this way, the PCS can be used for a variety of functions under

the direction of local software. A functional block diagram of this concept is shown below.

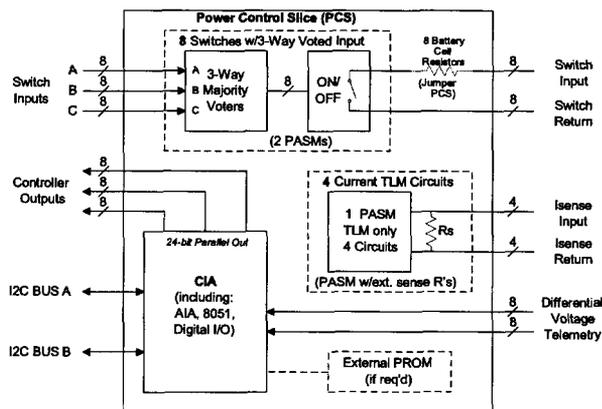


Figure 9 Power Control Slice Functional Block Diagram

The approach of using the CIA and the PASM for power control functions reduces overall NRE by avoiding specialized control ASICs. This is a case where functional building blocks can be used in other applications even when not optimized for it. The PCS provides the Power Control function.

The fundamental Power Control software and default states/values will be contained in non-volatile memory. Software parameters, or advanced management algorithms can be loaded into RAM. Due to a limited amount of ROM available within the CIA, it may be necessary to include external ROM on the PCS slice.

The power control function will use the PCS to switch in digital shunts to control the bus voltage and/or battery charge current.

The PCS monitors bus voltage and battery-charge current telemetry and compares them against a command value. PCS Shunt switches are sequentially turned ON to divert RTG output current to ground, thus reducing the current onto the battery bus (and hence the bus voltage). PCS Shunt switches are sequentially turned OFF to increase the RTG current onto the battery bus. The PCS control loop acts to balance the amount of RTG current available to the battery bus with the spacecraft load demand-plus-the desired battery charge current.

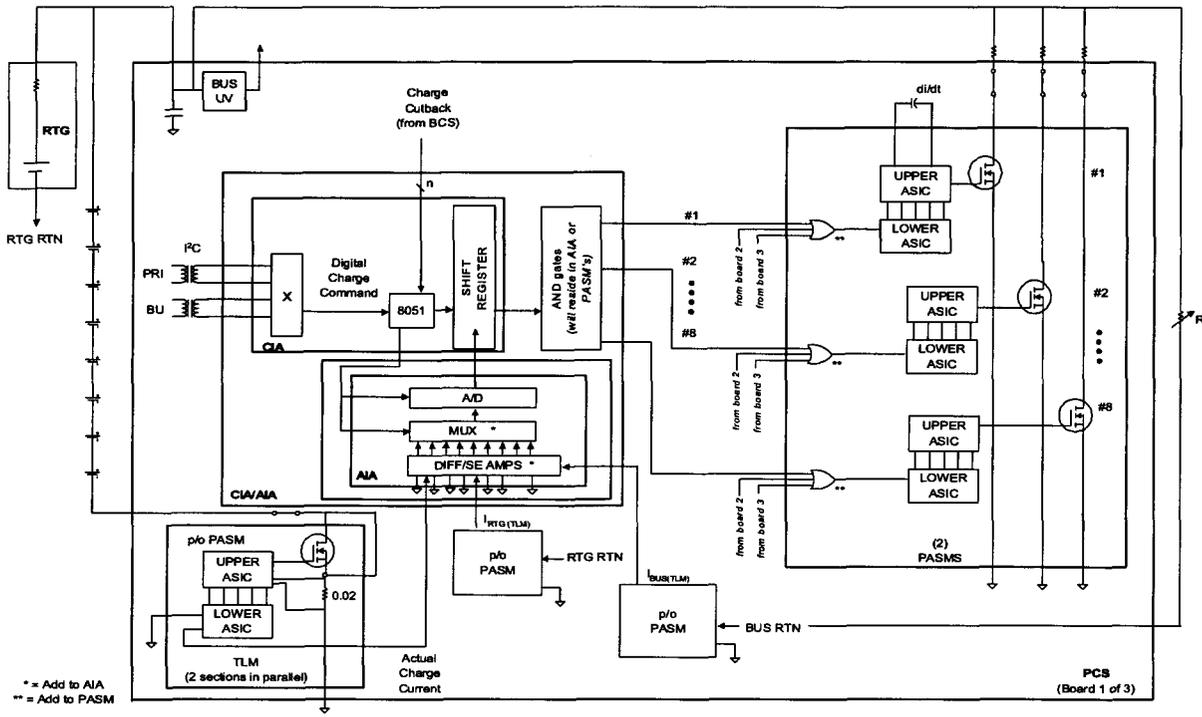


Figure 10 PCS Block Diagram

If the spacecraft load plus battery charge requirement equals the total RTG power all PCS shunts will turn OFF. If the spacecraft load plus battery charge requirement exceeds the total RTG power the battery charge current will naturally cut back toward zero. If the spacecraft load current, alone, exceeds the total RTG power; the battery will be discharged to supply the deficit. At this point, the battery/bus voltage will drop according to the battery voltage vs. state of charge (SOC) characteristic. Bus under-voltage protection prevents discharge of the battery below a set minimum voltage by sensing the under-voltage condition and sending a signal to predetermined load switches (PASMs) to remove non-critical busloads

the spacecraft load plus battery charge requirement exceeds the total RTG power the battery charge current will naturally cut back toward zero. If the spacecraft load current, alone, exceeds the total RTG power, the battery will be discharged to supply the deficit. At this point, the battery/bus voltage will drop according to the battery voltage vs. state of charge (SOC) characteristic. Bus under-voltage protection prevents discharge of the battery below a set minimum voltage by sensing the under-voltage condition and sending a signal to predetermined load switches (PASMs) to remove non-critical busloads.

Power Switch Slice

Just as the PCS is used for multiple applications the PSS is used for switching power loads, valves and pyro devices. Each application has some unique requirements; but in general, they all require power switching. The PSS is comprised of the CIA and four PASMs.

Power Distribution Function

The Power Distribution Function uses the PSS to provide load switching, telemetry, and fault protection. The number of slices will depend on the number of loads and total power of the spacecraft.

The command interface is via the standard interface to the spacecraft data bus. The I2C data bus is isolated between the physical and link layers.

Number of shunt load switches	24 total	24 for 23 redundancy
Total Shunt Power	300W	Equivalent to Maximum RTG source power
Power per Shunt switch	13W	300W / 23 switches
Battery Charge Current	Maximum: 1C (6A) Nominal: C/3 (2A) Minimum: 0 Increment: < C/50 (0.12A)	Battery Driven requirement TBC

If the spacecraft load plus battery charge requirement equals the total RTG power all PCS shunts will turn OFF. If

The PSS provides the capability to individually command sixteen switches on the board. Switches assigned to loads can be classified as loadshed or non-loadshed. The switches can be commanded in steady state mode or pulse mode. The steady state command turns the load on or off indefinitely. The pulse mode turns ON the switch for a specified duration after a specified delay. Pulse loads can be continued indefinitely with repeated commands.

The switch fault protection is composed of a current limit function and a selectable trip level. With current limit, other loads on the same power converter are not affected during the isolation of the fault.

Load current telemetry is available for each switch. The analog load current telemetry can be converted to digital telemetry by the command interface. Since telemetry is available on every switch, the power converter efficiencies can be calculated in flight as well as the identification of load variations, drifts and incipient failures.

The PASM can be used in different configurations. Switches can be connected in parallel to reduce the voltage drop for high current loads. It is configurable in series/parallel or bi-directional connection to the load. Additionally, these switches can be configured in various ways to meet critical load requirements or to provide needed cross strapping between loads.

Valve Drive Electronics Function

The PSS is used for the Valve Drive Electronics Function, providing the same functionality as in the power distribution function. Timing is more critical thus the pulse mode is used for all of the valves.

The PSS provides four cross-strapped outputs to allow a lower valve holding voltage. The lower voltage can be switched from either a central converter or a tap off the battery.

It takes two power switches per valve to hold it in position. One switch is connected directly to the battery to provide the actuation energy. The second switch is connected through a diode to provide the lower voltage holding power.

Pyro Drive Electronics Function

The PSS is used for the Pyro Drive Electronics Function, providing the same functionality as in the power distribution function. For pyro devices, safety is more critical thus the enable command and safety inhibit interface is available to provide the additional layers of protection.

The pulse mode is used for all of the pyro commands. The PASM will provide current limiting to ensure load sharing while simultaneous events are occurring.

6. EXPECTED RESULTS

It is very difficult to compare one generation of power electronics to another. It is difficult to compare "apples and apples", because the functionality is rarely the same. Cassini is the closest power system electronics to compare with the X2000 PSE because of the similar functionality.

Cassini used some gate arrays and hybrids while X2000 is using all mixed signal ASICs and MCMs. The X2000 PSE hardware is configured to perform the functional equivalent of Cassini, ignoring the additional functionality that comes with the new hardware. The following is a table of parameters to compare.

It is clear that the investment in mixed signal ASICs and MCMs has paid off in an almost two-to-one improvement in mass and volume. However, the impact of maintaining modularity is indicated in the housekeeping power. Each slice requires more power as compared to Cassini.

Using X2000 PSE hardware for a spacecraft as large as Cassini is not an efficient application because of the large number of boards. There is much less packaging efficiency when 38 boards are used vs. 15. As an example, using the same Cassini board size and the X2000 ASICs and MCMs, the functionality could be achieved in only 5 boards rather than 15.

The X2000 PSE is targeted towards much smaller spacecraft than Cassini; however, it is the closest in functionality for the purpose of a benchmark.

Table 2 Cassini Comparison

PARAMETER	EXPLANATION/ CLARIFICATION	Cassini	X2000 PSE
Recurring Cost		\$3,420 K	\$3,522 K
Mass (kg)	Total Core for Power Distribution	54.97 Kg	29.0 Kg
Power Control Capability		900W	900W
Minimum Housekeeping Power	All switches OFF	4.80 W	7.60 W
Maximum House Keeping Power	All switches ON	11.52 W	38.00 W
Complexity		Medium	High
Development Risk		Medium	High
Operability/Flexibility	Building blocks need to be useful for all missions, not just 1	Medium	High
Scaleability		High	High
Grounding/Isolation	Which implementation gives the optimum grounding	Good	Good
Fault containment		Small	medium
Volume		63,962 cc	35,775 cc
# of Slices		15	38
Shunt Regulator	Requires 3 PCSs	1	6
Capacitor Bank	one board for 1200uF	0	1
Power Control	Included in shunt regulator	1	0
REU		2	0
House Keeping Power	PCA	1	2
PD I/O		2	0
Power Distribution (Switches)	PSS	6	24
Valve Drive Electronics	PSS	0	0
Pyro Drive	PSS	2	5

6. CONCLUSION

The X2000 PSE development is producing many products beyond the flight hardware deliverables. The purpose of the program is to build a foundation and a process, which the follow on deliveries can leverage and enhance. The building blocks can be used in many other applications outside of the power system. Some of the building blocks could be used to provide motor control electronics or just about any power switching application.

The flexibility will ultimately improve the overall efficiency of the power system. By having a flexible design which is modular as well as adaptable, power systems on future spacecraft can save time, cost and mass with a minimum investment of dollars.

The power system electronic modules combine high-density packaging techniques and mixed signal ASICs for a reduction in mass and volume without sacrificing functionality or efficiency.

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Russell E. Haskell began his career in 1980 at RCA Government Communications Systems Division in Camden, NJ. He spent the next 14 years working on a wide variety of Power Supplies, and Power Systems for various Military applications. In 1994, he transferred to the Astrospace Division where he has continued to work on various Power Supplies, and Power Systems. Mr. Haskell has had many lead roles in his 19 year career, and has spent the last 3 years involved with the advanced HDI packaging of Power Electronics. He holds a BSEE from New Jersey Institute of Technology and a MSEE from Drexel University

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