Design of a switch matrix gate/bulk driver controller for thin film lithium microbatteries using Microwave SOI Technology

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***Abstract*—Integrated microbatteries are being currently developed to act as a "micropower" source in microsatellites. The current and voltage rating of the microbattery is fixed. Certain highly miniaturized systems require higher voltages and currents. A switching matrix is designed to achieve the same. The switching matrix is designed using High Voltage Metal Oxide Semiconductor (MOS) structures and H gates.**

This paper presents a design approach to help attain any random grouping pattern between the microbatteries. In this case, the result is an ability to charge microbatteries in parallel and to discharge microbatteries in parallel or pairs of microbatteries in series. This is achieved by providing the appropriate gate/bulk voltages to the matrix. High Voltage MOS structures are developed which can take higher drain-to-source voltages in a 3.3V process. The designs are built using Microwave Silicon- on-Insulator process.

Index Terms – MOSFET, Micropower, Microbattery, and Silicon-on-Insulator.

I. INTRODUCTION

In recent years, NASA has reported great successes in its effort to miniaturize spacecraft components using MEMS technology, integrated passive components and low power electronics as seen in Figure 1. Based on this success, the need has arisen for the design of ultra low power sources for micro satellite applications. Recent work has focused on the integration of the power generation, power storage, and power distribution and regulation functions in a single, highly compact package or module which can be integrated with the microdevices to be powered – a "micropower" source. This miniaturization and integration of power sources with the devices to be powered will enable the concept of distributed sensing for a host of planetary wide-area sampling and exploration missions. By providing point-of-use power, significant reductions in the mass associated with wiring and packaging can be obtained [1]. Similar advantages can be harnessed by colocating micropower sources and integrated circuit components on the same chip.

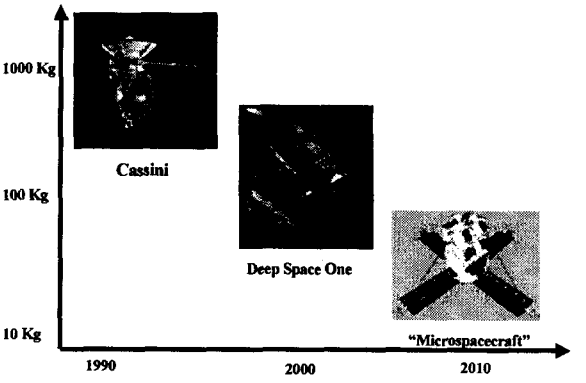

Figure 1 Reduction in spacecraft mass and volume.

Towards achieving this goal, Jet Propulsion Laboratory (JPL) has recently reported the development of micro-scale batteries, fabricated on silicon wafers, with footprints on the order of $(50\text{-}100\mu m)^2$. The capacities of these cells are primarily limited by the thickness and area of the cathodes. These thin film lithium microbatteries have emerged as a legitimate power source in many microspacecraft applications. Conventional bandgap voltage reference circuits can be quite large and are candidates for replacement by these microscale batteries. Analog sensors which require total isolation from digital noise for optimal performance can benefit from these on-chip power sources [2]. But in any microspacecraft, there always exists certain highly miniaturized systems like the microsensors, which require higher capacities and voltages than a single lithium microbattery can provide. Towards solving this problem, an innovative switch array system for thin film microbatteries is developed. This matrix helps provide the maximum voltage or current flexibility desired at the chip level. The switch matrix is designed using High Voltage MOS structures and specially designed H-Gate MOS devices to provide bulk-source isolation in Silicon-on-Insulator process. This paper describes an effort to control this switch matrix using a gate/bulk driver.

II. THIN FILM LITHIUM MICROBATTERY CHARACTERISTICS

The microbatteries used for the project have been designed, fabricated and tested at JPL, California Institute of Technology. The characteristics of the microbatteries are listed in TABLE I. The lithium microbatteries fabricated for this work were nominally 600μm*600μm, and provided between 10-50nAH capacity (Figure 2) [2]. These microbatteries can be cycled hundred of times with minimal capacity loss [2]. In this paper, a standard capacity value (50nAH) microbattery is used as a reference for the entire design.

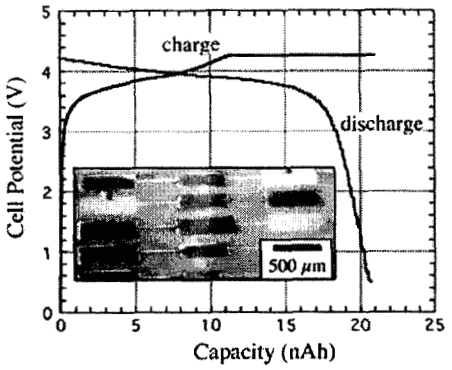

Figure 2 Charge/Discharge profile of lithium microbattery.

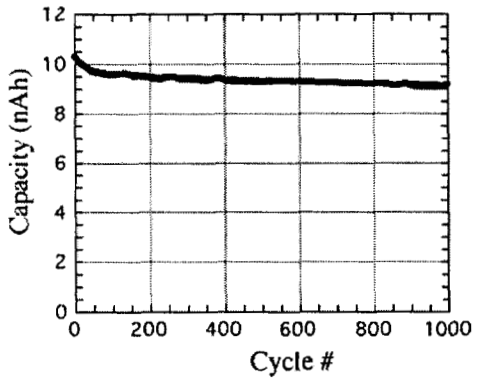

Figure 3 Capacity behavior as a function of charge cycles.

III. CHARGING ALGORITHMS FOR THIN FILM MICROBATTERIES

Lithium microbatteries commonly employ a constant current, constant voltage (CCCV) charging algorithm. In other words, a lithium microbattery is charged at a set current level (normally equal to 1C(capacity) rating of the microbattery) until it reaches its final voltage [3]. At this point, the controller switches over to constant voltage mode and provides the current necessary to hold the microbattery at this final voltage (4.25V per cell). During the constant voltage phase, current drops to a zero value over time. Thus, the charger should be capable of providing stable control loops for maintaining either current or voltage at a constant value, depending on the state of the microbattery [3].

TABLE I

LITHIUM BATTERY	CHARACTERISTICS
Capacity	1- 200nAH
Voltage Rating	
Rated Voltage	4.25V
Maximum Overcharge Voltage	4.3 - 4.4V
Electrical Breakdown	5.5V
Operating Range	4.25V – 3V
Deep Discharge to	0V
Charge / Discharge Rating.	
Rate of Charge	0.1C to 10 C
Efficient Rate	0.1C to 0.15 C
Normal Rate	1.0 C

TABLE I indicates that the capacity of the microbatteries is in the nano-ampere-hour range. As such, it is difficult to generate a finely accurate nanoampere current source using discrete components. To overcome this difficulty, pulse charging is considered because these microbattery chemistries respond well to pulses of current. The basic concept is to charge thin film microbatteries with large values of current, but with a small duty cycle at high frequency. This produces a fairly accurate net lower average current. In any microbattery stack array, the microbatteries are normally charged in parallel [4]. Serial charging is not practiced because of the difficulty in maintaining voltage balance [4].

II. MICROBATTERY POWER MANAGEMENT SYSTEM

Figure 4 is a block diagram representation of the integrated microbattery power management system, developed using Microwave Silicon-on-Insulator process rules. The microbattery power management system (μBPMS) is a system designed for programmability and flexibility features for a microbattery cell. Such features include charge/discharge option and characteristic monitoring of each cell. In addition, the system maintains a look up table indicating such parameters as number of charged cells, number of cells to be charged, number of faulty cells and the number of times a given cells has been charged/discharged. This data will be available to the user as a real time status of the system. The charge mechanism can be applied to single cells or multi-cells connected in parallel. The discharge mechanism can be applied to single cells or multi cells connected in parallel for user defined capacity requirements or cells connected in series for user defined voltage values.

The μBPMS consists of five parts: Charge Circuitry, Charge Controller, μBattery Switch Array System, Interface Circuitry and Controller as shown in Figure 4. The charge circuitry is a system that provides fifteen different current values in increments of 50nA and a constant voltage level. The current increments and/or constant voltage can be selected to charge the cells as required by the system. The charge controller system provides additional charge flexibility to the user by allowing pulse charging to be incorporated into the charging mechanism. The μBSAS consists of two parts: a

Switch Matrix and Switch Matrix Controller. The switch matrix allows the system to connect N cells in any desired configuration. While the switch matrix controller provides the desired control signals to achieve the desired configuration. The interface circuitry is a system component that allows the controller to communicate with the individual components of the μBPMS. The controller is a software/hardware integrated system that monitors the operation of the individual components of the system and perform tasks as outlined in the system specifications.

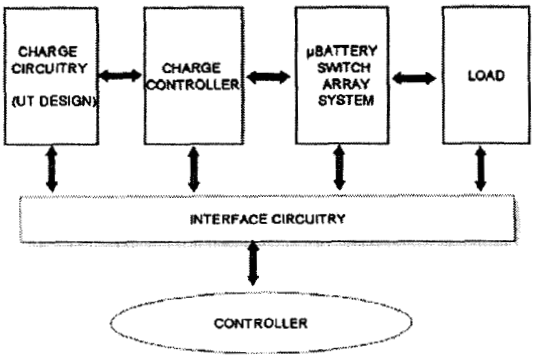

Figure 4 Microbattery power management system level architecture.

Figure 5 is the block diagram representation of the University of Tennessee's charger circuitry. The charger provides a digitally adjustable output current in increments of 50nA up to a maximum of 750nA. The output current is controlled using a four-bit, current-mode digital to analog converter (DAC). The controller is responsible for sending the four-bit control word to the charger circuitry. The constant voltage charging capability of 4.25V is implemented using a using a voltage regulator circuit. A flash analog to digital converter (ADC) constantly monitors the microbattery voltage and signals the charge controller when the microbattery is at full voltage capacity.

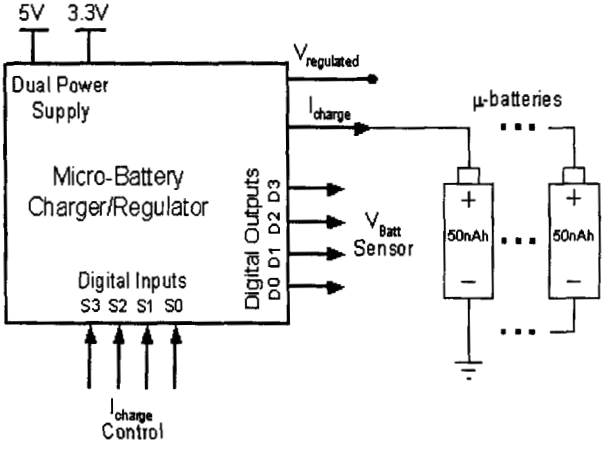

Figure 5 Microbattery charger architecture.

V. MICROBATTERY SWITCH ARRAY SYSTEM

The microbattery switch matrix groups the microbatteries in a serial or parallel combination to help satisfy the increased voltage or capacity needs of highly miniaturized loads. As seen in Figure 6, for charging cell 1, switch S1, S2 and S_CHARGE conduct while the other terminal switches block current.

For discharging cell 1, switch S1, S2 and the S_DISCHARGE form a closed path. Similar situations occur for other cells. As seen in Figure 7, if there exists a series discharge path (i.e. with all cells connected in series), then node Y experiences a potential of 17V (4.25V *4). Switches must handle such a high value of voltage. At the same time it can be observed that the switch S1 is used for both charging and discharging cell 1. As such, that switch must be bi-directional. It would also be desirable that the forward voltage drop associated with each switch during charging a cell be as negligible as possible.

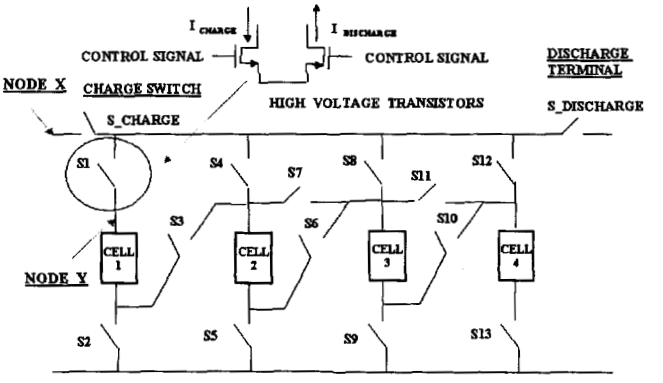

Figure 6 Microbattery switch matrix [6].

If one desires to retain a fully charged cell, for example cell 1, then switch S1 has to be fully off with no leakages present. If switch S1 experiences leakage then there exists a possibility wherein cell 1 could lose charge to Node X through switch S1. Initially, high voltage diodes were used for the design of the switches but experimental results showed that their leakage was in the range of 17nA (current required to charge a 50nAH microbattery at 1C rating is 50nA). That is too much leakage, so the design was discarded. After several experimental trials, high voltage MOS switches were found to satisfy the leakage requirements. Measurements indicated a leakage of 5pA.

Switch SC2 has an isolated bulk. This is because, when cell 1 and cell 2 are connected in series, the positive side of cell 1 is raised to a potential of 8.50V(4.25V*2). This forward biases the internal pn diode formed between the source and bulk, yielding a flow of current from Node X to Node Y, which is an undesirable factor. This has been eliminated by isolating the bulk and reverse biasing the pn diode.

At any point of charge cycle time, it is equally important that the voltage of the microbattery be known. This is because

the microbattery voltage sets the gate voltage of the charging switch. For example, if the microbattery voltage is at 4.1V, then the microbattery requires charging current to reach end-of-charge threshold value of 4.25V. If the gate voltage of switch SC2 is kept at 5V, then the device SC2 is not in a strong inversion region. This limits the amount of charging current going into cell 1. This difficulty is overcome by increasing the gate voltage to higher value, say 6V. Now, if the same gate voltage is maintained and if the microbattery voltage is at 0V, this could lead to device silicon breakdown. As such it is really important that the gate/bulk voltages for the different MOS switches be provided in a predictable fashion.

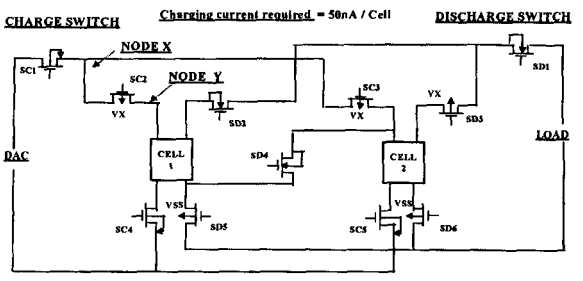

Figure 7 Implementation of a switch matrix using high voltage MOS switches.

This is achieved by an innovative gate/bulk driver controller which is described in the next section.

VI. MICROBATTERY GATE / BULK DRIVER CONTROLLER

Figure 7 schematic indicates presence of eleven MOS switches to achieve any desired grouping pattern between the microbatteries. The switches SC1, SC2, SC3, SD3 in this schematic require three different voltages (i.e., VB-Voltage of the microbattery, 0V, 4V) to implement the same (Table II). This can be indicated by two bits of digital information. For the other switches, the voltages are limited to 0V or 4V/5V. This again can be indicated by one bit of digital information. Adding up all the digital bits required to express the states of eleven MOS switches would give an eighteen-bit digital word. Now certain switches can be grouped together because they require the same voltage levels for any operating mode (Table III). This reduces or compresses the number of bits necessary to express a given switching state completely. As a result, the main controller (Figure 2) controls the microbattery switch array system through a six bit input control word only.

TABLE III Switches that can be grouped together:

Switches that can be grouped together	
SC2_BULK, SC3_BULK, SD3_BULK	→ Group A
SC1, SC2	→ Group B
SD1, SD2	→ Group C
SC4, SD6 (Inverse of SC4)	→ Group D

These six input lines are converted to a twelve-bit signal by using a Tree Decoder circuit. The block level representation of the switch matrix gate/bulk driver controller is shown in Figure 8.

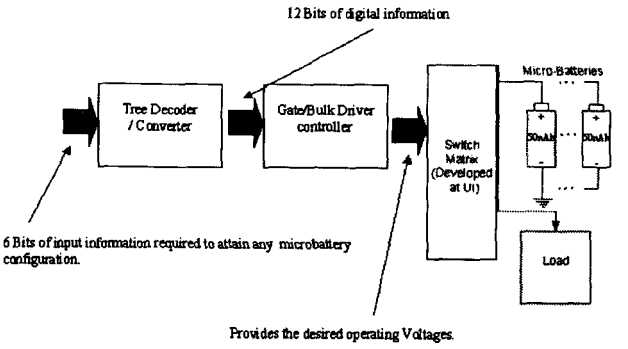

Figure 8 Switch matrix gate/bulk driver controller architecture.

Table II Gate/Bulk Driver Voltages For Different Mosfets:

SC1	SC2	SC3	SC4	SC5	SD1	SD2	SD3	SD4	SD5	SD6	
VB	VB	0V	5V	0V	5V	5V	0V	0V	0V	0V	→ A
VB	VB	VB	5V	5V	5V	5V	5V	5V	0V	0V	→ B
0V	0V	0V	0V	0V	0V	0V	0V	5V	5V	5V	→ C
4V	4V	4V	0V	0V	5V	5V	4V	0V	0V	5V	→ D

SC2_BULK	SC3_BULK	SD3_BULK	
0V	0V	0V	→ A
0V	0V	0V	→ B
0V	0V	0V	→ C
4V	4V	4V	→ D

A = Charging any microbattery
B = Charging microbatteries in parallel
C = Discharging microbatteries in parallel
D = Discharging microbatteries in series.
VB = Voltage of the Microbattery.

SC1,SC2,SC3,SD3 → 2 bits of information.
Other Switches → 1 bit of information.

The Tree Decoder circuit has two address lines A1, A2 (Figure 9) to enable the pass transistors used in the decoder. One of the three outputs is pulled high, depending on the two-bit address line [5]. The supply line voltage (VDD) is 3.3V and the threshold voltage drop (Vth) experienced across each PMOS transistor is 0.81V. The outputs of the Tree Decoder are connected to a Gate/Bulk Driver Controller as seen in Figure 9.

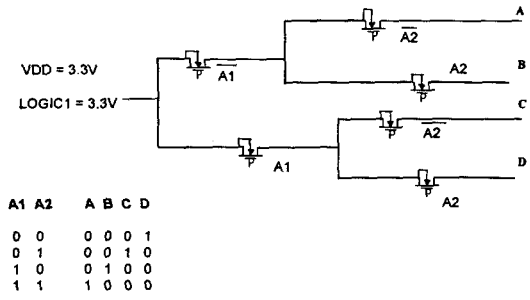

Figure 9 Tree Decoder circuit.

As mentioned before, the gate voltage of some MOS Switches (SC1, SC2, SC3, and SD3) are set by the microbattery voltage (VB). To attain best possible MOS switch operation three possible cases can be envisioned:

Case 1 3V < Microbattery Voltage < 5V
It is always desirable that the MOS devices operate in strong inversion region for best result. At the same time it is also important to maintain the gate-source voltage of the MOS devices to eliminate gate oxide breakdown.

Keeping the above-mentioned issues in mind, *a constant gate bias voltage of 6V is provided when the microbattery voltage is between 3V and 5V.* This limits the gate-source voltage to a value between 3V and 1V.

Case 2 2V < Microbattery Voltage < 3V
A gate voltage value of 4V is provided when the microbattery voltage reading is between 2V and 3V. This helps operate the MOSFET in a strong linear region.

Case 3 0V < Microbattery Voltage < 2V
For the MOS switch to operate in a strong saturation region, in this case, *the Gate voltage is maintained at 3.3V.*

To satisfy the different operating cases as mentioned above, a unique voltage generator for the gate/bulk terminal (Figure 10) is designed. The input lines A, B, C, D are the inputs from the Tree Decoder Circuit. The output X pushes to a voltage level based on the input word.

The supply voltage of the Tree Decoder is tied to a 3.3V rail. As such, the output signal equals the supply rail value for logic high condition. For Inverter A, the logical effort for falling transition equals the rising transition. Unfortunately, this is not true for the other Inverters. Inverter B will not produce a strong zero value. This is because, the PMOS will remain on even for logic high input. Introducing a weak PMOS structure solves this problem. The PMOS in Inverter C is tied to a higher supply rail. This effects the falling transition. A strong logic low is produced by connecting a strong N-channel MOS structure in parallel to the N-channel MOS in Inverter C.

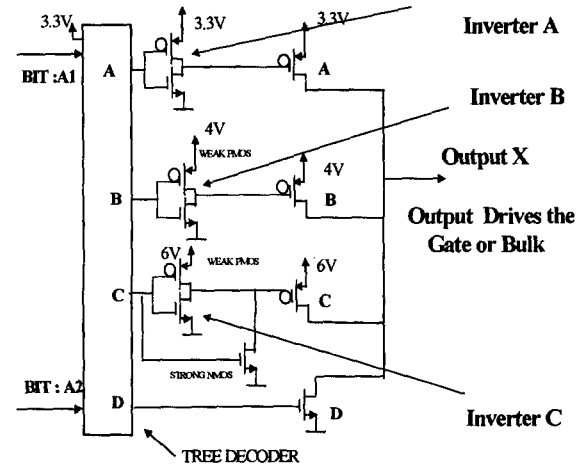

Figure 10 Voltage generator circuit.

Figure 10 schematic holds true only for switches SC1, SC2, SC3, and SD3. The same principle is used for other switches, which require two voltage values (0V or 4V/5V) to satisfy any microbattery configuration. The designs are implemented in a 3.3V low voltage, digital model of Microwave Silicon-on-Insulator process. This doesn't allow the devices to handle higher drain to source voltages. This problem can be solved by using a specially designed High Voltage MOS structure, as explained in the next section.

VII. HIGH VOLTAGE MOS STRUCTURE

Figure 11 gives a cross sectional overview of the High Voltage Microwave Silicon-on-Insulator MOSFET. This device is designed to have higher drain to source and drain to gate voltage. This is achieved by placing a lower doped drift region between the drain and the gate. Although this approach

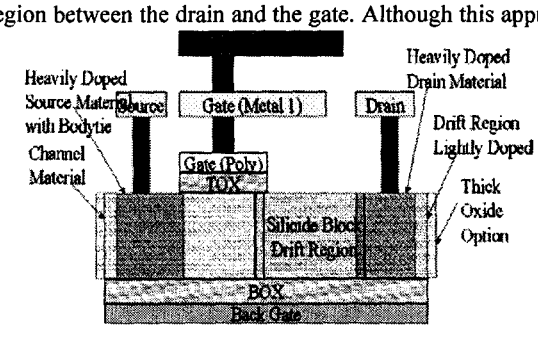

Figure 11 Cross sectional overview of the high voltage MOS structure.

increases the on- resistance of the transistor, the voltage tolerance of the device increases by two to eight times the rated process voltage in the sub-micron fabrication process. The gate overlap of the drift region and the length of the lightly doped drift region can affect the breakdown voltage and lifetime characteristics of the device. If the drift region is too long there may not be enough carriers that reach the channel region of the transistor. If the gate-overlap is too short the breakdown voltage of the transistor decreases.

Figure 12 represents the complete gate/bulk driver controller schematic to drive a two-cell switch matrix.

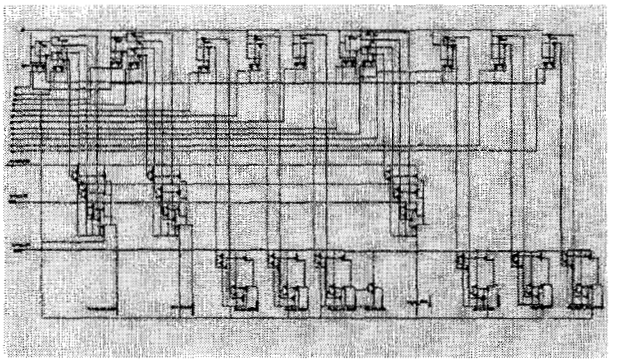

Figure 12 Two-cell microbattery gate/bulk driver controller.

VIII. SIMULATION RESULTS

Simulation results of the switch matrix gate/bulk driver controller, using 3.3V Silicon-on-Insulator SPICE models at room temperature are shown in Figures 13,14 and 15.

Figure 13 represents the input vector string of the Tree Decoder circuit. Voltage pulses are assumed at the input side to check the output vector values. Figure 14 reflects the simulation profile of the output string of the Tree Decoder circuit.

Figure 15 shows how switch matrix gate/bulk driver controller can provide switching voltages. The voltages are generated based on the values given by the Tree Decoder schematic. This simulation establishes the operation capability of the voltage generator illustrated in Figure 8.

IX. TEST CHIP

A test chip is being fabricated in a 0.35μm Microwave Silicon-on-Insulator process as seen in Figure 16. Test results will be presented in the conference. This designed controller is a subset of the complete microbattery power management system.

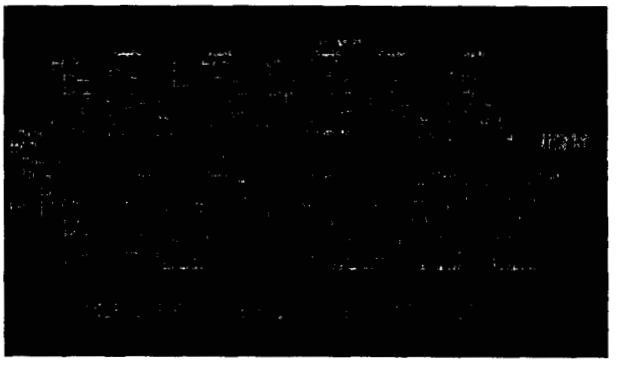

Figure 16 Microphotograph of the microbattery gate/bulk driver controller.

X. CONCLUSIONS

A gate/bulk driver controller for a two-cell switch matrix has been successfully developed. This controller is designed using an innovative voltage generator concept. The gate/bulk driver controller is a subset of the complete microbattery power management system. It sers the switch conditions for any grouping pattern of microbatteries. The controller is built using High Voltage MOS Structures, which can handle higher drain-to-source potentials in a 3.3V Microwave Silicon-on-Insulator process.

XI. ACKNOWLEDGEMENTS

The work described in this paper was carried out for the JPL,

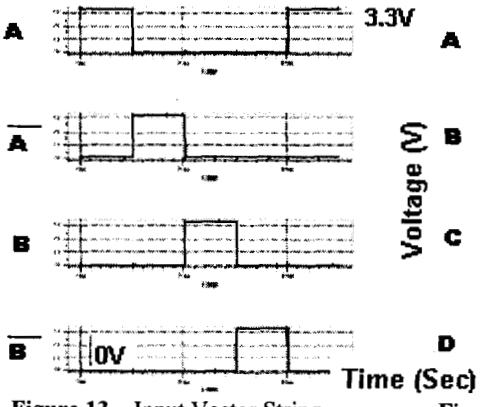

Figure 13 Input Vector String of the Tree Decoder.

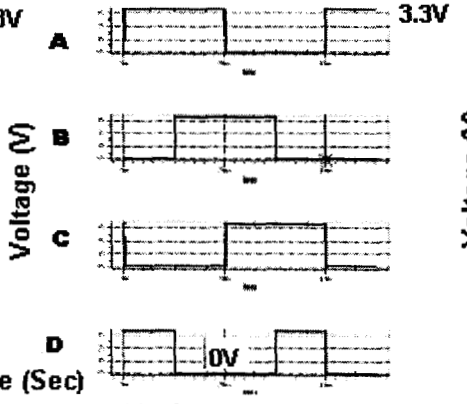

Figure 14 Output Vector String of the Tree Decoder.

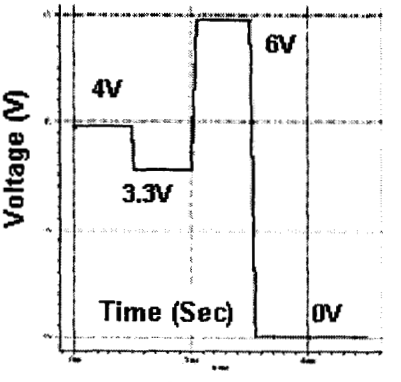

Figure 15 Output String of the Voltage Generator.

California Institute of Technology, under a contract with the National Aeronautics and Space Administration.

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