Small Computational Node Embedded within a High-Speed Network Fabric for Spacecraft Flight Applications

R. Kevin Watson, Richard D. Petras, Gary S. Bolotin
Jet Propulsion Laboratory, California Institute of Technology
Pasadena, California, 91011

Abstract: JPL is developing a highly integrated Micro Avionics Module aimed at the avionics needs of both small and large spacecraft and planetary rovers that will operate within a moderate radiation environment. The Micro Avionics Module will be based upon the commercially available Xilinx Virtex-II Pro field programmable gate array. The resulting product will be a low power, highly scalable, microprocessor-based avionics package that can be used alone or within a network. For example, such an avionics module could become the core C&DH computer of a Mars Scout-class spacecraft, or a stereo vision processor for a larger planetary rover. The key characteristics of this Micro Avionics Module are:

- Small size. The module will be less than ten cubic inches in volume.
- Low power. Depending on how the module is configured, milli-watts to a few watts of power consumption are anticipated.
- High computational power. One, two, or four PowerPC 405 processors running at up to 400 MHz are embedded within the Virtex-II Pros gate array. The processors can be voted against each other for increased fault tolerance or run independently for additional processing capability.
- Support for off-the-shelf operating systems like VxWorks and Linux.
- High I/O count. Hundreds of I/O pins are available. Each is programmable for voltage swing, impedance, and single-ended or differential usage.
- Large number of re-configurable FPGA gates. Up to eight million gates that can be used to implement dedicated functions like brushless motor controller(s), IEEE-1394 interface(s), software defined digital radio, etc.
- Architectural provisions such as a temperature adaptive power supply or self-controlled local heating so that the components can operate in ambient temperatures that are outside their normal operating temperature.
- Networking capability. Implementing a network controller(s) within the FPGA portion of the Virtex-II Pro is very straightforward and allow multiple modules to be operated in a distributed manner across slow (e.g., I2C) and fast, low latency (e.g., gigabit ethernet) networks.

We will discuss the architecture and implementation details including the design methods employed to harden the Virtex-II Pro for moderate radiation environments.