

## Electrochemically Deposited Semiconductor Nanowires

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Miniaturization of electronic devices is of great interest for several applications and successful miniaturization into efficient devices will require approaches to making nanometer scale structures of semiconductor elements for those devices. For the past several years, techniques for fabricating thermoelectric devices on the micrometer scale have been studied for cooling and for power generation applications [1]. Thermoelectric devices may be used both for generation of primary power from heat sources and by harvesting waste heat for additional power generation. In addition, as electronic devices become smaller and electronics are positioned in greater density, needs for increased localized cooling have developed.

Recent work in thermoelectric theory has predicted that the efficiency of a thermoelectric device can be increased by a factor of  $\sim 3$  if the leg diameter can be decreased to a size at which quantum confinement and interface scattering effects will occur [2, 3]. Nanowire semiconductors of  $\sim 10$  nm diameter will increase performance efficiency through enhanced charge carrier mobility by quantum confinement effects and by increased phonon scattering owing to low dimensionality. In addition, the high aspect ratio of the wires ( $10$  nm  $\times$   $20$ - $50$   $\mu\text{m}$ ) will assist in maintaining a large  $\Delta T$  at low heat flux.

Nanowires have been grown in alumina templates with pore diameters of  $100$  nm and  $40$  nm. In order to make high efficiency devices, templates with pore diameters of  $5$ - $15$  nm are necessary. Templates can be made by anodizing aluminum; pore size can be controlled by adjusting the anodization conditions, including current density and electrolyte composition. Templates with pore sizes from  $12$  to  $100$  nm have been made, as shown in Figure 1.

For use in devices, nanowires can be deposited electrochemically in templates as bundles of wires  $10$ - $50$   $\mu\text{m}$  in diameter, with each nanowire distinct, and contacted in parallel. Figure 2 shows a  $50$   $\mu\text{m}$  diameter bundle; the template was masked using a thin layer of  $\text{CrO}_2$ . Devices under study based on nanowire elements include thermoelectric generators and coolers and microcalorimeters. Other applications include solar cells with high surface area and light trapping capability, high surface area filters, and gas concentrators.

This paper will discuss electrochemical deposition of nanowire semiconductors, fabrication of alumina templates with  $5$ - $100$  nm pore diameter, and electronic and thermoelectric properties of nanowires expected to exhibit enhanced properties induced by low dimensionality.

### References

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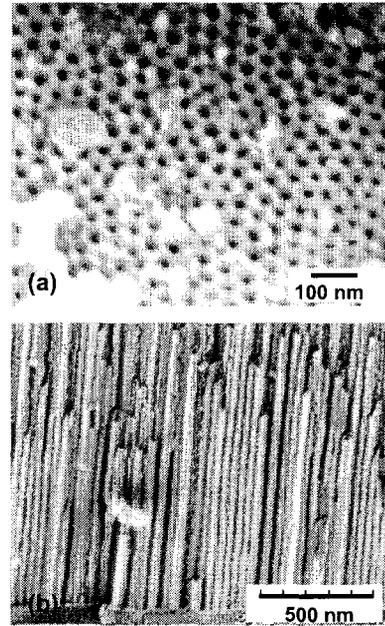


Figure 1. Template made by anodizing a  $10$   $\mu\text{m}$  thick layer of aluminum on silicon, with pore diameter  $12$  nm. (a) top view; (b) cross section.

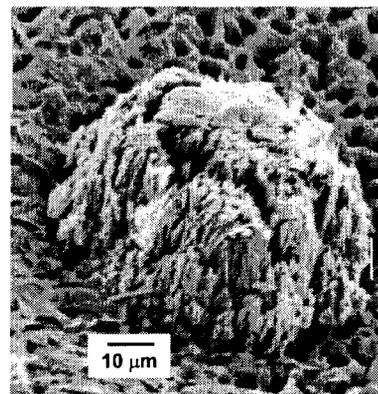


Figure 2.  $\text{Bi}_2\text{Te}_3$  nanowires,  $200$  nm diameter, grown in a  $50$   $\mu\text{m}$  bundle. The alumina template has been etched away.