HTMT

REALIZATION OF SUPERCONDUCTOR VLSI

FIRST FAB RUN—April 2000
- Initial 4 kA/cm² process mm
- Shift register (SR) tests (4, 16, 64, and 256 bits long (12 J/bit))
- Individual gate (logic, memory, I/O) and transmission line tests
- Thermal noise, electrical pulse jitter test

Shift Registers

FLUX-1 Sept. 2001
- 10.65 mm x 13.2 mm chip
- 1.75 μm, 4 kA/cm² Nb technology
- 20 GHz internal clock (design)
- 5 GB/s inter-chip data transfer
- Scan path diagnostics included
- 65000 junctions, 5000 gate equivalent
- Power dissipation = 5 mW @ 4.5K
- 40 GOPS peak computational capability (8 bits @ 20-GHz clock)
- Engineering flaws discovered during test

THIRD FAB—Dec. 2000
- All components for FLUX
- Individual gates
- First stage decoder
- Clock controller
- New memory cells
- Registers
- Transmission lines expts.
- ALU slice
- Interface parts / scan path
- Program counter
- Off-chip communications tests

FLUX 1R1 Aug. 2002
- 10.65 mm x 10.65 mm
- 63000 junctions
- 25 GHz clock (design)
- Power dissipation = 9.2 mW
- Currently under test

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