Reset Noise Suppression in Two-Dimensional CMOS Photodiode Pixels through Column-based Feedback-Reset

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Abstract

We present a new CMOS photodiode imager pixel with ultra-low read noise through on-chip suppression of reset noise via column-based feedback circuitry. In a 0.5 μm CMOS process, the pixel occupies only 10x10μm² area. Data from a 256² CMOS imager indicates imager operation with read noise as low as 6 electrons without employing on- or off-chip correlated double sampling. The noise reduction is achieved without introducing any image lag, and with insignificant reduction in quantum efficiency and full-well.

Introduction

Comparatively higher read noise in CMOS imagers is one of the main reasons why its performance is considered inferior to charge-coupled devices (CCDs) under low-light-levels. The read noise of a conventional photodiode pixel or a pinned-photodiode pixels operated in snap-shot mode, is usually dominated by the reset noise at the sense node of the pixel. Reset noise in a CCD is eliminated through correlated double sampling (CDS). However, on-chip CDS, in general, is not possible for CMOS imagers, since they are operated in “read-first reset-later” mode. Reset noise in CMOS imagers can be eliminated through off-chip CDS, but only at the cost of additional complexities and a full-frame buffer, increased flicker and white noise, and hence is generally avoided.

Recently there have been several attempts to obtain low-noise in CMOS imagers by suppressing front-end reset noise. It has been observed that a pixel reset under weak-inversion conduction (the so-called “soft-reset”) demonstrates sub-kTC noise due to a negative feedback mechanism inherent in the reset process [1, 2]. Reduction of reset noise has been achieved using external capacitive active feedback and band-limiting [3]. Although more than 4x reduction in reset noise has been reported, the size of the feedback circuitry limits the implementation to 1-D pixels. Noise as low as 25 electrons in 2-D CMOS imaging arrays without CDS have been reported by using tapered reset [4], while capacitive-divider based reset noise reduction schemes with relatively large pixel sizes have been demonstrated [5]. Other approaches involving in-pixel CDS has been reported [6], although it is not suited for implementation of small sized pixels required in most commercial imaging applications. These approaches provide either limited noise suppression or only 1-D pixel implementation.

In this paper, we present a new technique for suppression of sense-node reset noise by resetting a pixel through a per-column feedback amplifier. Unlike other proposed techniques for reset noise reduction, the noise-suppressed reset level is generated via column-based circuits, leaving the pixel structure essentially unchanged except for the addition of a single FET inside the pixel. Thus, it is fully compatible with implementation of two-dimensional (2D) imaging array in a small pixel pitch (10 μm in 0.5 μm CMOS technology). The technique enables low-noise pixels with minimal reduction in quantum efficiency, without requiring an increase in the conversion gain for reduction of the effective input-referred noise, and without introducing any image lag.

Fig. 1: CMOS imager pixel with column-feedback reset
**Pixel Design & Operation**

Fig. 1 shows the schematic of the low-noise pixel and the associated column-based feedback circuits. The pixel is implemented using a conventional n-well-to-p-substrate photodiode ("3-T") pixel. However, unlike a 3T pixel, it consists of only one additional reset-activation FET $M_{act}$, although it has an identical number of buses. All other feedback and feedback-assists circuits are column-based. The column-bus carrying the pixel voltage output is connected to the inverting input of a column-based high-gain feedback amplifier, whose output sets the reset level at the gate of $M_{reset}$ during reset, as shown in Fig. 1.

Reset noise results from the random fluctuations in the charge (or voltage) on the photodiode due to the intrinsic noise in the reset FET. These random fluctuations are frozen on the photodiode capacitance when the pixel is disconnected from the reset FET. Therefore, reset noise can be suppressed by reducing the amount of random fluctuations during reset. In our approach, fluctuations on the sense node are suppressed by sensing its instantaneous variation, and appropriately adjusting the drain current flow by modulating the gate of $M_{reset}$ through the high-gain negative feedback amplifier.

The pixel operates in "read-first reset-later" mode. Two samples are collected from each pixel – one prior to reset, and one following reset. As shown in the pixel timing diagram of Fig. 2, the first sample is collected while holding $\Phi_{set}$ and $\Phi_{flush}$ low, and setting $\Phi_{reset}$ and $\Phi_{init}$ high. At this point, the feedback bus is disconnected, and the column-bus voltage ($V_{col}$) proportional to the integrated charge on the photodiode is sampled at the bottom of the column. Following this, the pixel is reset. The reset phase consists of two phases – "hard-reset" phase followed by the "feedback-reset" phase. Hard-reset of the pixel is accomplished by momentarily pulsing $\Phi_{flush}$ high, while returning $\Phi_{reset}$, $\Phi_{init}$, $\Phi_{flush}$, and $\Phi_{reset}$ low. The R-C network is also activated at this time. As it charges $V_{reset}$ to the final level, the high-gain opamp continuously adjusts the feedback reset level ($V_{reset}$) to hold the differential input at virtual ground by making $V_{col}=V_{reset}$. In the process, the high-gain negative feedback compensates for any fluctuation at the sense node, and resets the pixel with less than KTC noise. The pixel does not reach equilibrium, but is reset in "soft-reset" mode under continuous feedback. However, soft-reset does not introduce any image lag, since it is preceded by a hard reset [1]. Sampling of the reset level is carried out with $\Phi_{init}$ high, following which the pixel $\Phi_{reset}$ is pulsed low simultaneously disconnecting the pixel, and ending the reset process.

Under soft-reset, the current flow is essentially unidirectional, limiting the effectiveness of the feedback process. In order to overcome this problem, the R-C network is used. The R-C network provides a constantly varying reference level providing the required modulation of drain current in $M_{reset}$. For this purpose, it is sufficient to make the time-constant of the R-C network smaller than that at the sense node.

The noise reduction stems from the fact that feedback is applied to a sense node that is not in thermal equilibrium. Fig. 3 shows the simplified circuit for noise modeling, where the pixel source-follower and the high-gain opamp are merged into one amplifier block of gain $A$ and an equivalent input transconductance $g_{ma}$. The pixel diode is modeled as a capacitor $C_{pd}$, and the transconductance of $M_{reset}$ is $g_{ma}$. Effective noise of $M_{reset}$ is reduced under feedback, since a change in the source of $M_{reset}$ is balanced by an amplified and opposite change at its gate, while the noise of the op-amp is reduced due to bandlimiting at the sense node. By adding the filtered noise components from $M_{reset}$ and the opamp, and by integrating over all frequencies, the effective noise at the sense node with capacitance ($C_{pd}$) is given by:

$$\left\langle V_{d}^{2} \right\rangle = \frac{K T}{C_{pd}} \left[ \frac{1}{A_{o}} \left( 1 + A_{o}^{2} \frac{g_{ma} C_{L}}{g_{ma} C_{pd}} \right) + A_{o} \left( 1 + \frac{g_{ma} V_{d}^{2}}{4 K T} \right) \right]$$

(1)
Results

Fig 5. Pixel layout with 10% pixel area in 0.5 Jum process.

The key to understanding the performance of the RC network is to recognize that the RC network can be simplified to a single-pixel RC network. The RC network consists of a source follower and a single-pixel RC network. The RC network can be represented as a single-pixel RC network. However, this does not pose a problem, since the source follower and the RC network are connected in parallel.

The RC network has two main components: the source follower and the RC network. The source follower provides the input signal to the RC network. The RC network then processes the signal and produces the output signal.

The RC network is a circuit that uses a combination of resistors and capacitors to perform a specific task. In this case, the RC network is used to generate a voltage signal that is proportional to the input signal.

The RC network has four main components: the input signal, the source follower, the RC network, and the output signal. The input signal is the signal that is applied to the RC network. The source follower provides the input signal to the RC network. The RC network then processes the signal and produces the output signal. The output signal is the signal that is generated by the RC network.

The RC network is a powerful tool for processing signals. It can be used to perform a variety of tasks, such as filtering, amplification, and integration. The RC network is a versatile circuit that can be used in a wide range of applications.

Fig 5 shows the layout of the pixel, arranged in a 2-D array. The pixel is divided into four sections, each corresponding to a different part of the pixel.

The left part of the pixel is the source follower, which provides the input signal to the RC network. The right part of the pixel is the RC network, which processes the signal and generates the output signal.

The bottom part of the pixel is the output signal, which is connected to the next stage of the circuit. The top part of the pixel is the input signal, which is connected to the source follower.

The RC network is a simple circuit that is easy to understand and implement. It is a versatile tool that can be used in a wide range of applications. The RC network is a fundamental building block in many electronic systems.
Furthermore, since a bank of 256 opamps operates in parallel, the opamp gain was limited to 10\(^{-12}\). Without feedback, the read noise in electrons expectedly decreased with increasing conversion gain, as indicated by the fitted trace (solid lines), with the conversion gain being inversely proportional to the sense node capacitance. A similar dependence is obtained when the pixel was operated in the feedback reset mode, except that a 5-6x reduction in read noise is observed for all conversion gains. Fig. 7 also indicates that read noise as low as 6\(\times\) is obtained without CDS. Further reduction in noise can be obtained by reducing the noise floor below 80 \(\mu\)V (primarily through an increase in the sampling capacitance), and by increasing the opamp gain. Compared to a conventional 3-T pixel of similar size, no measurable reduction in quantum efficiency was observed. Image lag was immeasurable when operated in either modes of reset.

One potential problem is that if the \(\Phi_{ed}\) swing is limited to a maximum of \(AV_{th}\), the sense node is reset one threshold lower than that achieved with a conventional pixel. In turn, this translates to a reduced signal handling capacity. In our implementation, since it had to fit in a 10 \(\mu\)m column-pitch. Furthermore, since a bank of 256 opamps operates in parallel during the reset phase, the tail current of each opamp was limited to 10 \(\mu\)A, in order to minimize problems stemming from resistive drops on the power and ground bus. As a result, the opamp gain was limited to < 40 dB. The signal chain noise was measured to be < 85 \(\mu\)V r.m.s.

The 256\(^2\) imager was operated both in a conventional hard-reset mode and in a feedback reset mode. Figure 6 shows an image captured by the imager while operating in the feedback-reset mode of operation. No photonometric degradation of the image was observed between normal-reset and feedback-reset modes of operation. Fig. 7 plots the measured total read noise as a function of conversion gain. Without feedback, the read noise in electrons expectedly follows the \(\sqrt{\Phi_{ed}}\) curve, as indicated by the fitted trace (solid lines), with the conversion gain being inversely proportional to the sense node capacitance. A similar dependence is obtained when the pixel was operated in the feedback reset mode, except that a 5-6x reduction in read noise is observed for all conversion gains. Fig. 7 also indicates that read noise as low as 6\(\times\) is obtained without CDS. Further reduction in noise can be obtained by reducing the noise floor below 80 \(\mu\)V (primarily through an increase in the sampling capacitance), and by increasing the opamp gain. Compared to a conventional 3-T pixel of similar size, no measurable reduction in quantum efficiency was observed. Image lag was immeasurable when operated in either modes of reset.

In conclusion, we have presented a high resolution 2D-CMOS imager with a new pixel and a reset scheme that affords nearly an order of magnitude reduction in reset noise through column-based feedback during reset. With the feedback circuitry residing outside the pixel, the fill-factor of the pixel is not compromised. As a result, the pixel maintains high QE, zero image lag, potentially high signal swing, and ultra-low noise (6\(\times\)) without CDS, significantly improving CMOS imager dynamic range and performance in low-light-levels.

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References