

MICROELECTRONICS PACKAGING RESEARCH DIRECTIONS FOR AEROSPACE APPLICATIONS

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INTRODUCTION

The Roadmap begins with an assessment of needs from the microelectronics for aerospace applications viewpoint. Needs Assessment is divided into materials, packaging, components, and radiation characterization of packaging. Materials research benefits microelectronics packaging, components, and radiation characterization. Greater functional density packaged in a smaller form factor is the most persistent challenge facing the microelectronics packaging research community. Feature size reductions are being introduced in silicon technology at an accelerating rate. As a result, there are more functions and input/outputs (I/O) within each integrated circuit (IC).

The use of Commercial-Off-the-Shelf (COTS) components is of interest to NASA due to wide availability and cost, however the need for higher reliability and longer field life is of concern. Use of plastic BGA (PBGA) packages continues to cause problems. In addition to being moisture sensitive, the assembled package can have rework issues. NASA research with electronic noses, System-in-a-Package and System-on-a-Chip technologies, and the identification of manufacturing processes, materials, quality, and reliability of embedded passive interconnects required for extreme temperature applications will be discussed. Single event upset and non ionizing energy loss contributions to a mission's cumulative radiation exposure are areas of component packaging radiation hardening technique research. Predictions of technology lifecycle development are embedded within the Needs Assessment discussion. Technology challenges and forecasts are also given. Table 1 gives an overview of technology challenges [SIA]. EMI refers to electromagnetic interference, k to dielectric constant, and EDA to electronic design automation.

NEEDS ASSESSMENT

Materials

Finer particle size for eutectic solder is required for increased density and smaller I/O pitch. New lead-free alloys will require further process optimization. No clean solder research in the area of solder ball prevention and reduction of residue levels is also needed. Residue levels become more critical for finer pitch and array components. Solder mask research will be required to reduce solder balls and improve adhesion to underfills, encapsulants and conformal coatings. Standardization for fluxless systems is also needed.

Coefficient of Thermal Expansion (CTE) mismatch between package materials and substrates is an area for further research. Flip chip interconnection is one example. In general, leadless chip carriers have a problem with the CTE board interconnection match.

Table 1. **Packaging** Technology Challenges [SIA]

Challenges for ≥ 65 nm through 2007	Issues
Improved underfills for flip chip on organic Substrates	Improved flow, faster dispense/cure, better interface adhesion, lower moisture Absorption Improved adhesion, smaller filler size, and improved flow for mold based underfills
Coordinated design tools and simulators to address chip, package, and substrate co-design	Mixed signal co-design and simulation environment Faster analysis tools for transient thermal analysis and integrated thermal mechanical analysis Electrical (power disturbances, EMI, signal integrity associated with higher frequency/current, and lower voltage switching) Commercial EDA supplier support
Impact of Cu/low k on packaging	Direct wirebond and bump to Cu Bump and underfill technology to assure low k dielectric integrity Improved mechanical strength of dielectrics Interfacial adhesion
Pb, Sb, and Br free packaging materials	Lower cost materials and processes to meet new requirements, including higher reflow temperatures. Reliability under thermal cycling (stress and moisture)
Challenges for < 65 nm beyond 2007	Issues
Package cost may greatly exceed die cost	Research investments required for packaging cost reduction are decreasing
Small, high pad count	Array I/O pitches below 80 microns

The successful integration of a porous low dielectric constant (k) material as an interlevel dielectric depends on the morphology of the embedded porosity. Simple site percolation models have been utilized to investigate porosity properties of low- k dielectrics with respect to the current technology trends. Significant differences between two generations of porous dielectrics, $k < 2.4$ and $k < 2.1$, have been found. The porosity fraction in the latter is above the percolation threshold, which may have serious impact on the materials physical properties [Petkov]. More research in this area is needed.

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New failure prediction models are required for epoxies and Z-axis adhesives. Additional research is also needed because epoxies and Z-axis adhesives require faster curing times and more stable formulation. The presence of moisture during curing of epoxies can alter final properties including glass transition temperature (T_g), degree of cure, mechanical properties, the role of micro-voids (near die metallizations), and the level of extractable ionics [Hagge]. While anisotropic adhesives and non-conductive adhesive interconnection techniques are very promising, the placement of components is more critical with these adhesives. The anisotropic adhesives have lower mechanical strength and therefore weaker links, and repair and rework are more difficult. Although such interconnections are already being used, the aging mechanisms are not well understood and the degradation of material performance with time needs more research [IME].

Softer unreinforced board materials are becoming more common and are potentially more vulnerable to damage or distortion by testing. This could affect follow on processes. Microvia planarity may be altered influencing the soldering process. Smaller board geometries are driving materials to lower dielectric constants and lower loss dielectrics with the need for higher conductivity conductors such as copper and silver. Major processing changes are needed by fabricators to meet the new design requirements for component interposers. Laminate copper thickness will need to be 25 μm or less to satisfy finer line width requirements [IRC]. Manufacturers of microprocessor modules often employ additive plating technology to achieve the required conductor widths, now 2 mils or less. Copper thinning technology is also being used to achieve the required copper thickness to etch much smaller line widths. Solder mask definition will also require accuracy well below the typical 50 μm accuracy presently available [IPC].

Process optimization is necessary for conformal coating with low volatile organic compounds. Faster flowing and curing (snap cure) underfill formulation will be required for fine pitch arrays. Underfill match to interconnect CTE also needs further research. A combination flux/underfill is another desired technology.

Packaging

Increasing functional density packaged in a smaller form factor is the greatest problem facing the microelectronics packaging research community. Another area of research concern for aerospace application is the use of COTS parts. COTS components are of interest to NASA due to wide availability and cost, however the need for higher reliability (NASA Grade 1) and longer field life is of concern. The cost of testing COTS to assure high reliability often exceeds the purchase price of the COTS parts. Three dimensional Plastic Encapsulated Microcircuits (PEM) COTS reliability is one such area requiring more work.

Feature size reductions are being introduced in silicon technology at an accelerating rate. As a result, there are more functions and I/Os within each IC. In the year 2005 predictions are that ICs will have as many as 2000 I/Os [IPC]. Table 2 shows directions for packaging research. Table 3 shows current and expected directions for ceramic technology. Several research needs are embedded within these trends.

Table 2. Packaging Trends

Metric	2004-2005	2006-2010
Extreme Environment Chip Rise Time (Nanoseconds)	1.5	0.8
On Chip Frequency (MHz)	300	350
Minimum Device Voltage (Volts)	2.5	2
Thermal Dissipation (Watts Avg/Max)	10/40	16/70
Usable Board Area (cm ²)	130	125
Thickness (mm)	1.5	1.52
Layer Count (Average)	4	2
Line Width/Space (Minimum Internal μm)	100/100	75/75
Minimum Microvia Diameter-Buried or Blind In μm	125	N/A
Maximum I/O Count	512	760
Total Number of Components	300	290
Maximum Total Number of Array Components	42	52
lamine chip carrier design features		
Line Width (μm)	25-50	12.5-25
Board Thickness (mm)	0.2	< 0.2
BGA Land Pitch (mm)	0.8	0.65
Device I/O	>1000	2000+
Board Design Features		
Conductor width (μm)	45	36
Board Thickness (mm)	0.5	0.5
Minimum SMT Microvia (mm)	0.1 x 0.5	0.1 x 0.4
Maximum Device I/O	1500	1500
THERMAL		
T _g	150-260	170-260
x-y access CTE	10-16	8-16
z access CTE (ppm below T _g , [30-260 °C])	60-85	50-75
MECHANICAL		
Inner Layer (1oz.)	1.1-1.4	0.7-1.1
Outer Layer (½ oz)	0.9-1.3	0.6-1.0
CONDUCTOR		
Profile RtM (μm)	6-10	4-8
Tensile Strength (KSI)	50-80	50-100
SUBSTRATE		
Dimensional Stability variation after etch ($\mu\text{m}/\text{cm}$)	< 2	1
Glass Reinforcement Weight Tolerance (%)	2-3	1-2
Resin Content Tolerance (%)	2	1-2
Single Ply Reinforcement (% of Multilayer)	15-30	25-50

Table 3. Ceramic Technology Trends [IPC]

Technology	Trend
Dielectric Paste	Tape/LTCC
Screen Printed Dielectric/Vias	Dielectrics with Photopatterned or Imaged Vias Tape Dielectrics with Photopatterned Vias
Screen Printed Conductors	Photopatterned Conductors
Surface Passive Components	Buried Passive RLC Components
Loss Tangent < 10 ⁻³	Loss Tangent < 10 ⁻⁹

Chip packaging has migrated from ceramic to organic area array packages such as Ball Grid Arrays (BGA), chip scale packages, and flip chips. In addition, the use of area array packages is driving the need for high reliability microvia printed wiring boards [Hagge]. Research needs also include development of further solder joint attachment reliability modeling for array packages, including discrete arrays for the variety of use environments. Use of plastic BGA (PBGA) packages continues to cause some problems. In addition to being moisture sensitive, the assembled package can have rework issues. The PBGA balls may be difficult to re-ball after collapse during rework. The PBGA package is also susceptible to warpage. Planarity defects cause the edges of the package to lift up, resulting in poor connection for the outer rows. Larger PBGA packages are more susceptible to warpage than the smaller packages [Fu].

Moisture absorbed during field life can interact with ionic material contained within plastic packages. The level of ionic content strongly influences failure rates. Lower ionic content correlates strongly with higher reliability in humid environments. The ionic materials are present either as residues from IC fabrication or assembly, or can come from the constituent materials contained in encapsulants, die adhesives, or laminate substrates. The failure mechanisms include both corrosion of aluminum bond pads or IC circuit lines, and degradation of gold-aluminum interfaces in wirebonds. Power cycling during field life is another factor effecting moisture adsorption and its influence on the field life itself [Simon].

Components

Greater density packaged in an increasingly miniaturized device is also the largest challenge facing microelectronics components research. These requirements drive higher power, even with operation at lower voltages. Silicon carbide high voltage diode components have been observed to degrade under forward polarization. Specifically, the forward voltage drop can increase from 3.5 up to 5 Volts or more over a period from minutes to days. With voltage drop, dark areas can appear in diode electroluminescence and the minority carrier lifetime diminished [NCSR].

Monolithic Microwave Integrated Circuits (MMIC) can insulate and be scaled to various diameters using inexpensive Czochralski or Kyropoulos substrate single crystal growth techniques. III-Nitride materials on lithium gallate have demonstrated low dislocation densities and have been implemented in high reliability optical devices. More research into components utilizing lithium salt substrates such as lithium gallate and lithium

aluminate is needed. These substrates offer new methods of achieving high reliability III-Nitrides. They have a small lattice match to III-Nitrides, are molecular beam epitaxy compatible, and offer opportunities to lattice match high compositions of Al for solar blind applications. These salt substrates also possess cleavage planes, can be chemically etched affording the removal of devices for heterogeneous integration onto heat sinks and mirrors, and permit substrate vias for low inductance power connections for MMIC [Irwin, NCSR].

Other research needs include determining the origin of current collapse in nitride high electron mobility transistors and SiC metal semiconductor field effect transistor components. Power actuated switching module I & II substrate reliability is yet another area requiring further research. There is also a need for high k , low leakage dielectrics for metal insulator semiconductor devices. The creation of light emitting devices operating in the ultraviolet portion of the electromagnetic spectrum is an attractive area of research for both military, space, and commercial applications, including: secure line of sight communications, solid-state lighting, bio-detection, and remote sensing (especially of biologic agents) [Irwin].

Microelectromechanical systems (MEMS) reliability assurance also requires further research. Some of these issues include fracture failure mechanisms and fracture toughness as well as interfacial strength. Other material properties of MEMS are also reliability issues. These include elastic modulus, Poisson's ratio, and CTE match with the substrate. Gyroscopic MEMS and radio frequency MEMS are two of the areas of NASA MEMS research. Test methods for micro-optoelectromechanical systems interconnect reliability are also needed.

MEMS technology can provide a relatively inexpensive method to make chemical, inertial, thermal, or pressure sensors. MEMS are currently used to measure pressure, acceleration, material strain, fluid flow, surface profiles, and chemical compounds. The sensing components of these devices are usually two-dimensional in shape, utilize the electrical and mechanical properties of bulk silicon and deposited thin films, and have been miniaturized using silicon-based integrated circuit fabrication techniques. Three-dimensional structures have been developed using folded polymers or precision assembly of 2D structures. An accurate measurement of layer thickness and profile is critical to successful MEMS device fabrication and subsequent function [FEI]. Utilizing a Focused Ion Beam (FIB) system, these measurements can be taken without special chip holders or wafer cleavage. This system uses a gallium ion beam to mill a portion of the device and an electron beam to produce a high resolution image of the MEMS cross-section [Lin].

Board test is another ripe research area. Efficiency of translation methods for converting different grid pitches from test bed to device or board I/O pattern is a problem for many components. Test beds are commonly on 0.100 inch centers but devices are now created with a variety of different pitches in metric dimensions. Some features must be protected from damage and require nearby test points to be used rather than direct testing. This presents a risk because the link between the test point and the actual contact is potentially

open and may require verification by other methods, such as optical. Tolerance of spring loaded test probes relative to their carriers can also be a cause for inaccurate test results (0.4 mm misregistration possible) [IPC]. Figure 1 shows additional parts testing challenges [GSFC].

Testing Issues

- Die Penetration
 - The Pentium III die is a flip chip solder bubble bonded die.
 - The sensitive regions of the processor are approximately 900 microns deep in the silicon die.
 - Thermal issues compound this by requiring cooling material in the beam line, as well.
- Thermal
 - The Pentium III can draw in excess of 20 watts of power
 - The packaged heat sink and cooling fan are removed and replaced with a water-cooled jacket, that is thinned to 10 mils over the die.
 - The large thermal issue is also the reason that the die cannot be thinned.

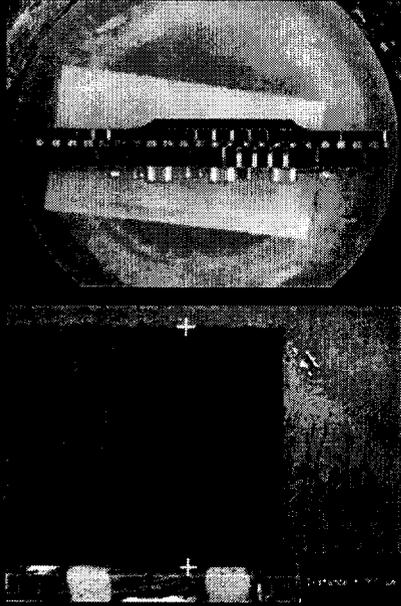


Figure 1. Component Testing Challenges [GSFC]

Radiation Characterization of Packaging

Much research is required in the area of Single Event Upset (SEU) packaging radiation hardening techniques. Related issues include charge dissipation which consumes IC power and temporal filtering which reduces speed. Charge dissipation and temporal filtering can also increase Linear Energy Transfer (LET) [Boeing]. Spatial redundancy, which consumes additional substrate area, is another packaging challenge faced when addressing component radiation hardening to reduce SEU [Bytkin].

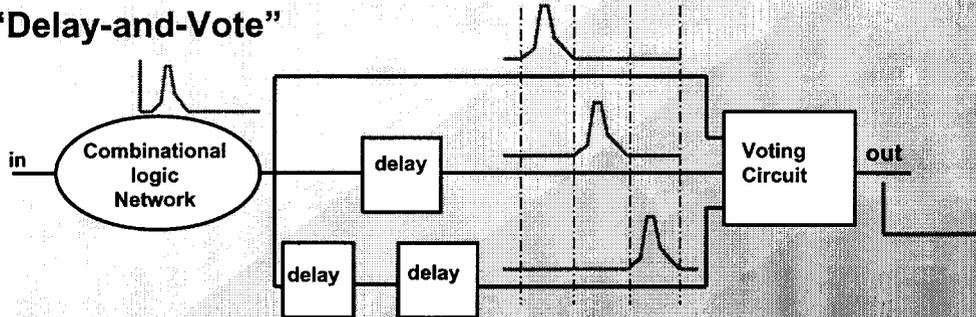
Figure 2 shows a Boeing approach to radiation temporal filtering and SEU reduction.



Temporal Filtering



“Delay-and-Vote”



Total Delay = 2 x Error Pulse Width ~ 2 x (Q_{COL} / I_{DRIVE})

if $I_{DRIVE} = 0.25 \text{ mA}$ and $Q_{COL} = 0.4 \text{ pC}$ then $2 \times (Q_{COL} / I_{DRIVE}) = 3.2 \text{ ns}$

- **Retargetability**

Architecture implementation.
Delay element redesign for
each process.

- **Scalability**

If Q_{COL} does not scale down with
 I_{DRIVE} , the required delay **increases**

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Figure 2. A Boeing Approach to SEU Reduction

Figure 3 shows a Boeing approach to spatial redundancy and SEU reduction.



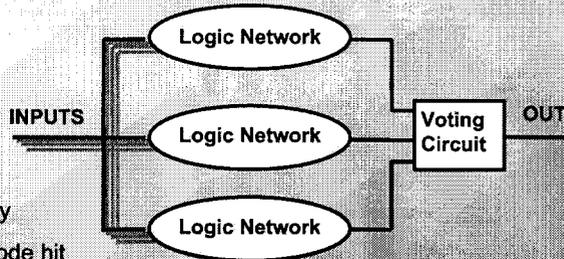
Spatial Redundancy - TMR



Triple Mode Redundancy (TMR)

Error on OUT requires simultaneous errors in 2 or more logic networks

- Does not increase LET threshold
- Does reduce effective cross-section by geometric probability of multiple node hit



$$X\text{-sec}_{EFF} \sim 1 / (\text{node separation})^2 \quad \sim 3X \text{ power and area penalty}$$

- **Retargetability**

Architecture implementation.
Modified structural netlists and/or cells

- **Scalability**

Adequate separation is critical

5/1/2002

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Figure 3. A Boeing Approach to Spatial Redundancy

In the past, charge collection spectroscopy has been used to determine minority carrier lifetime in Silicon On Insulator (SOI) and bulk devices. Comparisons of microbeam and broadbeam spectroscopy methods for determining minority carrier lifetime and radiation damage constants have also been studied. There remains a need for SOI microdosimeter designs to include methods to minimize lateral diffusion such as guard rings or other isolation boundaries. Such a device would provide an excellent test structure for experimental microdosimetry both in the realm of radiobiology and for SEU studies. In the latter category, an important application is the verification of neutron burst generation rate models central to SEU prediction software. Applications in radiobiology include the study of dosimetry in space and avionics. Unambiguous characterization of the sensitive volume and charge collection regimes requires the testing of such devices with a microbeam [Bradley].

The doses and dose rate levels behind 1 mm of aluminum shielding are given in Table 4, assuming a power-law dependence of E^{-3} in the integral spectra. These ionizing doses and Non Ionizing Energy Loss (NIEL) contributions to a mission's cumulative radiation exposure are less than other sources of radiation, and are not large enough to seriously impact the spacecraft design. For example, the NASA Solar Probe mission requires a flyby of Jupiter to take the spacecraft out of the ecliptic plane, during which it is estimated to receive 100 kilorad behind 1 mm of aluminum. The radioisotope power

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source is estimated to expose the electronics to the equivalent of 10^{11} 1-MeV neutrons/cm² in the course of the mission. These radiation levels are not trivial, but are within current spacecraft packaging design capabilities [Tsurutani]. Table 4 shows an industry estimate of maximum packaging radiation doses [Tsurutani]. SEE refers to Single Event Effect.

Table 4. Packaging Dose Rate Levels [Tsurutani]

Radiation Type	Maximum Dose Rate (rad Si s ⁻¹)	Maximum Dose/Event (rad-Si)
Protons	40.	4×10^4
Heavy Ions > 10 MeV/n ⁴ He + ³ He C + N + O Ne + Mg + Si Fe	~0. (SEE only)	~0. (SEE only)
Electrons	3.	3×10^3
Neutrons ≥ 1 MeV	~0. (NIEL only)	~0. (NIEL only)
Hard X-rays and γ-Rays with E > 50 keV	10^{-2}	1.

Figure 4 shows the most recent Goddard Space Flight Center (GSFC) Electronic Radiation Characterization (ERC) Project Roadmap [GSFC].

ERC Advanced Technology Roadmap

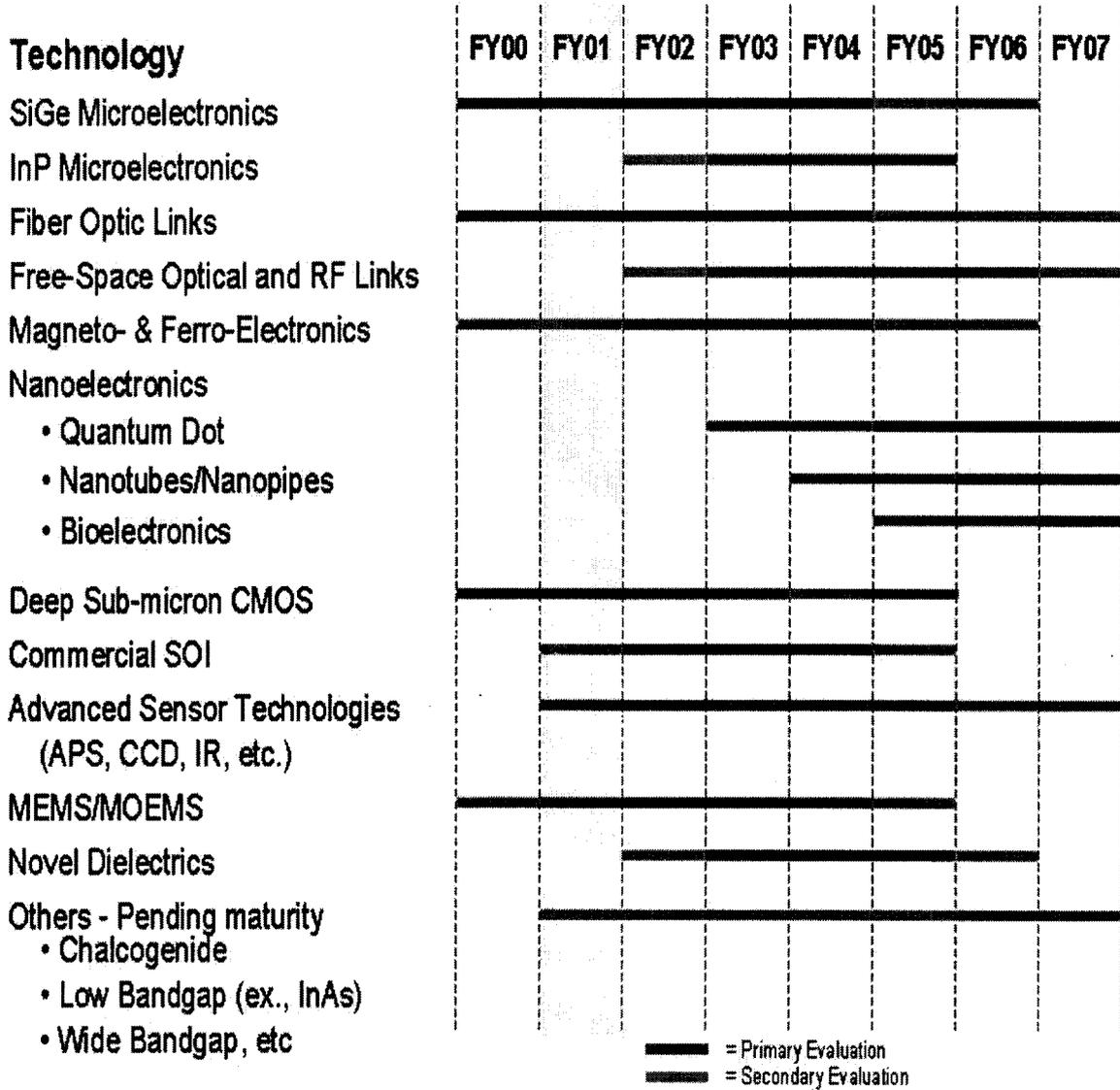


Figure 4. GSFC ERC Project Roadmap [GSFC]

RECOMMENDATIONS FOR FUTURE PACKAGING RESEARCH EMPHASIS

In general, a focus on materials evaluation and substrate related microelectronics issues will yield results which can be applied to the greatest variety of space electronics mission needs. A material issue not currently addressed is solder mask adhesion to encapsulants and conformal coating. A components research need is to study the reliability of UV LEDs. Another components research need is the evaluation of LTCC dielectric paste for extreme environments applications. SOI microdosimeter design is an area of radiation packaging characterization needing further research.

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