

# Automatic Evolution of Signal Separators Using Reconfigurable Hardware

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**Abstract.** In this paper we describe the hardware evolution of analog circuits performing signal separation tasks using JPL's Stand-Alone Board-Level Evolvable System (SABLES). SABLES integrates a Field Programmable Transistor Array chip (FPTA-2) and a Digital Signal Processor (DSP) implementing the Evolutionary Platform (EP). The FPTA-2 is a second generation reconfigurable mixed signal array chip whose cells can be programmed at the transistor level. Its chip architecture consists of an 8x8 matrix of reconfigurable cells. The FPTA-2 is reconfigured by evolution to achieve circuits that can extract a target signal that is combined with an undesired component or to perform the separation of a combination of two signals. The paper considers also an adaptive filter where the fitness function depends on the input signal. The results demonstrate that SABLES is not only able to perform signal separation and extraction, but it is also flexible enough to adapt to different input signals without human intervention, such as in the case of self-tuning and adaptive filters.

## 1 Introduction

This work describes the evolution of circuits that perform signal separation using the most recent version of the Field Programmable Transistor Array chip, the FPTA-2. Source or signal separation is a classic signal processing problem [1]: given  $N$  physically distinct measurements which represent a priori unknown linear combinations of  $N$  independent signal sources, the objective is to auto-adaptively extract  $N$  equivalent statistically independent signals, e.g., arising from independent physical sources. One approach to solve this problem is the H-J adaptive network, which is based on the modified Hebbian learning rule [2]. Cohen and Andreou [1] proposed a hardware implementation for a Neural Network implementing the H-J adaptive algorithm and tested it for the case of separating two sine waves (782Hz and 1kHz) applied at the network input, after being mixed. The interest in the signal separation problem is motivated by applications in communication systems, such as adaptive noise reduction and adaptive echo cancellation.

Particularly, our focus is to demonstrate the synthesis of circuits that can perform signal extraction and separation using the SABLES platform. This class of applications encompasses experiments in which the reconfigurable hardware evolves to a new configuration when the input signal characteristic changes, leading to potential applications

such as adaptive noise elimination. Additionally, this paper also describes an experiment accomplishing the separation of two source signals from a mixture of these signals given at the circuit input.

SABLES was used in the evolutionary experiments. This system solution provides autonomous, fast (about 1,000 circuit evaluations per second), on-chip circuit reconfiguration. Its main components are a JPL Field Programmable Transistor Array chip as transistor-level reconfigurable hardware, and a TI DSP implementing the evolutionary algorithm as the controller for reconfiguration.

This article is organized as follows. Section 2 describes the SABLES and the FPTA-2 chip. Section 3 describes the experiments, including the evolution of tunable filters excited by an "unknown" combination of source signals; and the evolution of a circuits performing signal separation. Section 4 summarizes the conclusions and future applications.

## 2 SABLES

SABLES integrates an FPTA and a DSP implementing the Evolutionary Platform (EP) as shown in Figure 1. The system is stand-alone and is connected to the PC only for the purpose of receiving specifications and communicating back the results of evolution for analysis [3].

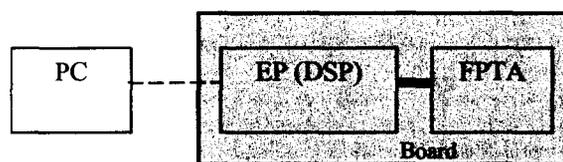


Fig. 1. Block diagram of a simple stand-alone evolvable system.

The FPTA is an implementation of an evolution-oriented reconfigurable architecture (EORA) [4]. The lack of evolution-oriented devices, in particular for analog, has been an important stumbling block for researchers attempting evolution in intrinsic mode (with evaluation directly in hardware). Extrinsic evolution (using simulated models) is slow and scales badly when performed accurately e.g. in SPICE, and less accurate models may lead to solutions that behave differently in hardware than in software simulations. The FPTA has transistor level reconfigurability, supports any arrangement of programming bits without danger of damage to the chip (as is the case with some commercial devices). Three generations of FPTA chips have been built and used in evolutionary experiments. The latest chip, FPTA-2, consists of an 8x8 array of reconfigurable cells. Each cell has a transistor array as well as a set of other programmable resources, including programmable resistors and static capacitors. Figure 2 provides a broad view of the chip architecture together with a detailed view of the reconfigurable transistor array cell. The reconfigurable circuitry consists of 14 transistors connected through 44 switches and is able to implement different building blocks for analog processing, such as two- and three-stage OpAmps, logarithmic photo detectors, or Gaussian computational circuits. It includes three capacitors, Cm1, Cm2 and Cc, of 100fF, 100fF and 5pF respectively. Details of the FPTA-2 can be found in [5]. Other implementations of reconfigurable analog devices can be found elsewhere [6-10].

The evolutionary algorithm was implemented in a DSP that directly controlled the FPTA-2, together forming a board-level evolvable system with fast internal communication

ensured by a 32-bit bus operating at 7.5MHz. Details of the EP were presented in [11]. Over four orders of magnitude speed-up of evolution was obtained on the FPTA-2 chip compared to SPICE simulations on a Pentium processor (this performance figure was obtained for a circuit with approximately 100 transistors; the speed-up advantage increases with the size of the circuit). The evaluation time depends on the tests performed on the circuit. Many of the evaluation tests performed required less than two milliseconds per individual, which for example on a population of 100 individuals running for 200 generations required only 20 seconds. The bottleneck is now related to the complexity of the circuit and its intrinsic response time. SABLES fits in a box 8" x 8" x 3".

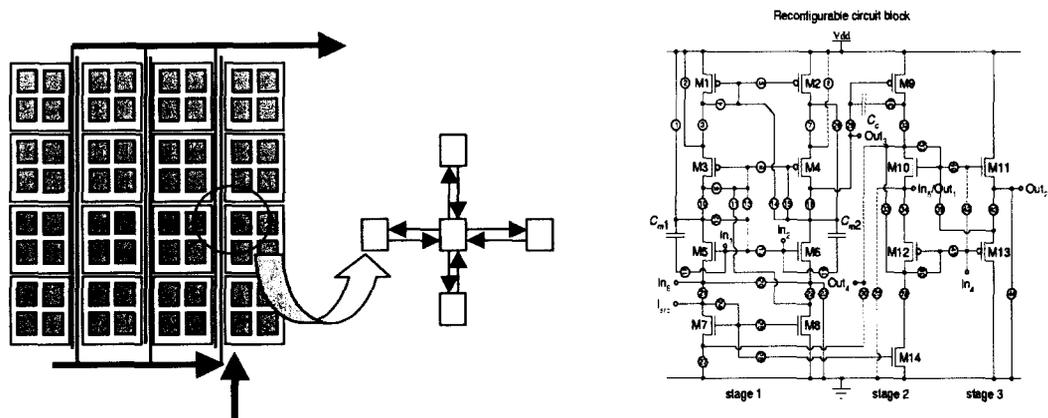


Fig. 2. FPTA 2 architecture in the left and schematic of cell transistor array (*re-configurable circuitry*) in the right. The cell contains additional capacitors and programmable resistors (not shown).

### 3 Experiments

The results for three different classes of experiments are presented in this section. The first two experiments demonstrate the evolution of circuits for signal extraction, while the last experiment shows the evolution of a circuit for signal separation. In the first case the evolving circuit is excited with combination of signal sources of known frequencies  $f_1$  and  $f_2$ , e.g., the known input frequencies are used by the fitness evaluation function. The objective is to amplify the signal at frequency  $f_1$  while attenuating the signal at frequency  $f_2$ . In the second case the circuit is excited with a combination of signal sources of *unknown* frequencies, e.g., knowledge of the input sine waves frequencies is not used by the fitness evaluation function. The objective of the experiment is to evolve a circuit that amplify the strongest component of the input signal and attenuate the weakest one, therefore improving a hypothetical signal/noise ratio. It is shown that when the frequency of the strong and/or weak component in the input signal changes, the circuit is reconfigured by evolution to "adapt" to the new input profile. Finally, in the third experiment evolution performs signal separation: the evolving circuit is excited with two linear combinations of pure sine waves (source signals) of known frequencies, and the circuit outputs are the original source signals.

Based on prior experimentation, the GA parameters selected for these experiments were: 70% mutation rate; 20% crossover rate; replacement factor of 20%; population of 400; and 100 to 200 generations. A binary representation was used, where each bit

determines the state (opened, closed) of a switch. Each execution took about 5 minutes in the SABLES system. More than 20 different GA executions were performed. In order to compute the fitness function, the FFT of the output signal(s) from the FPTA-2 was calculated. The fitness was a measure of the error of the FPTA-2 outputs to the target values in each experiment, as shown below.

$$Fitness = \sum_{i=1}^N |O_f(i) - T_f(i)| \quad (1)$$

where  $N$  is the number of samples used in the FFT (usually 64),  $O_f(i)$  is the magnitude of the  $i^{\text{th}}$  FFT component of the FPTA-2 output, and  $T_f(i)$  is the target magnitude of the  $i^{\text{th}}$  FFT component. Other fitness measures such as the sum of the squared deviations between the output and the target were tried, without significant improvement.

Referring to the input signals frequencies, they were restricted to values below 50kHz, because the data converters at SABLES operate at 100kHz sampling rate and due to bandwidth limitations of reconfigurable analog devices [10].

Another important feature of these experiments refers to the switches control voltages. The switches of the re-configurable chip are implemented as transmission gates. The control voltages that completely open or close the switches are 0 and 2V. However, through experimentation, it has been observed that the results significantly improve when the values 0.4V and 1.6V are used to control the switches, meaning that they are now partly opened and closed (partly closed if the higher and lower control voltages are respectively applied to the NMOS and PMOS transistors of the switch, and partly opened in the other case).

Finally, another important issue is the search space size. If we allow a completely unconstrained evolution, we will end up with a very large search space size. One approach to reduce the search space size is to have the FPTA-2 cells constrained to a particular topology, so that only the interconnections among the cells and the feedback resistance values [5] are evolved. Through experimentation, it has been verified that the constrained approach delivered better results. In the following experiments the cell topologies were fixed to the one of inverting amplifiers.

### 3.1 Combination of Known Signal Sources

To evolve the circuit we introduce an input signal consisting of a linear combination of 10kHz and 25kHz sine waves. The objective is to eliminate the 25kHz tone and amplify the 10kHz tone. Four cells of the FPTA-2 were used in this experiment. Figure 3 provides a high level schematic of the input/output interconnections in this experiment. Figure 4 depicts the FFT of the input signal and of the evolved circuit output. Figure 5 shows the evolved circuit response in the time domain, when excited by 10kHz and 25kHz tones respectively.

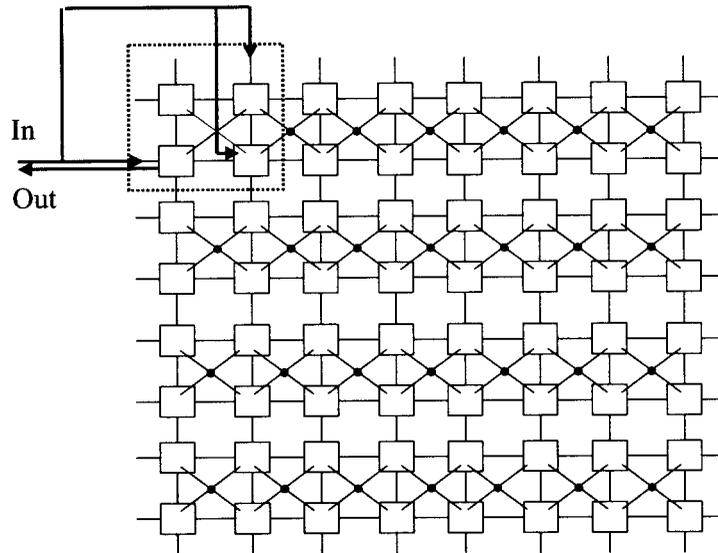


Fig. 3. Input (In)/Output(Out) connection in the signal extraction experiment. Only the four cells at the top-left of the array were used.

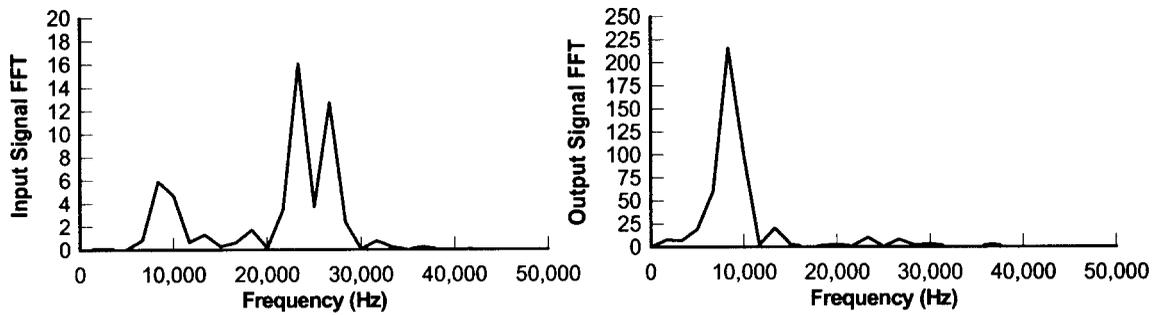


Fig. 4. Evolved circuit response in the frequency domain: FFT of the input (left); and output (right) signals.

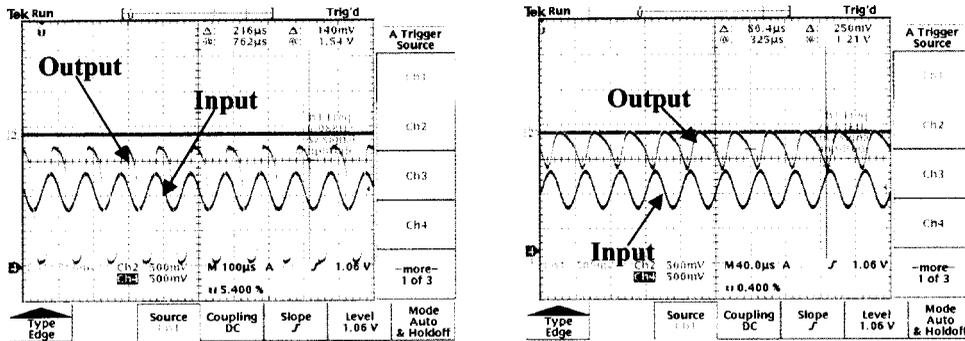


Fig. 5. Evolved circuit response in the time domain: when excited by a 10kHz input signal (left) and by a 25kHz input signal (right).

The evolved circuit displayed a 15dB gain at 10kHz and a 2dB attenuation at 25kHz.

Due to space limitation it is not possible to show in this paper the evolved circuits' schematics. The reader can refer to [12] to get the netlists of the evolved circuits.

### 3.2 Unknown Combination of Signal Sources

The linear combination of two source signals (10kHz and 20kHz) was applied to the FPTA-2 chip, as previously shown in Figure 3. Nevertheless, the source signals are unknown to the evolutionary system, in the sense that no information about the input signal is used by the fitness evaluation function. The fitness criteria employed here is to amplify the strongest tone at the input signal and attenuate the weakest one, which we *respectively* assume to be signal and noise. Four cells of the chip were used in the experiment. Figure 6 summarizes the performance of the evolved circuit. Initially, the 10kHz tone has about twice the amplitude of the 20kHz tone. The evolved circuit (C1) output increases the "signal/noise" ratio from 4.1dB to 16.9dB. In this case, the 10kHz tone is attenuated by 2.86dB, while the 20kHz tone is attenuated by 15.8dB. If we invert the source signal ratios, it is observed that a new circuit configuration, C2, is evolved: the "signal/noise" ratio increases from 10.8dB to 18.5dB. In this case, the 10kHz tone is attenuated by 12.5dB, while the 20kHz tone is attenuated by 4.8dB. It can be observed that the performance is better in the first case. Table 1 compares the results in terms of the achieved and target FFT values  $O_f$  and  $T_f$ .

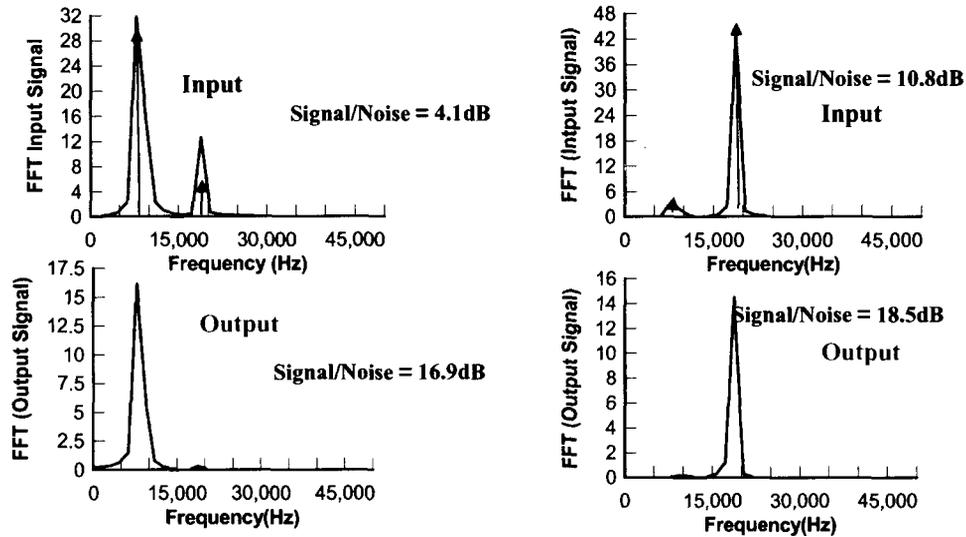


Fig. 6. In the left, FFT of the input (top) and output (bottom) of circuit C1 when the 10kHz tone has twice the amplitude of the 20kHz tone. In the right, the same information is shown for circuit C2, when the 20kHz tone has a higher amplitude.

**Table 1:** Comparison between the target and the attained FFT for the two circuits presented in this section: circuit 1 (passing 10kHz ) and circuit2 (passing 20kHz).

	Wanted tone		Unwanted tone	
	Output( $O_f$ )	Target ( $T_f$ )	Output ( $O_f$ )	Target ( $T_f$ )
<b>Circuit 1</b>	16.1	> 20	0.33	0
<b>Circuit 2</b>	14.5	> 20	0.21	0

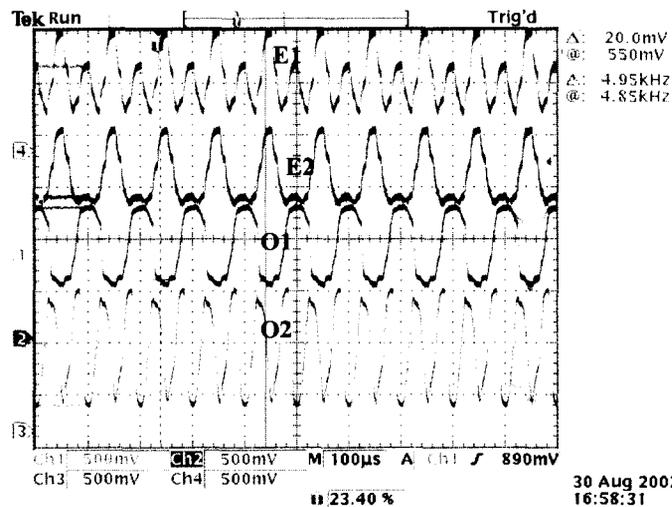
### 3.3 - Signal Separation Experiments

The goal of this experiment is to design a circuit able to separate two mixed signals,  $E_1(t)$  and  $E_2(t)$ , obtained by the linear combinations of pure sine waves,  $e_1(t)$  and  $e_2(t)$ , of known frequencies. The circuit outputs are the original pure sine waves. As in the previous case studies, we chose for the frequency of the pure sine wave  $e_1(t)$ ,  $f_1 = 10\text{kHz}$  and for the pure sine wave  $e_2(t)$ ,  $f_2 = 20\text{kHz}$ . These signals were linearly combined by a mixing matrix to produce the chip inputs  $E_1(t)$  and  $E_2(t)$ :

$$\begin{bmatrix} E_1(t) \\ E_2(t) \end{bmatrix} = \begin{bmatrix} 0.25 & 0.5 \\ 0.5 & 0.25 \end{bmatrix} \begin{bmatrix} \sin(2\pi 10,000t) \\ \sin(2\pi 20,000t) \end{bmatrix}$$

The set of experiments was performed using 10 cells of the FPTA-2. Following the same procedure of the previous experiments, the cells were constrained to be inverting amplifiers reducing thereby the search space.

Figure 7 depicts the inputs and outputs of the best circuit achieved in this set of executions.



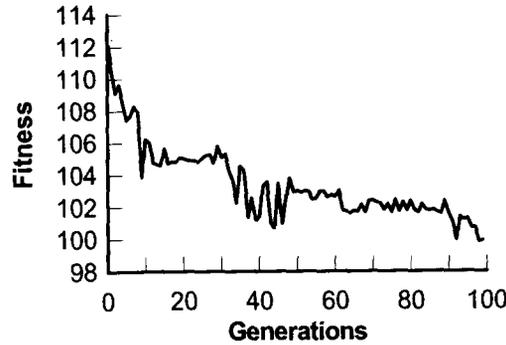
**Fig. 7.** Result of the signal separation experiment. At the top the inputs  $E_1$  and  $E_2$  are shown. At the bottom the outputs  $O_1$  (10kHz) and  $O_2$  (20kHz) are shown.

Table 2 summarizes the evolved circuit performance in terms of the FFT and of the values measured in the frequency analyzer. The target FFT values used in the fitness function are also included in the table.

**Table 2:** Evolved circuits in the signal separation experiment. Amplitude of 10kHz and 20kHz tones as measured by the spectrum analyzer and calculated by an FFT algorithm used during evolution.

	10kHz Tone		20kHz Tone	
	FFT	Spectrum Analyzer	FFT	Spectrum Analyzer
Input $E_1$	33.6	-13dB	8.86	-20dB
Input $E_2$	7.6	-20dB	41.1	-15dB
Output $O_1$	36.9 (Target: $T_f > 20$ )	-13dB	1.07 (Target: $T_f = 0$ )	-35.3dB
Output $O_2$	0.6 (Target: $T_f = 0$ )	-30dB	84.5 (Target: $T_f > 20$ )	-13dB

From Table 2, it can be observed that the output  $O_1$  attenuates the component  $e_2$  (20kHz) by -15dB (from -20dB to -35.3dB), while keeping  $e_1$  (10kHz) at the same level. On the other hand, the output  $O_2$  attenuates the component  $e_1$  by -10dB (from -20dB to -30dB), and amplifies  $e_2$  by 2dB (from -15dB to -13dB). Finally Figure 8 plots the fitness of the best individual along the generations averaged over 3 GA runs. It can be observed from this graph that the fitness does not go to 0 for the best individuals. This is an expected systematic constant due to the way the fitness function was written – the minimum possible fitness in this experiment is 80.



**Fig. 8:** Fitness against generations for the signal separation experiment.

This experiment is a first approach to tackle the independent component analyzer problem, which consists of recovering the original source signals from signals acquired from a set of sensors that pick up different linear combinations of source signals.

#### 4. Discussion and Conclusions

Most of the experimental results could be conventionally implemented using low or high pass filters with zeros/poles in the range of 10-20kHz and a control or adaptation block. Supposing  $R=10K$ , a value that is in the range of the polysilicon on-chip resistances [4], we would then be talking about  $0.1\mu$  capacitors. In order to implement a capacitor of this size using the chip fabrication process (about  $1\text{fF}/\mu\text{m}^2$  for metallic capacitors), a silicon area of  $100\text{mm}^2$  would be used, against only about  $2\text{mm}^2$  used by the evolved circuits.

Several factors explain this discrepancy: the resistive effect of the switches contributes to increase the RC constant; to a small extent the exploration of parasitic capacitors of the MOS transistor; and the capacitances of the probing instruments (10p for the oscilloscopes). By cascading the filters evolved using a small number of cells, the FPTA-2 chip will be able to realize steeper frequency responses (possibly with roll-off superior to 60dB/dec).

It has also been demonstrated that the reconfigurable hardware can evolve to “adapt” to changes in the input signal. The task of separating a mixed sine wave input (with frequencies unknown a priori) has been approached using a 2x2 neuromorphic analog network implemented in VLSI using a total of 76 transistors [1]. The network training time was 80ms and they were able to separate the two sine waves by 15dB (worst) to 35dB (best). The evolved FPTA-2 hardware used 140 fixed transistors, taking a training time of the order of seconds and separating the sine waves by 17dB (worst) to 22dB (best). In the case of Evolvable Hardware, we point out that the reconfigurable chip was not specifically designed for the signal separation task, as it happens in the neuromorphic approach.

The results demonstrate that our evolutionary platform can perform signal separation and extraction for input signals consisting of a combination of sine waves, being also capable to adapt to different input signals without human intervention. Future applications will consist of the separation of more complex signals, such as mixed speech signals.

Among the lessons learned from the experiments reported in this paper, we emphasize the advantages of using partly opened/closed switches; and constraining the reconfigurable circuitry [4] to a particular topology. Future work will focus in extending these experiments to evolve filters with more stringent requirements; tackle more realistic case of adaptive noise cancellation; and tackle the problem of separating mixed speech signals.

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