SIP QUALIFICATION AND PRA APPROACHES

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ABSTRACT

System in a package (SIP) development is a response to an increasing demand for integration of different functions into one unit to reduce size and cost and improve functionality. Qualification of the newly developed multifunctional electronics are becoming complex at the package level and even more at the second and system levels. Even for one die package, after many years of data collection, just recently industry came to agreement in releasing an industry-wide specification.

Probability risk assessment (PRA) implemented by NASA for spaceflight missions from the risk point of view may be narrowed at the element level for the advanced electronic systems and SIP and to electronic subsystem level. This paper will review the key elements of an industry-wide specification recently published by IPC. It will report on a few other unique qualification approaches that are currently being implemented or developed for risk reduction in high reliability applications. Risk level assessment based 2-P, 3-P, and LogNormal distributions will be compared for plastic ball grid array (PBGA) and flip chip BGA (FCBGA). Cycles-to-failures (CTFs) test results for temperature ranges of –30 to 100°C and 0 to 100°C (two profiles) are compared. Finally, it will review finite element analyses performed for optimization of unique silicon base SIP package assembly with five chips on a microboard. Qualification approach for level and level 2 of this SIP will also presented.

Key words: Probability Risk Assessment, Weibull, LogNormal, ball grid array, BGA, FCBGA, IPC9701, solder joint reliability, Systems-in-a-package, SIP

INTRODUCTION

BGAs and CSPs are now widely used for many electronic applications including portable and telecommunication products. System in a package (SIP) development is the most recent response to further increasing demand for integration of different functions into one unit to reduce size and cost and improve functionality.

The BGA version now started to be implemented for high reliability applications with more unique requirements. The BGA version of area array package introduced in late '80's and implemented with great caution in early '90's was further evolved in mid '90's to CSP with much finer pitch. Now distinguishing between size and pitches become difficult for the array versions. These are now categorized as area array packages in order to be able to distinguish them from the flip chip bare die category. The bare dies have been around for a longer time, but their associated issues including known good die and difficulty in direct attachment to printed wiring board (PWB) have limited their wide implementation.

CSP definition has evolved as the technology has matured and refers to a package with 0.8 mm pitch and lower, now as low as 0.4 mm pitch. Packages with fine pitches, especially those with less than 0.8 mm, and high I/Os may require the use of microvia PWB which is costly and they may perform poorly when they are assembled onto boards. Extensive work has been performed by the JPL consortia in understanding technology implementation and reliability issues from BGA to CSPs. Lessons learned by the team have been continuously published and presented in previous SMTAI conferences [1-2]. A Book recently published also include chapters related to this subject[3-5].

Recent approaches have been to increase functionality through systems-in-package, i.e., stacking die/package in the height in order to avoid reducing the pitch. This approach will ease stringent board and assembly requirements. The first SIP using chip scale package included two stacks of flash and SRAM die into a single package. Also known as multi chip package (MCP) now recently released in four die may include two flash memories, a fast-cycle-RAM (FCRAM), and an SRAM. There are many unique packages including one that uses silicon-based SIP was developed using discrete flip chip dice attached to a microboard with area array configuration.

This paper will give examples of qualification approaches for advanced electronic packages especially a silicon based SIP. Cycle-to-failure (CTF) test data for BGA and FCBGA assemblies will be compared for a defined risk level using Weibull and LogNormal distributions

QUALIFICATION SPECIFICATION

An industry-wide guideline document, IPC SM785, for accelerated reliability test of solder attachment has been around for more than a decade. Only recently, industry came to agreement to release an industry-wide specification, IPC9701, in response to BGA and CSP technology

implementation[6]. The SM785 guideline, even though very valuable and still valid, did not provide an answer to the key question as what the data means in terms of product application and data comparison. As it well established by industry and JPL Consortia [1-5], many variables could be manipulated in order to show favor or disfavor test results. In addition, in some cases, considerable resource and time could have placed to generate failure data not related to solder attachment. Examples include the use of surface finish with a potential of inducing intermetallic rather joint failure, especially for a novice user/supplier.

The IPC 9701 Specification, addresses the solder joint reliability due to thermal expansion mismatch between the package and PWB. In order to be able to compare solder joint reliability of package technologies, PWB materials (FR-4), using a relatively thick nominal control thickness to minimize bending (0.093"), surface finish choice to eliminate intermetallic failure (OSP, HASL), Pad configuration to eliminate failure due to stress riser (non solder mask defined), and pad size to have a realistic failure opportunity for package/PWB (80%-100 package pad), etc. were standardized in order to minimize their effect on the test results.

Since the release of this document in early 2002, there has been questions regarding as why other variables including use of immersion Au/Ni surface finish, a realistic production finish for many product applications is not allowed in this specification. Potential technical issues associated with the use of such variables were the key elements that team decided not to include them in specification. It should be noted, however, that package supplier/user can evaluate this surface finish or others as become available or any other variables, as long as deviations from the specification are clearly stated.

The thermal cycle (TC) test ranges, test profile, and the number of cycles (NTC) reported were also standardized and are listed in Table 1. These include the reference cycle in the range of 0 to 100° C (TC1) to a sever military cycle condition of –55 to 125°C (TC4). Three out of five total TC conditions are identical to the test conditions recommended by JEDEC 22 Method A104, Revision A. The NTC varied from a minimum value of 200 cycles to a reference value of 6,000 cycles.

IPC committee is currently working on a follow on specification to include performance test methods and requirements for mechanical damage. Currently, there is no standard requirements for this types failures including including bend test and dynamic loading during functionality test or due to load application.

Table 1 Temperature cycling requirements specified in Table 4.1 of IPC 9701

Test Condition	Mandated Condition
Temperature Cycle (TC) Condition: ***TC1***	***0°C ↔ +100°C (Preferred Reference)***
TC2	–25°C ↔ +100°C
TC3	–40°C ↔ +125°C
TC4	–55°C ↔ +125°C
TC 5	-55 °C<-> 100°C
Test Duration	Whichever condition occurs FIRST: 50% ***(preferred 63.2%)*** cumulative failure (Preferred Reference Test Duration) or
Number of Thermal Cycle (NTC) Requirement: NTC-A	200 cycles
NTC-B	500 cycles
NTC-C	1,000 cycles (Preferred for TC2, TC3,and TC4)
NTC-D	3,000 cycles
NTC-E	***6,000 cycles (Preferred Reference TC1)***
Low Temperature Dwell	10 minutes
Temp. tolerance (preferred)	+0/–10°C (+0/–5°C) [+0/–18°F (+0/–9°F)]
High Temperature Dwell	10 minutes
Temp. tolerance (preferred)	+10/–0°C (+5/–0°C) [+18/–0°F(+9/–0°F)]

CURRENT APPROACH ON ELECTRONIC QUALIFICTION FOR SPACE MISSIONS

NASA has established a standard thermal cycle requirement under NASA Handbook, NHB 5300.4, "Requirements for Soldered Electrical Connections". The IPC 9701 includes the 3A-1 version requirement under TC5 (-55/100°C) and NTC-A (200 cycles). The only difference is the long dwell time requirement of 45 minutes (3 A-1 Rev) whereas the dwell for the IPC is 10 minutes. The subsequent revision does not define a specific cycle or temperature range and emphasis has been placed on meeting the mission requirement by doing the right qualification test. JPL develops a life cycle requirement based on the mission application and uses the 200 cycles as baseline.

For the 2003 Mars mission (Mars Exploration Rover, MER), a team was formed to address systematically the issues of package qualification for package, PWB, and assembly, and inspection. The PQV team (package qualification and verification) identified issues associated with design, new packages, PWB, and manufacturing. Qualification tests were performed for electronic packages as needed to meet the specific spacecraft module environmental requirements, thereby, enable to define risk and develop risk mitigation approaches. In addition to vibration, landing load, etc, the temperature cycle requirement was the three times of equivalent thermal cycles for ground and flight exposures. The effect of local package heat dissipation was included in calculation using the case temperature rise. In most cases, this effect was carried out during qualification test by turning power on at the end of cold dwell time and power off at the end of hot dwell cycle.

PRA for Complex NASA's Mission Success

Probabilistic Risk Assessment (PRA) is a comprehensive, structured, and logical analysis method for complex risk evaluation[7]. The method is aimed at identifying and assessing risks in complex technological systems for the purpose of cost-effectively improving their safety and performance. PRA has been widely developed and expanded by the nuclear industry to assess safety. Since its inception, the analytical method has gradually improved and expanded by experts in the field and has gained credibility over the past two decades in other industries as well.

Because of its logical, systematic, and comprehensive approach, PRA has repeatedly proven capable of uncovering design and operation weaknesses that had escaped even some of the best deterministic safety and engineering approaches. This methodology showed that it was very important to examine not only low-probability and high-severity mishap scenarios, but also scenarios involving strings of high-probability and low-severity, nearly benign, mishaps. Contrary to common perception, the latter with a high probability of occurrence is oftentimes more detrimental to safety than the former.

NASA has relied on many analyses including the Failure Modes and Effects Analysis (FMEA) method for system safety assessments. To date, FMEA continues to be required by NASA in all its safety related projects. Under Office of Safety and Mission Assurance (OSMA), a team of experts exists with PRA implementation experience. NASA's objective is to rapidly become a leader in PRA and to use this methodology effectively to ensure mission and programmatic success, and to achieve and maintain high safety standards at NASA. NASA intends to use PRA in all of its programs and projects to support optimal management decision for the improvement of safety and program performance.

Risk Reduction Tool Developed by JPL

At JPL, a software tool for risk analyses has been developed and implemented to achieve life-cycle risk management[8]. The defect, detection, and prevention (DDP) software is a process and tool for assessing risk, and planning the mitigation of risk. DDP handles the concepts of requirements, risks, and mitigations, and their interrelationships. Implementation of the DDP process is carried out by a mass of expertise, project team and a few specialists, by capturing trees of requirements and potential failure modes. Failure mode in a general sense defined as inability to achieve the requirements.

Scoring the impacts of these failures on requirements results in a prioritized set of PACTs (preventive measures, analyses, process controls and tests each of which has an effectiveness versus failure modes. A resource cost (dollars, schedule, mass) is associated with each PACT. It is the goal of the DDP process to optimally select the subset of the PACTs that minimize the residual risk subjected to the project resources. This technique has been applied at various levels of assembly including the system and subsystem levels, as well as down to component level.

The output of the DDP process will only be as thorough as the available information and the breadth of the involved expert. The level of evaluation fidelity will be as good as the level information detail. At higher level of evaluation, the scoring will be primarily based on engineering judgement and corporate knowledge bases, i.e a qualitative approach. At the lower levels of evaluation, more detailed information may be available (testing and modeling results, etc) and scoring could be more accurate.

The DDP is not based on a scientific risk analyses such as PRA and especially at higher level, scoring done mostly based on judgement, a gross qualitative value assignment. In addition, for a typical matrix of requirements, failure modes, and PACTS, a large number of interrelationships among these variables need to be scored. This is extremely time consuming and cumbersome, especially when many cells in matrix are not significant and are repetitive.

Virtual qualification approach based on PRA may answer the scientific risk level not defined by this tool, especially

when details analyses are considered. The approach proposed by the prinicpal author concentrates on key failure modes and prevention using statistical distributions, enabling the quantitative acceptable risk. The first element of this qualification approach is to compare risk level calculated for the same data set fitted by different statistical distributions.

Virtual Qualification a PRA Approach

A physics of failure based approach to virtual qualification of advanced area array assemblies, against solder fatigue failure was reported previously[9]. The approach applies Monte Carlo Simulation to evaluate solder joint fatigue life distributions, given material property variations and manufacturing capabilities. Results were analysed using a simple model for inclusion of manufacturing variables. Simulation of product life distributions for virtual qualification, can be a valuable tool to evaluate and qualify design options.

Risk modeling aspect, a backbone of a typical PRA, can be developed using and extending this approach. Statistical distribution due to ground and flight thermal cycle exposures shall be considered in conjunction with distributions of package/assembly failures by simulation and test data. Other variables that significantly affect the risk are the extrapolation of failure data generated under accelerated testing for applications using relationship such as Coffin-Manson for electronic package/PWB/Assembly.

Risk Level Dependency on Distribution

Often, 2- and 3-parameter Weibull distributions have been used to characterize failure distributions and provide modeling for prediction in the areas of interest[10]. The Weibull cumulative failure distribution was used to fit cycles to failure data. The equation is

$$F(N) = 1 - \exp\left(-(N - N_1)/(N_o)^m\right)$$

where
F(N) is the cumulative failure distribution function
N is the number of thermal cycles
N_o is a scale parameter that commonly is referred to as characteristic life, and is the number of thermal cycles with a 63.2% failure occurrence.
N_1 is the failure free cycles for 3-parameter Weibull
The m is the shape parameter and for a large m is approximately inversely proportional to the coefficient of variation (CV) by 1.2/CV; that is, as m increases, the spread in cycles to failure decreases

This equation, in double logarithm format, results in a straight line for two Weibull parameters. The slope of the line will define the Weibull shape parameter. For the 3-P Weibull, CTFs for early failure cycles, deviate from the fitted line and data generally tend to concave downward. The pronounce curvature generally indicates that there is a failure free period (N_1) before wearout take effect. This implies that the 3-P Weibull distribution should be fitted to this type of data to calculate the failure free cycles (N_1).

Another distribution is LogNormal that is versatile distribution as it has a range of shapes, and therefore is often a better fit to CTFs data than its normal distribution version. It is called LogNormal since it uses logarithm of variable (here logarithm of cycles) rather than cycles for its normal distribution. Similar to Weibull distribution, this distribution does not extend below zero to negative infinity , whereas its normal distribution includes such a meaningless failure attributes for CTFs.

Risk Levels for 2-P and 3-P Weibull for BGA Assemlies

Table 2 lists both 2-P and 3-P Weibull parameters for two CTFs data sets generated for two types of plastic ball grid array (PBGA) assemblies [5,9]. CTFs are for the PBGA 313 I/Os and PBGA119 I/Os with a full array population. The temperature cycle for the 313 I/O assemblies were from –30 to 100°C (condition A) with ramp rates of 5°C/min and dwells of about 20 minutes. The cycling temperature range for the PBGA 119 I/O assemblies was narrower and ranged from 0 to 100°C (condition B) with 10 and 5 minutes of ramp and dwell times, respectively. In addition to Weibull parameters (e.g., m and N_o,), the risk levels for 0.01, 0.05, and 0.1 accumulated failures are also listed in the table.

Several observations can be made from the CTFs and risk levels are demonstrated below

- The Weibull m parameter is 21 and varied between 3 to 7 for test results under condition A and B, respectively, The higher value of m indicates a narrower CTF distribution for A condition.
- As expected, N_o and N_{mean} values are higher for condition B, a narrower temperature range and shorter cycle compare to A condition. Projection based on using Coffin-Manson relationship also resulted in a lower lower value than the test results. Package size (313 vs 119 I/Os) and shorter cycle for B partly contribute to this difference.
- The risk values for test data under condition A were only slightly changed when 2-P and 3-P Weibull distributions are used. The m and N_o values for the two are approximately the same since the failure free cycles was negligible (44 cycles for N_1 vs 4,000 cycles for N_o). This means that early CTFs did not deviate from the linearity of CTFs.
- The risk levels and m were different when 2- and 3-P Weibull distribution were fitted for the CTFs data set generated under B condition. In this case, for the same risk level, the 3-P Weibull showed higher acceptable CTFs. This is less conservative than its 2-P version.

Risk Levels for 2-P Weibull and LogNormal for PBGA and FCBGA Assemlies

Table 3 lists the 2-P Weibull and LogNorma parameters for CTFs under conditions A, B, and C for two PBGAs data sets reported in Table 2 and flip chip BGA (FCBGA) assembly failure data reported in literature[11]. The FCBGA was fully populated and had 1849 I/Os. Even though the

temperature cycle for this case (condition C) was the same as condition B, the dwell and rates were slightly different. For this condition, ramp rate and dwells were 10°C/min and 10 minutes, respectively. Using parameters given for Weibull and LogNormal distribution in literature, risk levels for 0.01, 0.05, and 0.1 were calculated and listed in the Table.

A few key points from the Table are:

- The N_o for the FCBGA1849 I/O is about 70% of PBGA 313 I/O, when adjusted for delta T using Coffin-Manson relationship, and 40% of PBGA 119. As expected, the larger I/O package has lower reliability.
- For all three types of distributions, the acceptable CTFs increased when the risk requirement level increased.
- The acceptable CTFs for an identical risk level were slightly different for 2-P and LogNormal for the A condition data set. Differences increased for B and C condition data sets.
- In all cases, the CTFs for a risk level, are much higher when LogNormal rather than Weibull distribution is used. Risk projection for failures based on the LogNormal distribution was the least conservative.

Table 2 Comparison of 2- and 3- parameter Weibull distritutions for two PBGA package assemblies for two thermal cycle ranges

Weibull Parameters	2 P Weibull (A, -30/100°C)	3 P Weibull (A, -30/100°C)	2 P Weibull (B, 0/100°C)	3 P Weibull (B, 0/100°C)
m	21.4	21.17	6.88	2.87
N_o	4104	4001	12215	5443
N_1	N/A	44	N/A	6576
N_{mean}	4000	4000	11420	11420
1%	3310	3310	6260	7674
5%	3572	3572	7932	8512
10%	3694	3694	8808	9062
Package	PBGA 313	PBGA 313	PBGA119	PBGA119
Sample size	13	13	27	27

Table 3 Comparison of 2-parameter Weibull and LogNormal distribution for PBGA and flipchip BGA assemblies

Weibull LogNormal Parameters	2 P Weibull (A, -30/100°C)	LogNormal (A, -30/100°C)	2 P Weibull (B, 0/100°C)	LogNormal (B, 0/100°C)	2-P Weibull (C, 0/100°C)	LogNormal (C, 0/100°C)
m	21.4	NA	6.88	NA	9.77	NA
N_o	4104	NA	12215	NA	4956	NA
N_{mean}	4000	4000	11420	11420	4710	4689
Sigma (σ)	NA	0.062	NA	0.17	NA	0.112
Mu (μ)	NA	8.29	NA	9.33	NA	8.45
1%	3310	3455	6260	7592	3095	3610
5%	3572	3604	7932	8522	3657	3900
10%	3694	3686	8808	9064	3936	4060
Package Type	PBGA 313	PBGA 313	PBA119	PBGA 119	FCBGA 1849	FCBGA 1849
Sample size	13	13	27	27	18	18

SIP FOR A UNIQUE SI BASE PACKAGE

A unique commercial systems-in-a-package package was developed and reported[12]. For this package, the substrate is attached to the PWB using an area array packaging approach that provides a very low inductance path from the PWB to the ICs, while also improving heat dissipation (see Figure 1).

This technology involves copper interconnect definition by lithographic techniques on silicon wafers. This approach offers very high routing resources with high speed, low noise 50Ω signal paths. Additionally, solder bump technology provides ultra-low (pH) inductance. Eliminating package overhead allows ICs to be placed closer together, further reducing chip-to-chip bus capacitance, which reduces power wasted in charging the bus (CV^2f_{data}, where f_{data} is typically one-fourth the clock frequency). Alternatively, lower bus power can be traded against higher bus frequency to improve performance at a fixed power level.

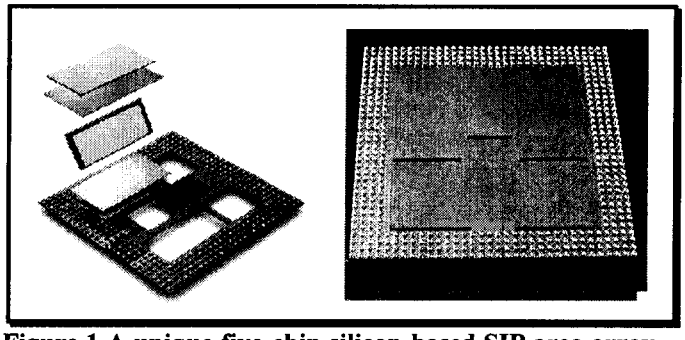

Figure 1 A unique five-chip silicon-based SIP area array configuration

As discussed previously, the integrity of bump at IC level and ball joints at PWB is a major reliability concern for advanced electronic packages and become more critical for SIP. Temperature fluctuations caused by either power transients or environmental changes, along with the resulting thermal expansion mismatch between the five IC chips, package materials, and board result in time- and temperature-dependent creep deformation of solder bump/ball joints in Si-based SIP assembly. This deformation accumulates with repeated cycling and ultimately causes solder joint cracking and interconnect failures depending on the weakest IC or board interconnects. To minimize development costs and maximize reliability performance of the SIP, advanced analysis was performed during the design and development phase of to determine analytically the weakest joints and to modify design as required.

Analyses were performed for a peripheral array SIP that had 697 solder balls in 40mm by 40mm dimension microboard as shown in Figure 2.

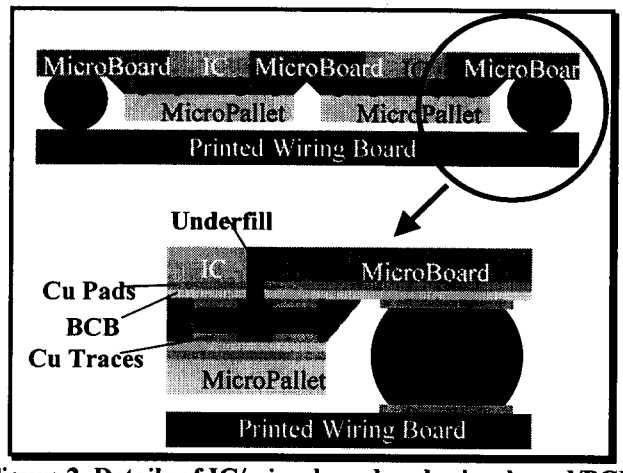

Figure 2 Details of IC/microboard and microboard/PCB attachment configuration for the silicon-based SIP

The basic structure of the Si-base SIP consists of a "microboard" with etched drop-in through-holes for the ICs. Each IC is partnered with a corresponding "micropallet" that provides connection continuity to the microboard where signals are routed between ICs using copper traces. The IC/micropallet and micropallet/microboard solder bump joints are secured using standard underfill material. Interconnection to PWB is carried out by the large area array solder balls. A benzocyclobutene (BCB) interlayer redistribute thermal stress mismatch due to silicon, solder bump, microboard and solder balls. Two types of interconnections for bump and balls were considered. Analyses were performed for eutectic (63Pb/37Sn) and a high temperature solder (90Pb/10Sn) for both bump and solder balls either using ball (configuration 1) or solid interconnect (configuration 2).

Base on the amount of plastic damage per cycle,, the weakest solder interconnection was found to be for one of the five IC bump interconnect, i.e. MPU, at the microboard/ micropallet interface. Slight improvement could be achieved by the use of a bump joint with 90/10 composition and increase of bump diameter. The CTFs were calculated from damage accumulation for a temperature cycle in the range of 0°C to 100°C (5 minute ramp and dwell). The CTFs for the 90/10 solder solid interconnects both at the IC and PWB interconnects (both configuration 2, i.e. Ball 2/Bump2), with CTFs of more than 38,000 cycles for the ball/PWB interconnects. The lowest CTFs was found to be for the Ball 1/Bump2, i.e. 90/10 solder ball to PWB interconnect and 90/10 solid interconnects (micropallet/microboard), for the MPU IC through the thickness at the bump/microboard interface. The CTFs was only 369 cycles.

This example clearly shows that even for a two design joint configurations, there are at least 72 interfaces (2 configurations x 6 chips x 3 interconnects x 2 interfaces) are required to considered in optimization. This will become even more complex if design for all materials, bumps, and balls are to be included in the optimization process

development. The complexity of design will transfer to user during qualification especially for high reliability application with a very low level of acceptable risk requirement. Innovative qualification approaches need to be developed to identify the weakest points of design with limited resources.

SIP Qualification at Level 1 and Level 2

Figure 3, Table 4, and Table 5 provide details information on qualifications steps for production implementation of the Si-based SIP. It includes a large number of tests that are required to be performed both at level 1 and level 2 prior to its wider acceptance. This comprehensive and costly qualification requirements after optimization by sophisticated modeling techniques, clearly demonstrates design complexity of SIP packaging technology and necessitate the development of innovative qualification approaches in this area. An acceptable industry-wide standard development in this area would reduce cost and ease data comparison for wider product applications.

CONCLUSIONS

As electronic packages become more miniature and complex, sophisticated modeling along with tests as well as development of probability risk assessment associated with failures may be required to be developed for their effective implementation. Based on the examples discussed for risk assessment of PBGA and FCBGA and modeling for a SIP, the following points are revealed:

- Risk projections based on 2- and 3-P Weibull distributions were the same for one sets of PBGA CTF data whereas differ for the other sets. Applicability of 3-parameter should always be evaluated.
- Risk projections for PBGA and FCPBGA based on the LogNormal in comparison to 2- and 3-P Weiblull were resulted in CTFs that were the least conservative, i.e., LogNormal CTFs were the highest for the same acceptable risk level.
- The theoretical example for optimization of a Si-based SIP reveled that a large number of interconnect sites compete for failures needed to be addressed. For this design, the weakest interconnection site was at the first level, i.e, IC to microboard, not at the second level of microboard to PWB interconnections.

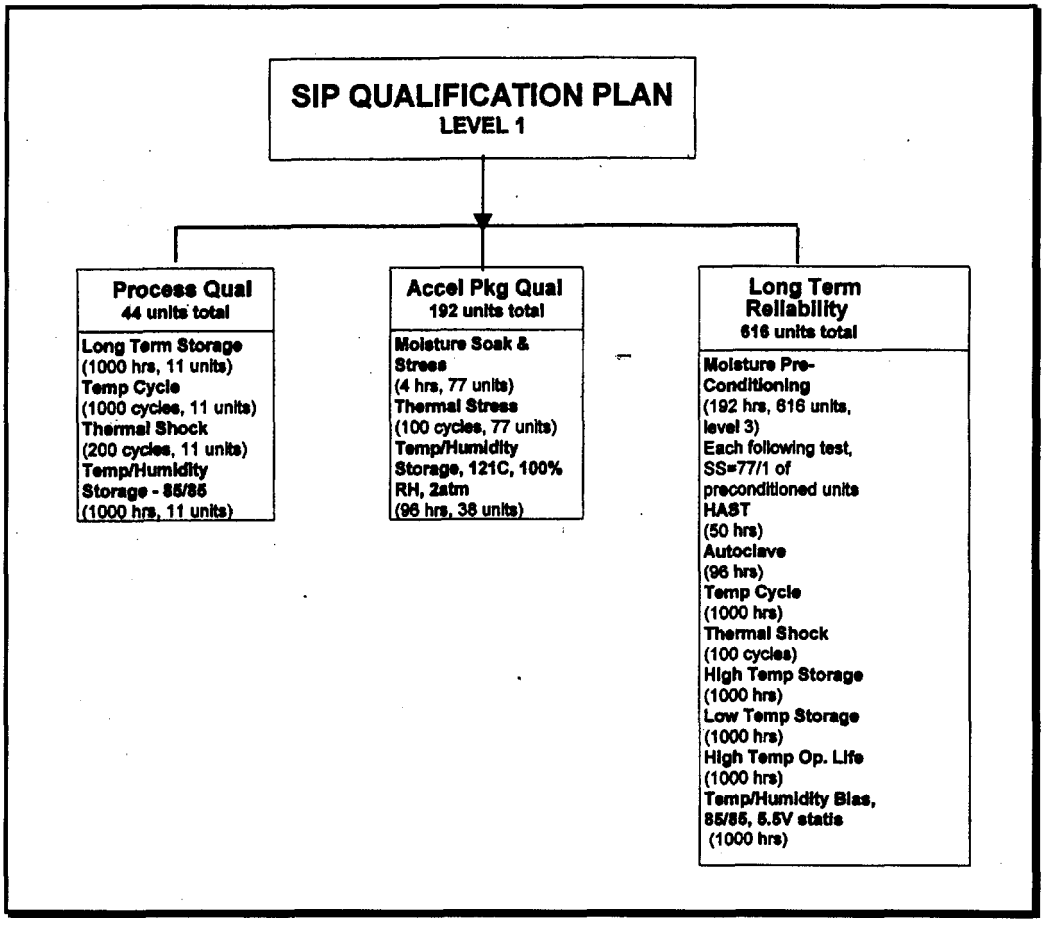

Figure 1 An example of level 1environmental qualification approach for a SIP

Table 4 An example of level 1, package, qualification test for a SIP

SiP Level 1 Tests	Standard	In	Out	Rejects
High temp Storage	150C 1000 hrs	11	11	0
Mechanical Stress Tests				
Mechanical Shock	JESD22-B104	11	11	0
Vibration	JESD22-B103	11	11	0
Constant Acceleration	MIL-STD 883D, Method 2001, Cond. B	11	11	0
Moisture Pre Conditioning Level 3	EIA/J-STD-020	55	55	0
Pressure Cooker Autoclave	121C/100% RH, 96 hrs	11	11	0

Table 5 An example of SIP qualification at level 2 for portable computer application

SiP Level 2 Tests	Environmental Condition	In	Out	Rejects
Operational Test	10 cycles, 50% RH, Ambient/35C, 2 hrs, 35C/10C, 2 hrs,	6	6	0
Non-Operational Test	10 cycles: uncontrolled RH, Ambient/85C, 15 min 85C/-40C 15 min	6	6	0
Non-Operational Storage Test	-20C & 65C 72 hrs @ each temp	6	6	0
Four Corner Temp/humidity Test	0C, 5% RH 0C, 95% RH 45C, 5% RH 45C, 95% RH 24 hours each condition	6	6	0

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