Interferometer Real Time Control Development for SIM

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ABSTRACT

Real Time Control (RTC) for the Space Interferometry Mission will build on the real time core interferometer control technology under development at JPL since the mid 1990s, with heritage from the ground based MKII and Palomar Testbed Interferometer projects developed in the late '80s and early '90s. The core software and electronics technology for SIM interferometer real time control is successfully operating on several SIM technology demonstration testbeds, including the Real-time Interferometer Control System Testbed, System Testbed-3, and the Microarcsecond Metrology testbed.

This paper provides an overview of the architecture, design, integration, and test of the SIM flight interferometer real time control to meet challenging flight system requirements for the high processor throughput, low-latency interconnect, and precise synchronization to support microarcsecond-level astrometric measurements for greater than five years at 1 AU in Earth-trailing orbit. The electronics and software architecture of the interferometer real time control core and its adaptation to a flight design concept are described. Control loops for pointing and pathlength control within each of four flight interferometers and for coordination of control and data across interferometers are illustrated. The nature of on-board data processing to fit average downlink rates while retaining post-processed astrometric measurement precision and accuracy is also addressed.

Interferometer flight software will be developed using a software simulation environment incorporating models of the metrology and starlight sensors and actuators to close the real time control loops. RTC flight software and instrument flight electronics will in turn be integrated utilizing the same simulation architecture for metrology and starlight component models to close real time control loops and verify RTC functionality and performance prior to delivery to flight interferometer system integration at Lockheed Martin's Sunnyvale facility. A description is provided of the test environment architecture supporting the RTC path to flight.

Keywords: Interferometer, real-time control, low-latency, interconnect, instrument flight software

1. INTRODUCTION

The Space Interferometry Mission scheduled for launch into Earth trailing orbit in 2009 will utilize Michelson optical interferometers with baselines on the order of 10 meters operating in coordination to make high precision measurements of the relative angular positions between pairs of stars. Systematic sequences of measurements across the full sky will provide for the buildup of a precision grid of reference stars whose angular positions within the grid are catalogued two orders of magnitude more accurately than currently available, enabling observation of star motions with sufficient sensitivity for indirect detection of orbiting planets down to a size of a few Earth masses or better.

Figure 1: SIM Flight System

1.1 Flight system overview

A concept drawing of the deployed SIM flight system on orbit is shown in Figure 1. The fundamental relative angular position measurement made by a SIM interferometer is depicted in Figure 2. Internal metrology guages track changes in the distance of the path the white light takes from the siderostat to the detector in the beam combiner of each interferometer.

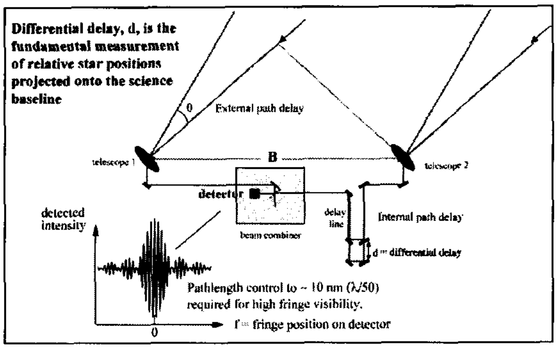

Figure 2: Measurement of relative star positions

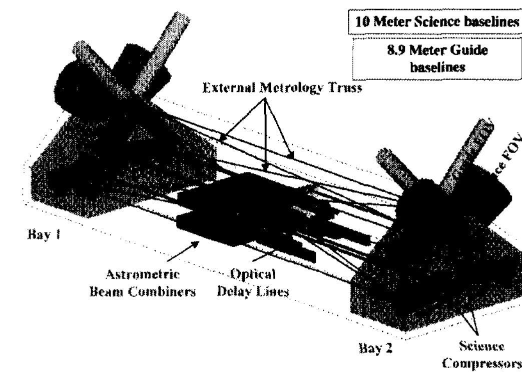

Figure 3: Interferometer configuration

A concept drawing of the SIM Interferometer assembly is shown in Figure_. [ref] Two science interferometers and two guide interferometers are integrated with all baselines parallel. The guide interferometers share a common siderostat in each arm. Each of the two guide interferometers tracks a different single guide star to provide a 3-axis guide reference frame within which a science interferometer makes a set of measurements. Also shown in Figure_ is the external metrology truss, a frame of metrology guages that track the relative orientation between each science baseline and the guide baseline.

1.2 Real Time Control subsystem overview

The interferometer Real Time Control subsystem is shown in the context of the other subsystems of the flight system in Figure_. The susbsytems include the Spacecraft subsystem (SCS), Precision Structure subsystem (PSS), Starlight subsystem (STL), and the Metrology subsystem (MET). Not shown is the sixth subsystem, the Integral Propulsion Module (IPM), which brings the flight system from low earth orbit to Earth trailing orbit. RTC external interfaces include connections to SCS for power and data, and connections with STL and MET for reading sensors and commanding actuators for interferometer real time control loops and telemetry. Interferometer science and engineering telemetry is stored on the spacecraft solid state recorder between the periodic downlink sessions.

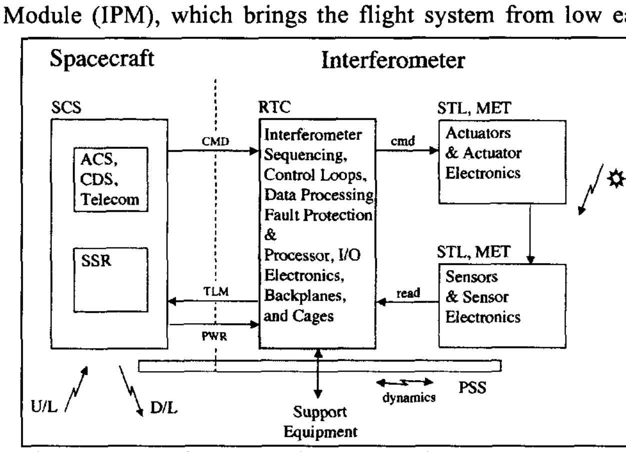

Figure 4: Real Time Control subsystem (RTC) context

Representative spacecraft telemetry rates to ground in the range of 1.0 Gbit/hr at beginning of mission and 0.1 Gbit/hr at end of mission (L+5.5 yr) would accommodate an average interferometer telemetry stream from RTC to the spacecraft solid state recorder in the neighborhood of 0.02 Gbit/hr through most of the mission within downlink totals of 20 hours/wk. A solid state recorder of 48.0 Gbit buffers the telemetry data between downlink passes with margin for lost passes. Averaging and compression in RTC will provide the needed data reduction from a typical raw interferometer data stream of several Gbit/hr to the 0.02 Gbit/hr fill rate of the solid state recorder.

Real time control of siderostats, fast steering mirrors, and alignment actuators provides for proper pointing and alignment of the white light and metrology beams within the interferometer from the siderostats through the transfer optics, into the beam combiner, and onto the CCD detector. Real time control of a delay line and pathlength modulator provides for control of the central fringe position on the detector to within 10 nm to maintain high fringe visibility and minimum measurement noise.

The equipment list for the reference design interferometer will be developed in support of system requirements review scheduled in 2003 and further developed for system preliminary design review scheduled in 2005. Today significant STL, MET, and RTC design and implementation experience is being gained in technology development testbeds currently in operation.

2. RTC TECHNOLOGY DEVELOPMENT

The MKIII stellar interferometer was successfully operated on Mount Wilson in the early 1990s, demonstrating the use of general purpose processor boards for high rate real time pointing and phasing control for precision relative angular position measurements between star pairs. The techniques were further refined with the successful development and operation of the Palomar Testbed Interferometer in the mid 1990s. These systems implemented multiple Motorola 680xx processors, VME backplane, and reflective memory to provide kilohertz sampling and commanding for the 100 Hz bandwidth phasing control loops, and integral slower rate groups for pointing control.

A next generation core RTC system has since been developed within the Interferometry Technology Program and SIM Project in several technology development testbeds. These testbeds developed the core system utilized for Keck Interferometer on Mona Kea and prototype real time software for the Starlight and SIM flight missions. The first of the next generation testbeds, the Realtime Interferometer Control Software Testbed (RICST), was assembled in 1996 (Fig. 5). RICST is a hardware-in-the-loop single baseline interferometer with a laser or white light point source, beam combiner, phasing control (avalanche photodiode detector, delay line, internal metrology), and pointing control (CCD camera, fast steering mirror, and siderostat).

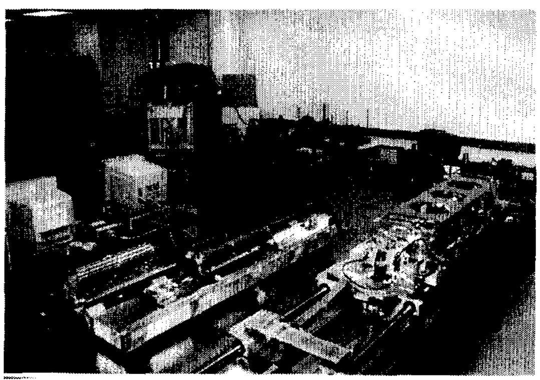

Figure 5: RICST single-interferometer testbed

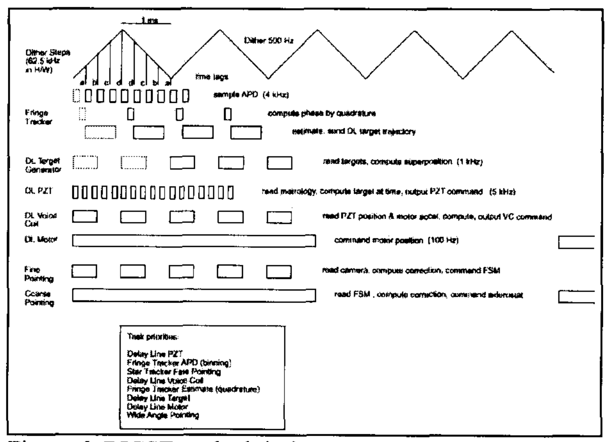

Figure 6: RICST testbed timing

The RICST interferometer testbed has supported incremental development of an RTC core executive and representative

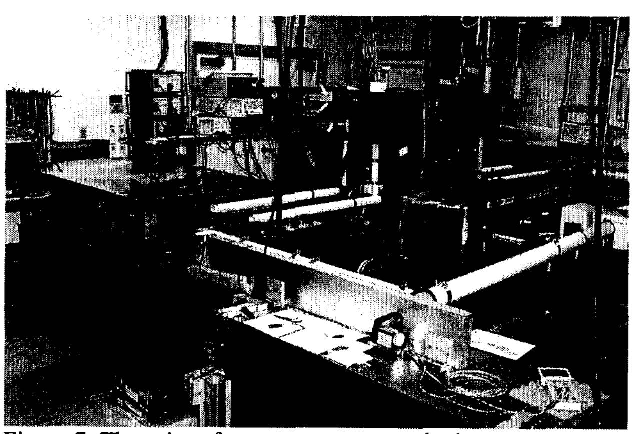

Figure 7: Three-interferometer system testbed STB-3

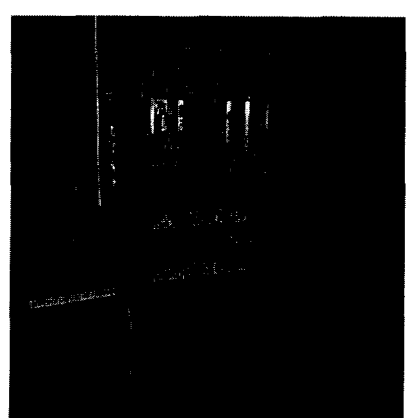

Figure 8: STB-3 real time control rack

interferometer software applications for phasing control, pointing control, and telemetry. A RICST timing diagram (Fig. 6) illustrates typical sampling and commanding rates for interferometer phasing and pointing control. A triangular dither waveform provides for fringe phase detection with avalanche photodiode sampling at 4.0 kHz and and phase estimation at 1.0 kHz. Delay line voice coil commanding occurs at 1.0 kHz and delay line pzt commanding occurs at 5.0 kHz. Pointing control commanding of the fast steering mirror and siderostat are commanded at lower rates, below 1.0 kHz.

The interferometer software and hardware developed for RICST were applied to the System Test Bed 3 (STB-3), a three-baseline interferometer developed in 1999 and 2000 which successfully demonstrated the feasibility of controlling the position of the science interferometer fringe position on the science detector using the real time fringe position

Figure 9: Microarcsecond metrology (MAM) operation

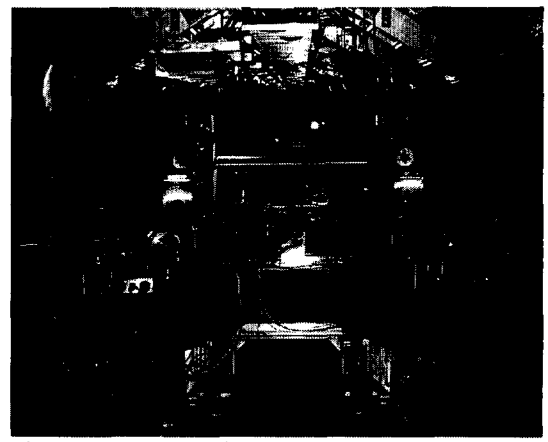

Figure 10: MAM testbed in vacuum chamber

measurements from two guide interferometers. The real time control architecture of STB-3 is similar to that envisioned for the SIM flight system, with a separate flight computer for each interferometer and one for the external metrology truss that references the interferometer baselines within a common frame (Fig. 7). Three interferometer computers currently share the same VME backplane in the current STB-3 testbed (Fig. 8). The next phase of STB-3 development will separate the interferometer computers into separate electronics cages connected by a high speed interconnect as planned for flight RTC.

The RTC technology developments of RICST and STB-3 are currently being applied in the Microarcsecond Metrology testbed (MAM-1), a demonstration in vacuum that the sub-aperture internal metrology guage provides a faithful measurement of the path length traversed by the full aperture starlight beam through the instrument from each siderostat through transfer optics and beam combiner to the detector (Fig. 9). Unlike RICST and STB-3, MAM-1 is operated in vacuum (Fig. 10) and fringe measurement and control are performed with flight-like CCD detector and with the fringe dispersed across a row of several pixels. Pathlength modulation for fringe phase measurement and control is provided by voicecoil modulation of a full-aperture flat on MAM-1 as an alternative to a cats-eye focus to a pzt actuated flat on RICST and STB3. Sample and command rates for interferometer pointing and phase control are similar for the three testbeds. A timing circuit board with a common design on the three testbeds provides time synchronization of signals for sampling and commanding of interferometer functions occurring at the different sampling and commanding rates. The three technology testbeds utilize PowerPC computer boards with VxWorks operating system, with real time software coded in C++.

SIM flight RTC subsystem concept development is proceeding on several fronts in parallel with the technology testbed developments. These include RTC subsystem engineering, electronics, control analysis, simulation software, flight software, and subsystem integration and test. An overview of each of these developments is provided in the following sections.

3. RTC SUBSYSTEM ENGINEERING

RTC subsystem engineering develops subsystem requirements and design, including interfaces between RTC assemblies and between RTC assemblies and integration and test support equipment.

3.1 Requirements flowdown

The Real Time Control subsystem is one of six subsystems comprising the SIM flight system as outlined in Section 1.2. The functions required of the real time control subsystem by flight system are identified in one branch of the requirements tree. A functional decomposition tree illustrated in Fig. 11 shows the relationship of each level-4 subsystem (e.g., RTC), to the systems and project functional elements above, and the component assemblies of each subsystem below. Following a branch of the requirements tree in the accompanying Fig. 12 (branch 2 of the tree is used for illustration in the figures) shows the contents of requirements documents at each level of the functional breakdown structure. The subsystem development team is responsible for development of level-4 functional requirements and for providing support to the development of level-3 and level-2 requirements above and the subsystem's level-5 requirements below. Real Time Control subsystem specifies subsystem-wide design requirements and what is required of each RTC assembly in order to meet functions required by flight system according to the requirements flow-down process below. In level-2 requirements, project specifies project-wide design requirements and what is required of each level-3 system in order to meet the level-1 requirements on the project.

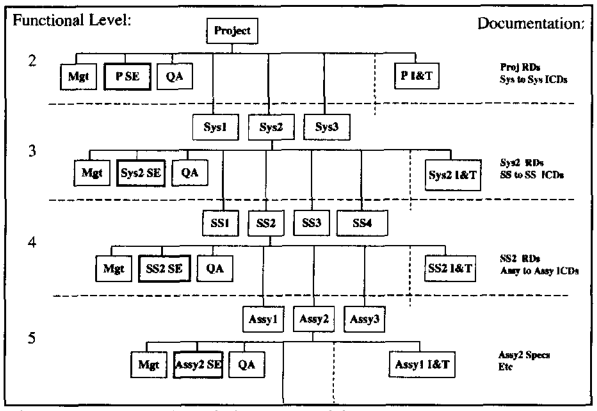

Figure 11: Functional decomposition tree

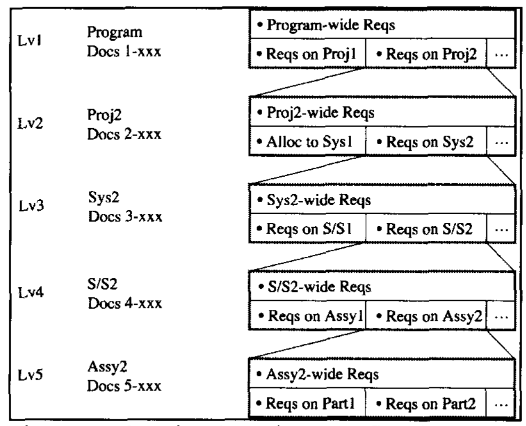

Figure 12: Functional requirements flowdown

In level-3 requirements, each system specifies system-wide design requirements and what is required of each of its level-4 subsystems in order to meet the level-2 requirements on that system.

In level-4 requirements, each subsystem specifies subsystem-wide design requirements and what is required of each of its level-5 assemblies in order to meet the level-3 requirements on that subsystem.

3.2 Subsystem design

RTC subsystem engineering establishes a subsystem design that performs the functions and subsystem-to-subsystem interfaces required of RTC by flight system in level-3 functional requirements. The subsystem design also supports the subsystem-wide requirements, assembly-to-assembly interfaces, and required functions of RTC assemblies as elaborated in RTC level-4 requirements. The functional requirements are being developed in preparation for SIM system requirements review scheduled in 2003.

The RTC subsystem flight design concept is architecturally similar to the representation of RTC in the technology testbeds. For the flight RTC subsystem, one flight computer is assigned to each of the four flight interferometers and one flight computer is assigned to each of the two external metrology trusses, for a total of six flight computers including redundancy (Fig. 13). This matches the STB-3 testbed architecture, which has one computer per interferometer and one computer for the external metrology truss. STB-3 omits the redundant interferometer and redundant external metrology truss needed for flight.

Local communication within an electronics cage utilizes the VME backplane directly. A high speed interconnect provides for low-latency communication between electronics cages. Sensor and actuator electronics supplied by the Starlight and Metrology subsystems are hosted in the RTC electronics cages using the VME backplane interface. Electronics associated with the highest sample and command rate loop requirements are in the same cage as the flight computer, as is the case for each of the four interferometer computers which support the high rate phasing loops directly

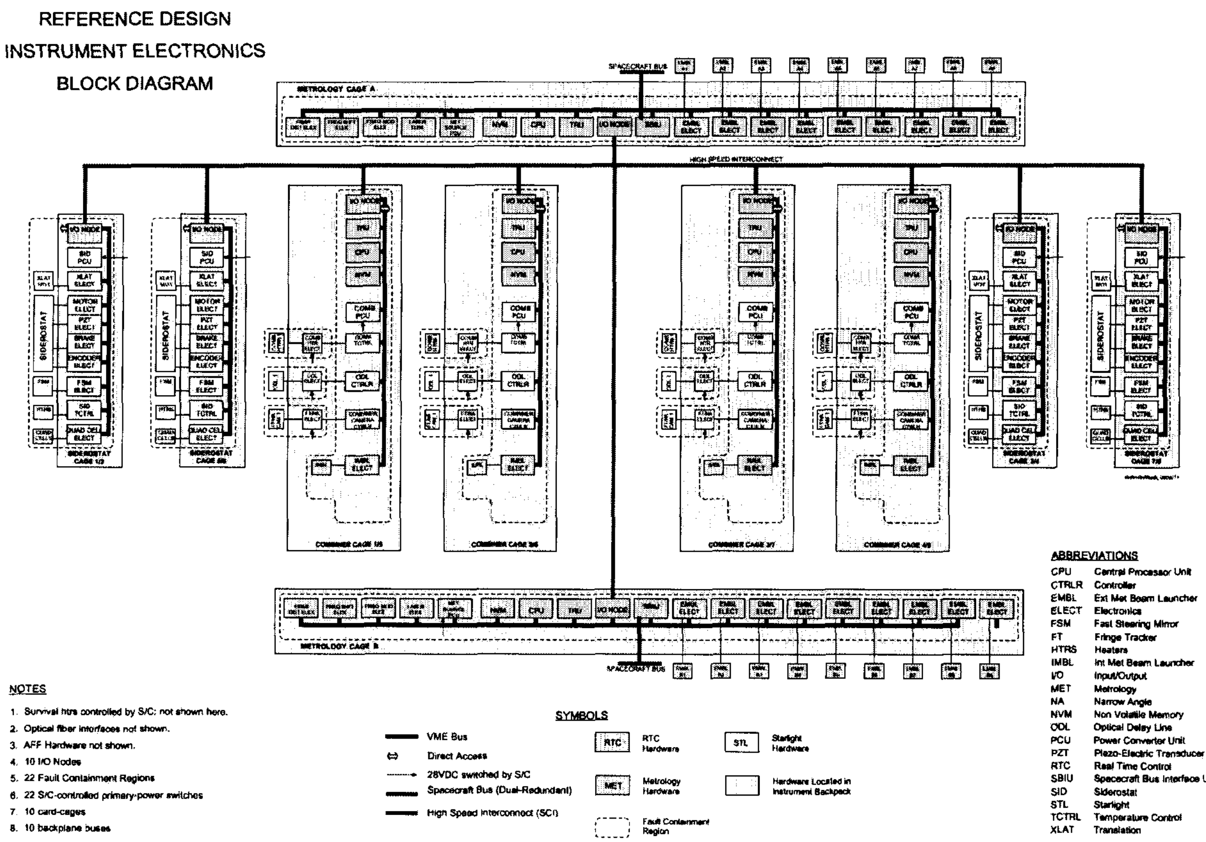

Figure 13: Interferometer electronics block diagram

through the VME backplane. Lower rate pointing loops utilize the high speed interconnect for sample and command traffic between the siderostat cages and the flight computer cages.

4. RTC ELECTRONICS

Primary hardware components of the Interferometer Real Time Control Subsystem flight electronics are the interferometer flight computer boards and the high speed interconnect I/O boards. Building on SIM technology testbed developments, the reference includes PowerPC flight computer boards with VME interface. For the high speed interconnect between cages various options are under consideration for flight implementation, including the IEEE 1596 scalable coherent interconnect, which provides for communication of sample and command data packets between electronics cages with latency in the range of 10 microseconds or less. Commercial IEEE 1596 scalable coherent interconnect I/O boards, have been tested in anticipation of their use on STB-3 for checkout of low latency data transfer between interferometer computer cages in the next phase of STB-3 development.

The flight computers and data busses of RTC subsystem together with the sensor and actuator electronics of the Starlight and Metrology subsystems provide the processing throughput, redundancy management, and radiation tolerance required to support interferometer flight software functions. A processing throughput of several hundred MIPS per flight computer is required to support command and telemetry functions concurrently with operation of the high rate pointing, metrology, and phasing control loops in science operational modes. Fault containment regions isolate propagation of failures to preserve redundant capability. Radiation hardness to a total ionizing dose of 30 kRad including margin is expected to satisfy requirements for the SIM Earth trailing orbit. As a part of the RTC electronics development activity, Starlight and Metrology electronics boards are integrated with RTC boards for cage assembly testing prior to subsystem integration testing and electronics cage environmental testing.

The multi-processor SIM RTC architecture supports partitioning of functionality across RTC flight computers and local microcontrollers in Starlight and Metrology sensor and actuator electronics for flexibility in subsystem partitioning, software development, and flight system implementation, integration, and test. Data bus latency requirements are driven by the closure of three concurrent sets of phasing control loops with sampling rates in the kilohertz and the associated estimators, pointing control, and related functions. Single fault tolerance capability also drives the maximum allowable latencies across the instrument data bus.

5. CONTROL ANALYSIS

The RTC control analysis team develops and delivers interferometer real time control algorithms to be incorporated in the RTC flight software. Algorithms are developed and tested in a simulation environment with tools for setting up control architecture, timing structures, and models of the interferometer plant, sensors and actuators. Control algorithms are coded in a convenient language (e.g., C) for development, test, delivery, and incorporation in flight software. Hardware models developed for control analysis simulation are designed for use as common models in the flight software test and subsystem integration and test environments.

Control analysis simulations of interferometer fringe tracking and pointing algorithms have been developed by the RTC control analysis team for assessment of function and performance for both technology testbeds and flight RTC subsystem. A simulation of fringe tracking with the avalanche photodiode detector and simplified delay line model has been utilized in the development and verification of RICST and STB-3 delay line and fringe tracking software functions. The fringe tracking model has since been extended for the case of dispersed fringe tracking with a CCD detector and has been utilized in development and verification of the fringe tracking algorithm currently being implemented on MAM-1. Further extensions of the RTC control analysis model will build up the remaining pointing and phasing control functions for a full interferometer, then for coordinated operation of multiple interferometers.

Realization of the interferometer control algorithms in a high fidelity discrete time simulation environment must not only demonstrates that real time control performance requirements (e.g., control of fringe position on the detector to within 10 nanometers 1-sigma) are met, but also that the interferometer sampled data telemetry streams will be free of systematic errors and other real effects which would prevent science processing of the measurement data on the ground to the required microarcsecond performance levels.

6. SIMULATION SOFTWARE

Simulation software development establishes the test environment for virtual real time interferometer flight software testing. Much of the simulation software can be adapted also to the hardware substitution test environment of subsystem integration and test.

Hardware component models from the control analysis simulation are adapted with models of the flight hardware-to-software interfaces to provide a simulation environment for testing of the interferometer flight software builds without any required modification to the build. The simulation software provides a fully simulated test environment for testing flight software. Once developed, this software simulation testbed is easily and inexpensively replicated to multiply the throughput of software testing by the flight software development team, avoiding testbed bottleneck..

Interfaces between flight test article and test environment are formally represented in the simulation software, as are also the interfaces between flight software and flight hardware. These constraints in the architecture of the simulation software enables commonality of hardware models and enables substitution of hardware for simulated elements for hardware-in-the-loop subsystem integration testing. The flight test article to test environment interface in the software simulation testbed is illustrated in Fig. 14.

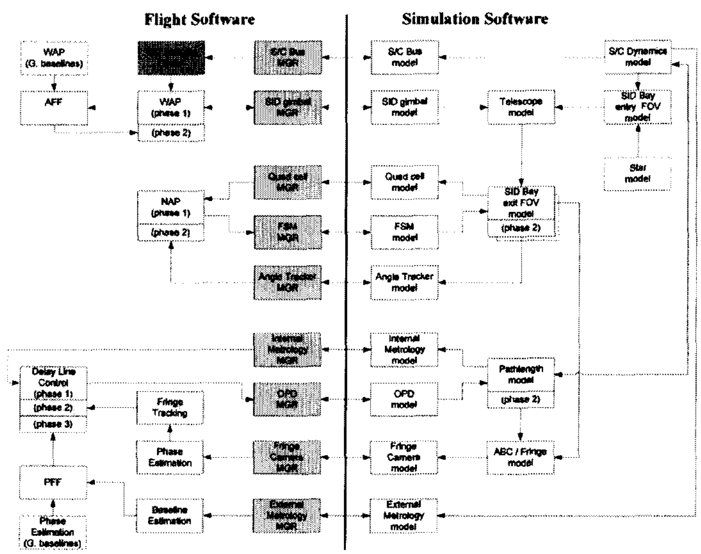

Figure 14: Flight software to simulation software interface

Current efforts in the development of the RTC flight software development environment will support development and test of RTC prototype interferometer flight software for an initial set of functions including flight software executive, commanding, pointing, fringe acquisition, fringe tracking, and telemetry in preparation for system requirements review and preliminary design review. Subsequent simulation software developments will add support for a complete set of RTC functions and modes according to the RTC flight software development plan.

A real time flight software development testbed will complement the simulation-only environment by incorporating commercial or breadboard versions of the RTC flight computers and the high speed interconnect and spacecraft bus hardware. This extension of the software development environment provides early verification of the flight software operating system and executive on the target computer during software development testing and prior to software delivery for subsystem integration and test. The real time software development testbed includes the flight system interfaces between RTC and SCS to enable integration with the corresponding SCS flight software testbed to form a flight system testbed for integrated RTC and SCS flight software verification. The combined flight system testbed will be delivered to Mission System for sequence testing with the integrated SCS and RTC flight software builds prior to start of project level integration in ATLO (Assembly, Test and Launch Operations).

7. INTERFEROMETER FLIGHT SOFTWARE

SIM interferometer flight software implements the set of in-flight real time command, data, and control functions required to operate the SIM flight instrument and achieve instrument science objectives. Examples of interferometer command and data functions include: 1) Startup and initialization, 2) Command and sequence decoding and execution, 3) Instrument hardware and software configuration management, 4) Fault detection, isolation, and recovery, 5) Configurable telemetry collection, buffering, and 6) Data compression and packetizing for spacecraft bulk storage and downlink.

The SIM instrument data system will satisfy requirements for ground testability as well as on-orbit science gathering, performance characterization, and fault diagnosis. Configurable telemetry collection provides required visibility into the instrument operation through selection of specified data and collection rates for inclusion in the instrument telemetry along with or in place of nominal science and engineering data streams. Interferometer system fault protection maintains and restores nominal instrument operability through autonomous or ground assisted reconfiguration around failures or faults. Examples of interferometer control functions include: 1) Pointing alignment and control, 2) Guide and Science fringe phase sensing and control, 3) Pathlength feedforward control of science fringe, 4) Guide and science optical path difference estimators, and 5) Baseline orientation estimators

Pointing acquisition and control utilizes siderostat and steering mirror articulation to acquire and hold a guide star image on the beam combiner pointing detectors. Alignment control establishes and maintains the laser and starlight beam geometries within allowable tolerances.

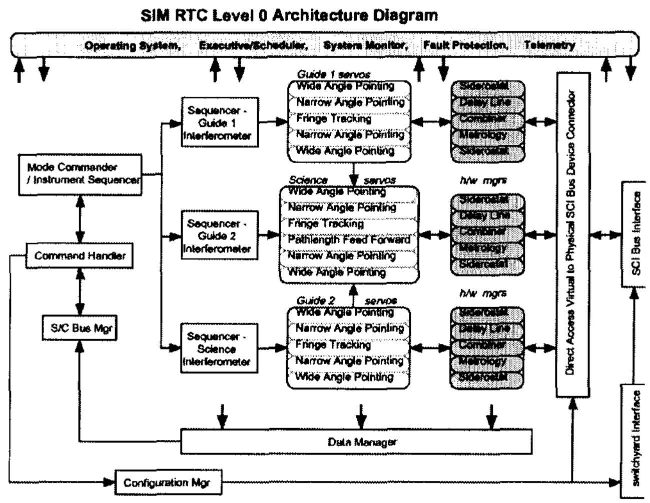

Figure 15: Top level RTC flight software architecture

Baseline length and orientation estimators incorporating guide star and metrology inputs maintain the reference orientations against which science fringe offsets are measured. Interferometer control functions establish and maintain starlight and metrology beam alignment and support instrument calibration functions. Operational modes for astrometric science and the various instrument support functions follow a state transition heirarchy designed for testability and in-flight operational reliability.

Pointing control sensors read by RTC that support coarse and fine pointing functions include quad cells and beam combiner pointing CCD. Pointing control actuators commanded by RTC include siderostats, fast steering mirrors, and other transfer optics. Fringe phase control sensors and actuators are sampled and commanded to perform metrology guage acquisition and tracking, fringe acquisition and tracking, optical path difference estimation, and feedforward of estimated optical path difference to the science baseline. Phase sensors include internal metrology guage, external metrology guage, and beam combiner dispersed fringe CCD. Phase actuators include delay line coarse motor, and voice coil for fine control and dither.

RTC flight software receives sequences for The SIM Interferometer depends on the spacecraft flight software to maneuver to the correct inertial orientation for each tile observation. With the spacecraft oriented and settled at a tile location, the spacecraft holds orientation while the interferometer runs through a tile sequence of target and reference star observations. With the completion of each interferometer tile sequence, the spacecraft maneuvers to the next tile location and the interferometer executes the sequence for the next tile. The cycle repeats until the spacecraft and interferometer have completed a planned sequence of tiles and spacecraft and interferometer await the start time for the next sequence of tile observations.

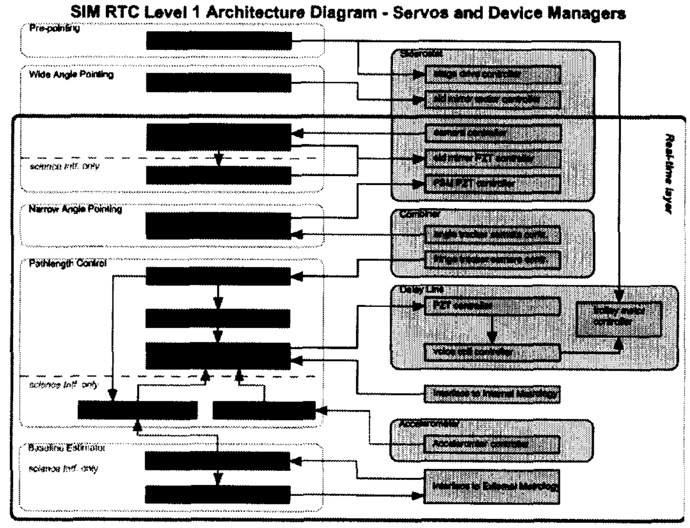

Figure 16: Level 1 RTC flight software architecture

8. RTC INTEGRATION AND TEST

The RTC integration and test team develops the test environment within which the RTC flight article will be tested and conducts integration and test prior to delivery of the subsystem for system integration and test at Lockheed Martin Sunnyvale. Flight dynamics models from the flight software development testbeds are adapted for the RTC hardware and software integration and test environment. Starlight and Metrology electronics are integrated to the VME backplane

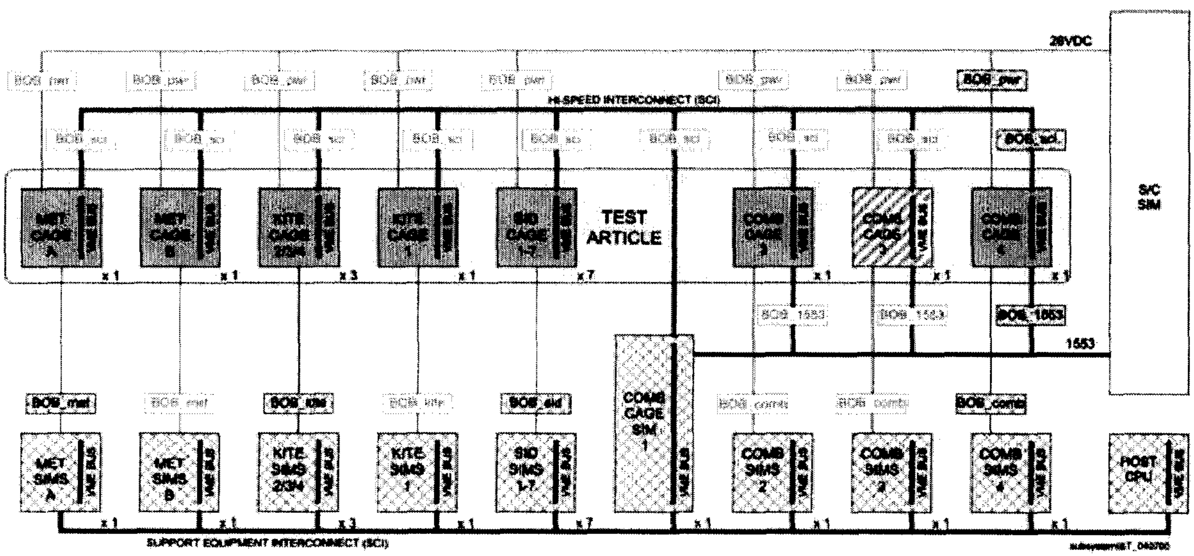

Figure 17: RTC subsystem hardware and software integration

in each RTC electronics cage by the RTC Electronics team prior to delivery for RTC subsystem integration and test. Starlight and Metrology hardware models from the RTC software development testbeds are adapted to the electronics interfaces for closed loop testing with the RTC flight software builds. A representative subsystem integration configuration for RTC hardware and software integration (Fig. 17) shows the interferometer electronics cages, high speed interconnects, and associated simulators and breakout boxes (BOB's) for subsystem integration and test. The electronics cages include the beam combiner cages, siderostat cages, internal metrology cages, and external metrology truss (kite) cages. Wherever hardware is not available to support testing, hardware simulators are used in place to preserve full subsystem functionality for continuity of testing. RTC subsystem tests will include testing to the same procedures planned for system test in order to identify problems early and minimize debug time in the system level tests at Sunnyvale. Hardware simulators and simulation software developed for RTC subsystem integration and test are delivered along with the flight subsystem to ensure continuity of full subsystem functionality in support of flight system integration and ATLO.

9. CONCLUSIONS

The role of the interferometer real time control subsystem within the SIM flight system has been described along with an overview of interferometer RTC flight subsystem development activities and related RTC technology development in the SIM technology testbeds. Key design requirements for this challenging flight subsystem include a multiprocessor architecture with hundreds of MIPS required per flight computer, a high speed interconnect between electronics cages with latency less than 10 microseconds, and precision synchronization of multiple high rate interferometer sample and control loops to support both onboard real time control requirements and interferometer science data processing on the ground. The RTC software development environment and subsystem integration and test environment are produced in support of subsystem delivery and subsequently provide important test capability for sequence testing by SIM mission system, flight system integration, and assembly, test, and launch operations (ATLO).

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